IPD series for Automotive

8ch Low-side switch

BD8LA700EFV-C

Features
- Monolithic power IC that has a built-in control part (CMOS) and a power MOS FET on 1chip
- 8ch Low-side switch for driving resistive, inductive load
- 16bit Serial peripheral interface(SPI) for diagnostics and control
- Built-in Open Load Detection circuit in output-off state
- Built-in Over Current Protection circuit (OCP)
- Built-in Active Clamp circuit
- Built-in Thermal shutdown circuit (TSD)
- Low On resistance of R_{ON}=700mΩ(V_{IN}=5V, Tj=25°C, Io=0.2A, Typ)
- Surface mount HTSSOP-B24 Package
- AEC-Q100 Qualified (Note 1)

(Note 1) Grade1

Product Summary

Digital part Operating voltage	3.0V to 5.5V
Analog part Operating voltage	4.0V to 5.5V
On-state resistance（25°C,Typ）	700mΩ
Over current limit（Typ）	1.2A
Active clamp energy(25°C)	75mJ

Package

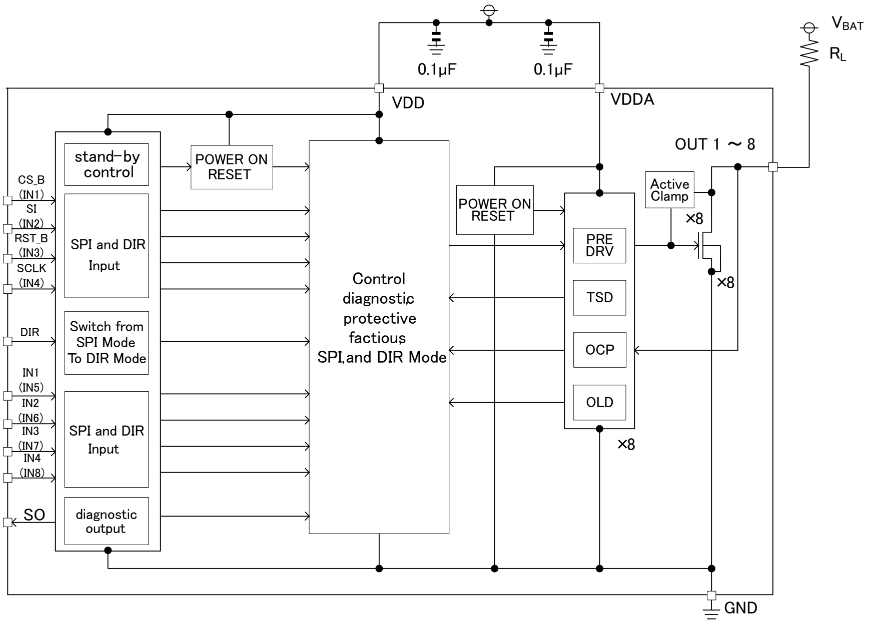
	W(Typ) x D(Typ) x H(Max)
HTSSOP-B24	7.80mm x 7.60mm x 1.00mm

HTSSOP-B24

Overview
BD8LA700EFV is 8ch Low-Side switch for automotive and industrial equipment. It has a built-in, Open Load Detection circuit, Over Current Protection circuit, Active clamp circuit and Thermal Shutdown circuit.

Application
For driving resistive, inductive load

Basic Application Circuit (Recommendation)



〇Product configuration: Silicon monolithic integrated circuit 〇The product is not designed for radiation resistance.

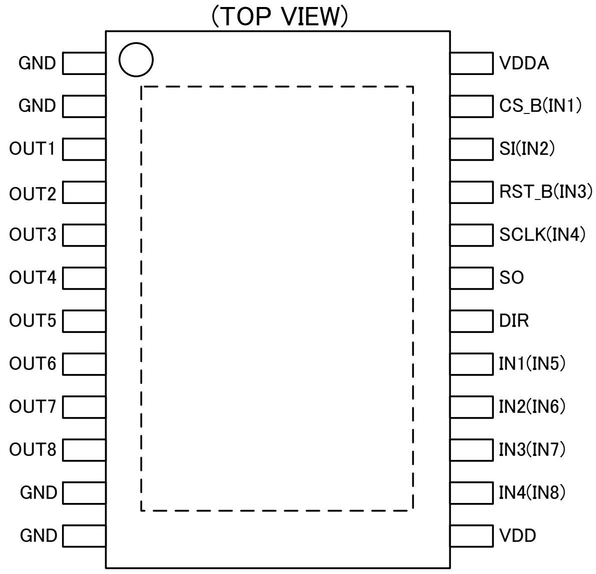
Pin Descriptions

Pin	Symbol	I/O(Note 1)		Function
1	GND	-		GND
2	GND	-		GND
3	OUT1	O		Channel 1 output
4	OUT2	O		Channel 2 output
5	OUT3	O		Channel 3 output
6	OUT4	O		Channel 4 output
7	OUT5	O		Channel 5 output
8	OUT6	O		Channel 6 output
9	OUT7	O		Channel 7 output
10	OUT8	O		Channel 8 output
11	GND	-		GND
12	GND	-		GND
13	VDD	-		Digital power supply
14	IN4(IN8)	I	PD	Control input for Channel 4 and 8 (DIR=L) / Control input for Channel 8 (DIR=H)
15	IN3(IN7)	I	PD	Control input for Channel 3 and 7 (DIR=L) / Control input for Channel 7 (DIR=H)
16	IN2(IN6)	I	PD	Control input for Channel 2 and 6 (DIR=L) / Control input for Channel 6 (DIR=H)
17	IN1(IN5)	I	PD	Control input for Channel 1 and 5 (DIR=L) / Control input for Channel 5 (DIR=H)
18	DIR	I	PD	SPI mode, DIR mode change input terminal
19	SO	O		Serial data output terminal
20	SCLK(IN4)	I	PD	Serial clock (DIR=L) / Control input for Channel 4 (DIR=H)
21	RST_B(IN3)	I	PD	Reset terminal (DIR=L) / Control input for Channel 3 (DIR=H)
22	SI(IN2)	I	PD	Serial data input (DIR=L) / Control input for Channel 2 (DIR=H)
23	CS_B(IN1)	I	PU/PD (Note 2)	SPI enable input (DIR=L) / Control input for Channel 1 (DIR=H)
24	VDDA	-		Analog power supply
FIN	FIN	-		Since it has connected with sub of IC, please connect the heat dissipation metal to external GND potential.

(Note 1) O：Output terminal, I：Input terminal
PD：Pull Down terminal, PU：Pull Up terminal
(Note 2) Pull Up at DIR=Low setting, Pull Down at DIR=High

Pin Configurations

HTSSOP-B24
(TOP VIEW)



Absolute Maximum Ratings

Item	Symbol	Limit values	Unit
Power supply voltage (Pin No:13,24)	V_{CC}	-0.3 to +7	V
Output voltage (Pin No:3 to 10)	$V_{DS1\sim8}$	-0.3 to 45(Internally limited)	V
Output current (Pin No:3 to 10)	I_{Dn}	0.5(Internally limited) (Note 1)	A
Diagnostic output voltage (Pin No:19)	V_{SO}	-0.3 to +7	V
Input voltage(Pin No:14 to 18,20 to 23)	V_{IN}	-0.3 to +7	V
Junction temperature range	T_j	-40 to +150	°C
Storage temperature range	T_{stg}	-55 to +150	°C
Maximum junction temperature	T_{jmax}	150	°C
Active clamp energy (single pulse) ($Tj_{(0)}$=25°C)	E_{S1}	75(Note 2)	mJ
Active clamp energy (single pulse) ($Tj_{(0)}$=150°C)	E_{S2}	25(Note 3)	mJ
Active clamp energy (repetitive) ($Tj_{(0)}$=105°C)	E_{AR}	20(Note 4)	mJ

(Note 1) However, never exceed T_{jmax}.
(Note 2) Max Active clamp energy at $T_{j(0)}$ = 25°C, using single non-repetitive pulse of 0.5A
(Note 3) Max Active clamp energy at $T_{j(0)}$ =150°C, using single non-repetitive pulse of 0.5A. Not 100% tested.
(Note 4) Max Active clamp energy at $T_{j(0)}$ =105°C, using repetitive pulse of 0.4A and cycles of 1M times. Not 100% tested.

Operating Voltage Ratings（-40°C ≤Tj ≤+150°C）

Item	Code	Limit values	Unit
Digital part Operating voltage	V_{DD}	3.0 to 5.5	V
Analog part Operating voltage	V_{DDA}	4.0 to 5.5	V

Electrical Characteristics（**unless otherwise specified, V_{DDA}=V_{DD}=5V, -40°C≤Tj ≤+150°C**）

Item	Symbol	Limit values Min	Typ	Max	Unit	Condition
[Power Supply Block]						
VDDA Standby current (All output on standby mode)	I_{DDAS}	-	0	20	μA	V_{DDA}=V_{DD}=V_{CS_B}=5V V_{RST_B}=0V
VDD Standby current (All output on standby mode)	I_{DDS}	-	0	20	μA	V_{DDA}=V_{DD}=V_{CS_B}=5V V_{RST_B}=0V
VDDA Operating current)	I_{DDA}	-	3.0	5.0	mA	V_{DDA}=V_{DD}=5V
VDD Operating current)	I_{DD}	-	0.5	1.0	mA	V_{DDA}=$_{VDD}$=5V
VDDA power on reset Threshold Voltage	V_{PORA}	-	-	4.0	V	
VDD power on reset Threshold Voltage	V_{POR}	-	-	2.7	V	
[Input PIN]						
L level input voltage	V_{INL}	0	-	VDD×0.2	V	
H level input voltage	V_{INH}	VDD×0.7	-	VDD	V	
Input Hysteresis	V_{HYS}	0.1	0.3	0.5	V	
L level input current 1 (RST_B,DIR,IN1 to IN4,SCLK,SI)	I_{INL1}	-10	0	10	μA	V_{RST_B}, V_{DIR}, V_{IN1} to V_{IN4}, V_{SCLK}, V_{SI}=0V
L level input current 2(CS_B)	I_{INL2}	-100	-50	-25	μA	V_{CS_B}=0V, V_{DIR}=0V
L level input current 3(CS_B)	I_{INL3}	-10	0	10	μA	V_{CS_B}=0V, V_{DIR}=5V
H level input current 1 (RST_B,DIR,IN1 to IN4,SCLK,SI)	I_{INH1}	25	50	100	μA	V_{RST_B}, V_{DIR}, V_{IN1} to V_{IN4}, V_{SCLK}, V_{SI}=5V
H level input current 2(CS_B)	I_{INH2}	-10	0	10	μA	V_{CS_B}=5V, V_{DIR}=0V
H level input current 3(CS_B)	I_{INH3}	25	50	100	μA	V_{CS_B}=5V, V_{DIR}=5V
[Power MOS Output]						
Output ON resistance	$R_{DS(ON)}$	-	0.70	0.87	Ω	V_{DD}=V_{DDA}=5V, I_{Dn}(Note 1)=0.2A, Tj=25°C
		-	1.30	1.56	Ω	V_{DD}=V_{DDA}=5V, I_{Dn}(note 1)=0.2A, Tj=150°C
Output leak current	$I_{L(OFF)}$	-	0	1	μA	V_{DS}=30V, Tj=25°C, V_{DIR}=0V
		-	5	20	μA	V_{DS}=30V, Tj=150°C, V_{DIR}=0V
Output leak current (Open load detected)	I_{OL}	15	40	90	μA	V_{DS} =40V, V_{DIR}=5V
Switching time	t_{ON}	-	30	50	μs	V_{DD}=5V, V_{INn}(Note 1)=0V/5V, R_L=60Ω, V_{BAT}=12V, V_{DIR}=5V
	t_{OFF}	-	30	50	μs	V_{DD}=5V, V_{INn}(Note 1)=0V/5V, R_L=60Ω, V_{BAT}=12V, V_{DIR}=5V
Slew rate on	dV/dt_{ON}	0.3	1.0	3.0	V/μs	V_{DD}=5V, V_{INn}(Note 1)=0V/5V, R_L=60Ω, V_{BAT}=12V, V_{DIR}=5V, 80% to 20% of V_{BAT}
Slew rate off	$-dV/dt_{OFF}$	0.3	1.0	3.0	V/μs	V_{DD}=5V, V_{INn}(Note 1)=0V/5V, R_L=60Ω, V_{BAT} =12V, V_{DIR}=5V, 20% to 80% of V_{BAT}
PWM Output range	f_{PWM}	-	-	5	kHz	V_{DD}=5V, V_{INn}(Note 1)=0V/5V, R_L=60Ω, V_{DIR}=5V, V_{BAT}=12V
Output clamp voltage	V_{CL}	45	50	55	V	I_{Dn}(Note 1) =1mA(output off state)

(Note 1) ” n” shows the channel number.

Electrical Characteristics（unless otherwise specified, V_{DDA}=V_{DD}=5V, -40°C≤Tj ≤+150°C）

Item	Symbol	Limit values			Unit	Condition
		Min	Typ	Max		
[Serial Output]						
L level output voltage	V_{SOL}	-	0.3	0.6	V	I_{SO}=1mA
H level output voltage	V_{SOH}	VDD-0.6	VDD-0.3	-	V	I_{SO}=-1mA
Serial out output leak current	$I_{SO(OFF)}$	-5	0	5	μA	
[Protect circuit]						
Over current detection current	$I_{OCP(ON)}$	0.5	1.2	2.0	A	
Over current detection time	t_{OCP}	400	1000	2200	μs	
Open load relase voltage	$V_{OLD(OFF)}$	1.2	2.5	3.5	V	
Open load detection voltage	$V_{OLD(ON)}$	1.0	2.0	3.0	V	V_{INn}(Note 1)=0V, V_{DIR}=5V
Open load detection time	t_{OLD}	50	150	600	μs	
TSD detection temperature(Note 2)	Tjd	-	175	-	℃	

(Note 1) ” n” shows the channel number.
(Note 2) Not 100% tested..

Definition

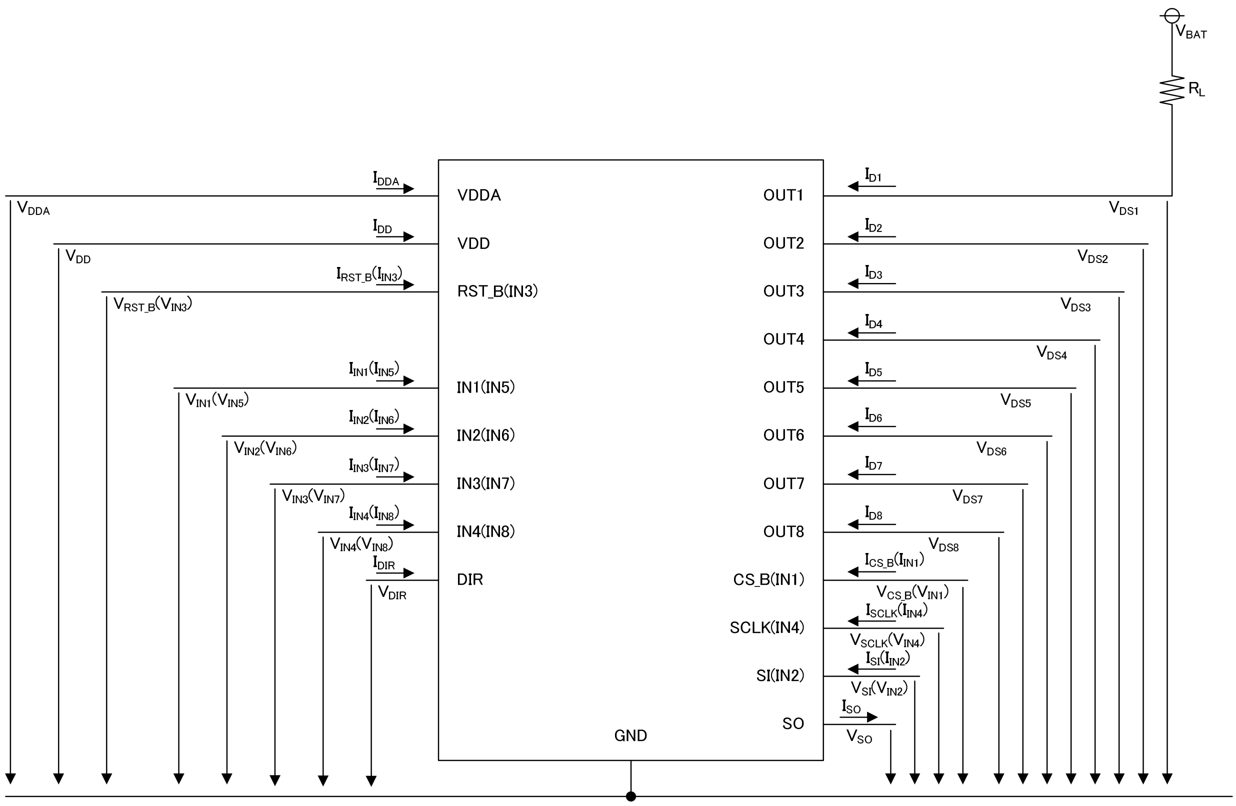


Figure 1. Definition

Measurement Circuit

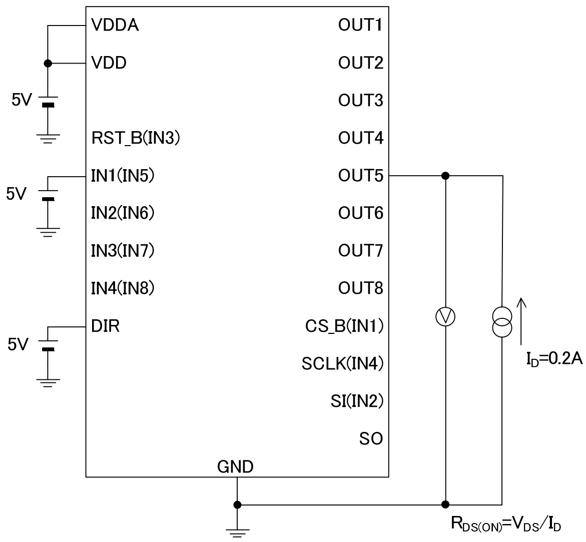


Figure 2. Output ON Resistance Measuring Circuit Diagram

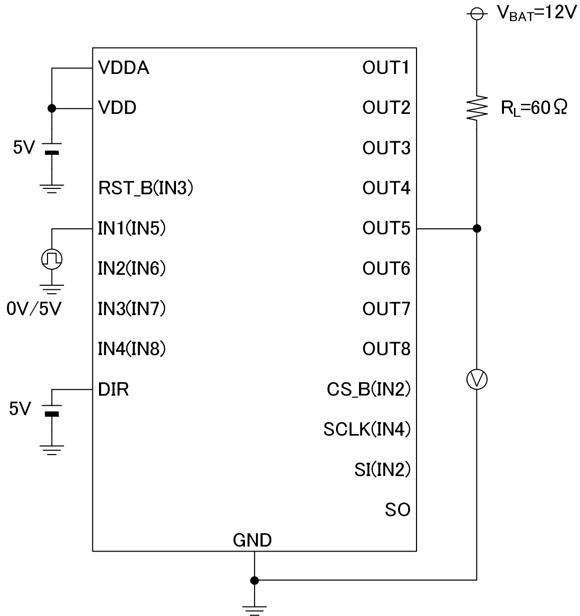


Figure 3. Switching Time Measuring Circuit Diagram

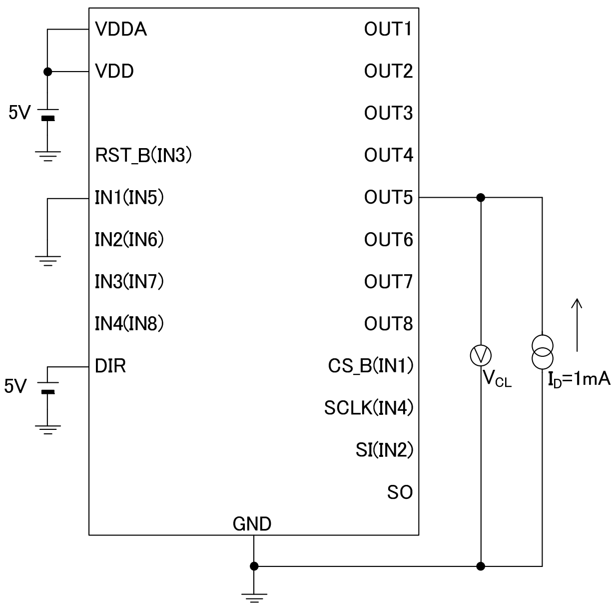


Figure 4. Output Clamp Voltage Measuring Circuit Diagram

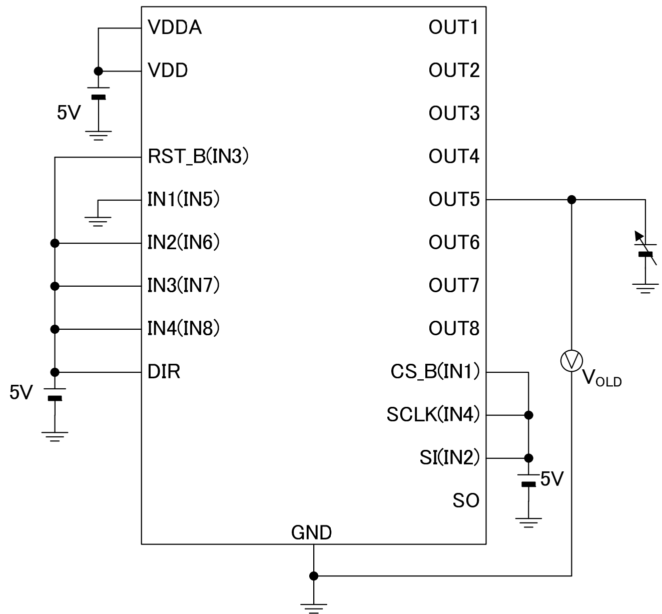


Figure 5. Open Detection Measuring Circuit Diagram

DIR(Direct)mode Diagnostic Output Truth Table

<table>
<tr><th rowspan="2">V_{IN}</th><th rowspan="2">TSD</th><th colspan="2">OUTPUT</th><th rowspan="2">mode</th><th rowspan="2">V_{SO}</th><th rowspan="2">Output state</th></tr>
<tr><th>V_{OUT}</th><th>I_{OUT}</th></tr>
<tr><td rowspan="3">H</td><td rowspan="2">OFF</td><td rowspan="2">-</td><td>I_D < 0.5A</td><td>Normal</td><td>L</td><td>ON</td></tr>
<tr><td>I_D ≥ 0.5 to 2.0A</td><td>Over current detection</td><td>H</td><td>OFF</td></tr>
<tr><td>ON</td><td>-</td><td>-</td><td>Thermal shut down</td><td>H</td><td>OFF</td></tr>
<tr><td rowspan="2">L</td><td rowspan="2">-</td><td>V_{DS} > 3.0V</td><td>-</td><td>Normal</td><td>L</td><td>OFF</td></tr>
<tr><td>V_{DS} ≤ 1.0 to 3.0V</td><td>-</td><td>Open load detection</td><td>H</td><td>OFF</td></tr>
</table>

Characteristic Data (Reference Data)　(V_{DD}=5V, V_{DDA}=5V, IN=5V, Tj=25°C unless otherwise is specified)

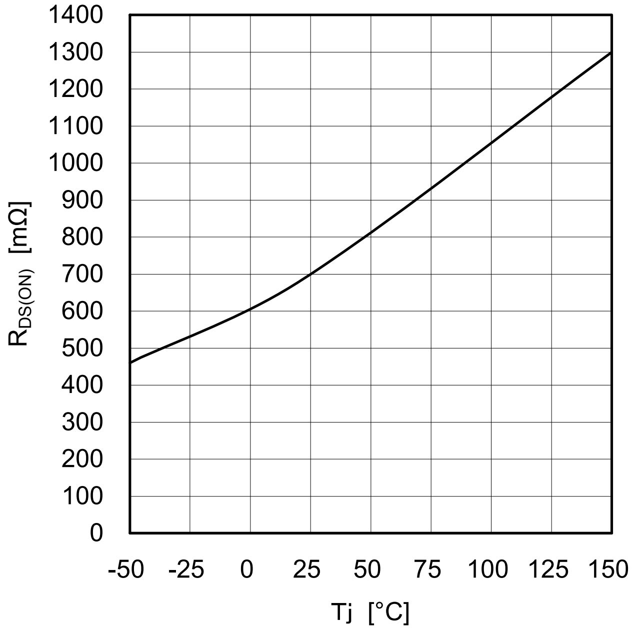


Figure 6. Output ON Resistance Characteristic
[Temperature Characteristic]

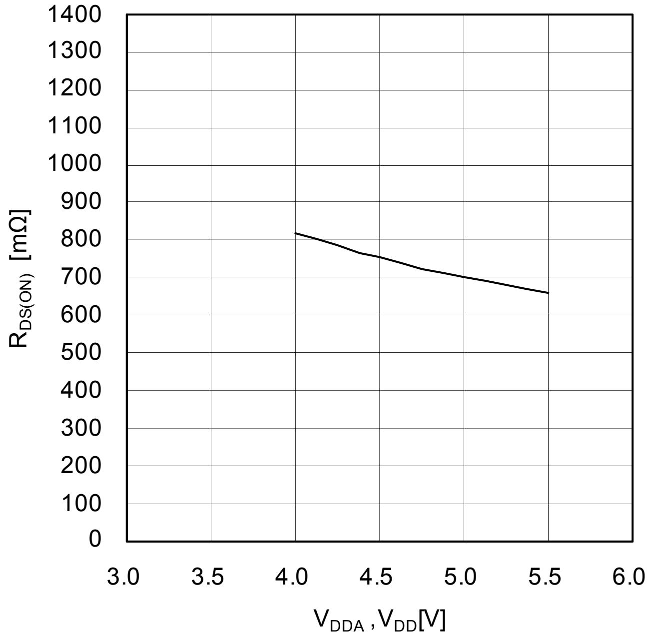


Figure 7. Output ON Resistance Characteristic
[Source Voltage Characteristic]

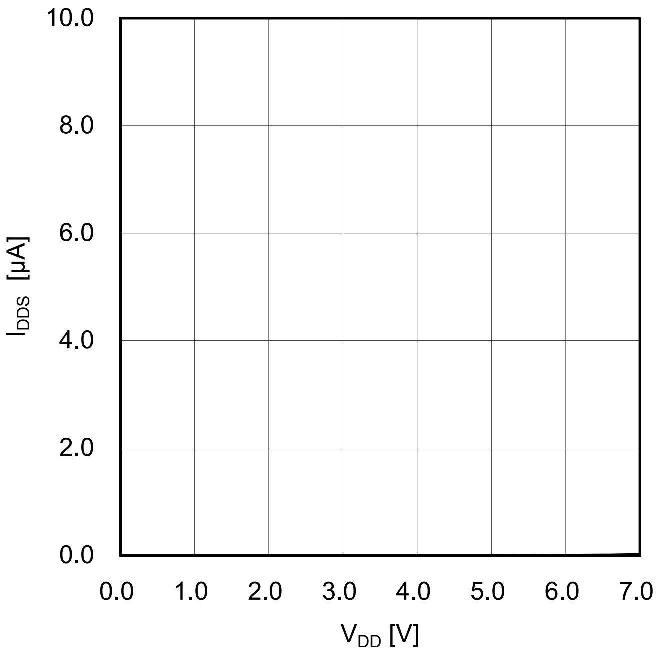


Figure 8. Standby Current Characteristic (VDD)

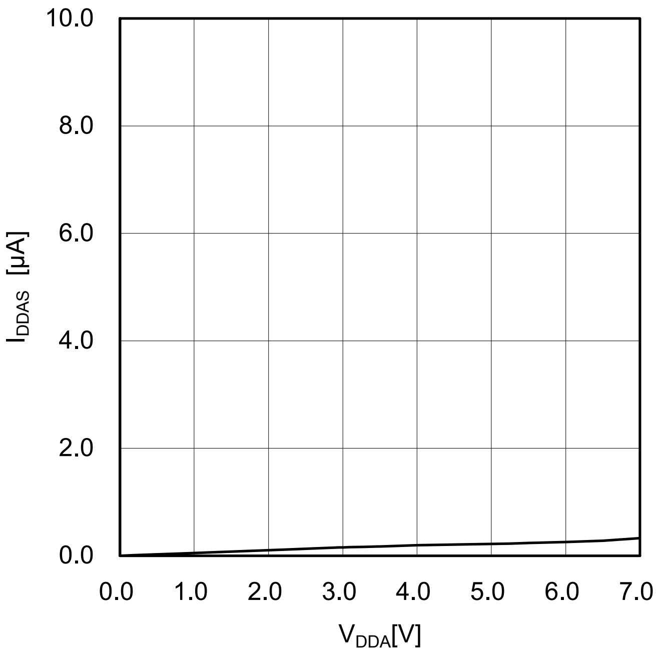


Figure 9. Standby Current Characteristic (VDDA)

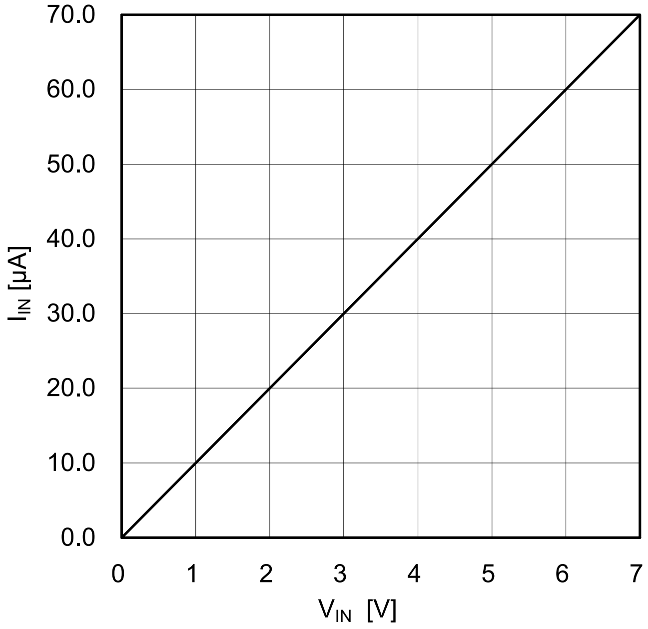


Figure 10. Input current Characteristic
(IN1~4, DIR, SCLK, SI, RST_B, CS_B(Note 1))

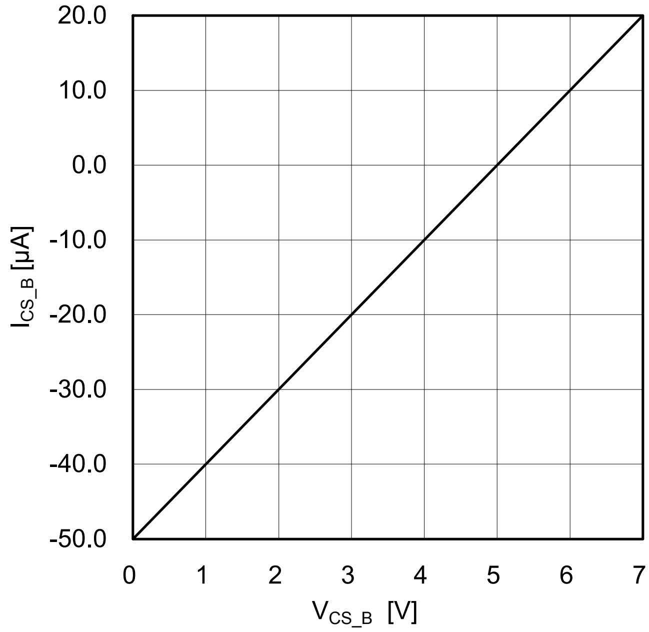


Figure 11. Input current Characteristic (CS_B)

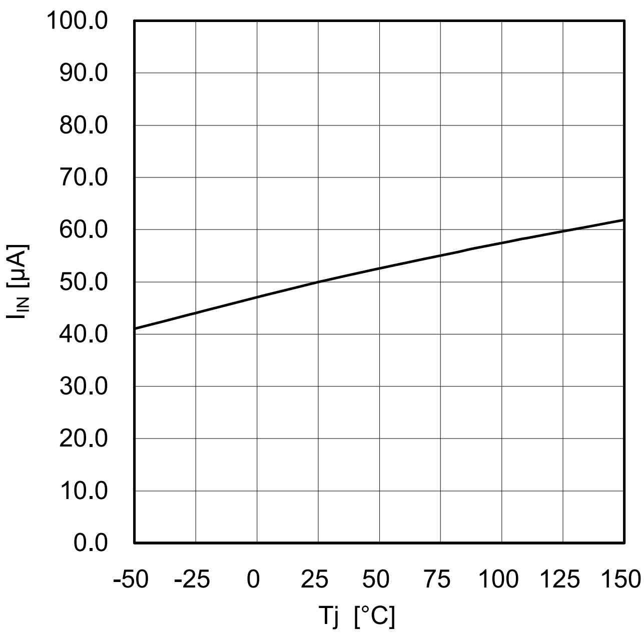


Figure 12. Input current Characteristic
［Temperature Characteristic］
($V_{IN1\ to\ 4}$, V_{SCLK}, V_{SI}, V_{CS_B}(Note 1), V_{RST_B}=5V)
(Note 1)DIRMode

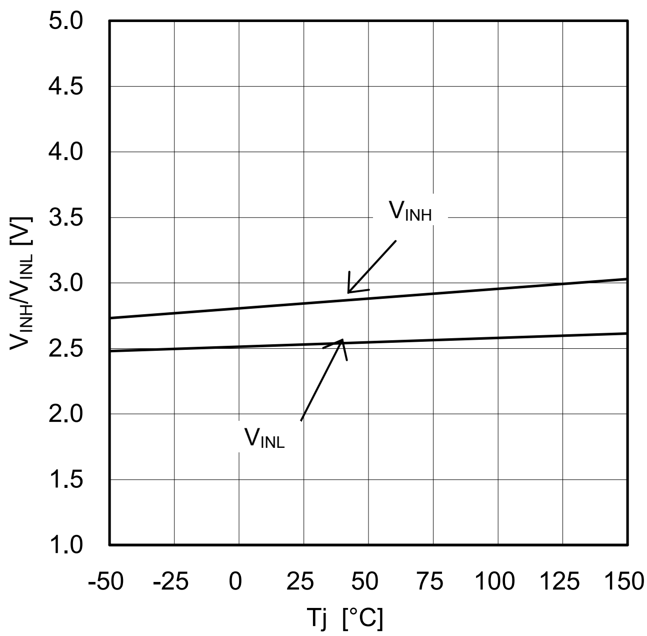


Figure 13. Input Voltage Threshold Characteristic
［Temperature Characteristic］

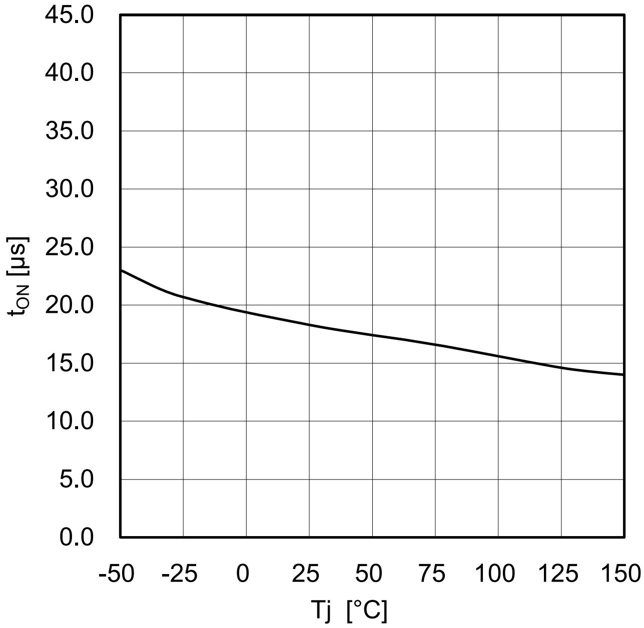


Figure 14. Switching Time (t_{ON})
[Temperature Characteristic]

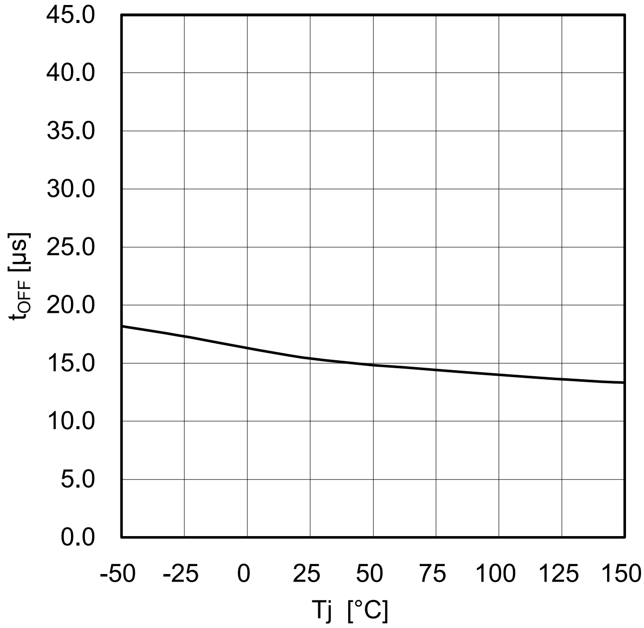


Figure 15. Switching Time (t_{OFF})
[Temperature Characteristic]

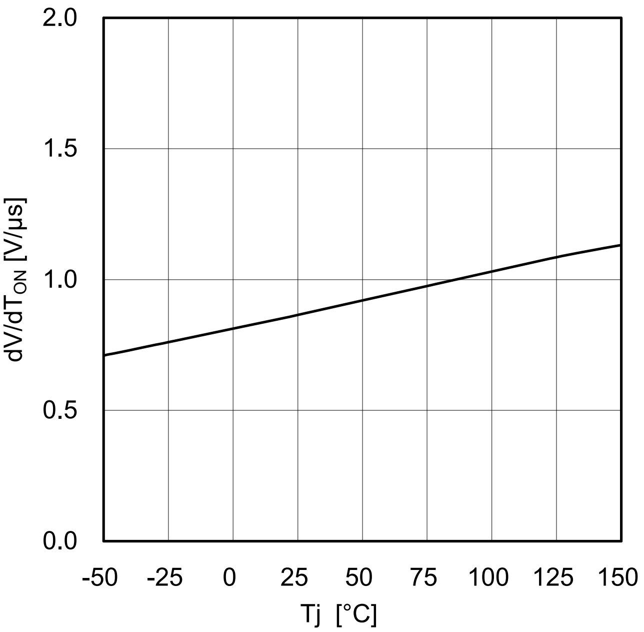


Figure 16. Slew Rate (at ON)
[Temperature Characteristic]

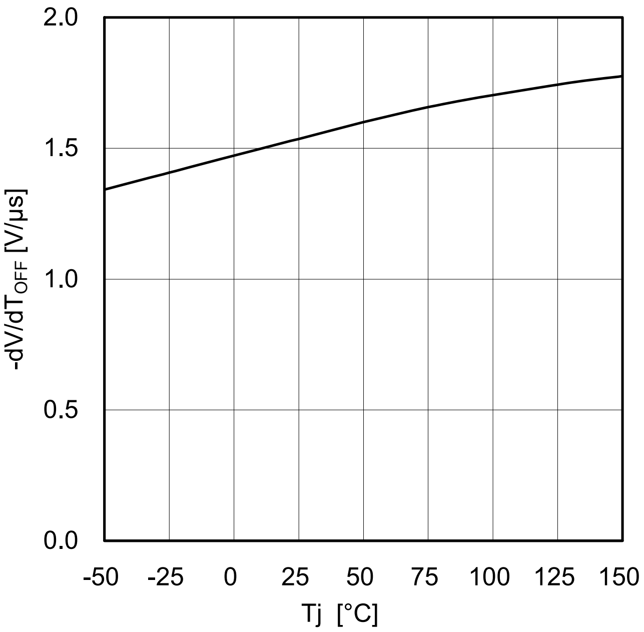


Figure 17. Slew Rate (at OFF)
[Temperature Characteristic]

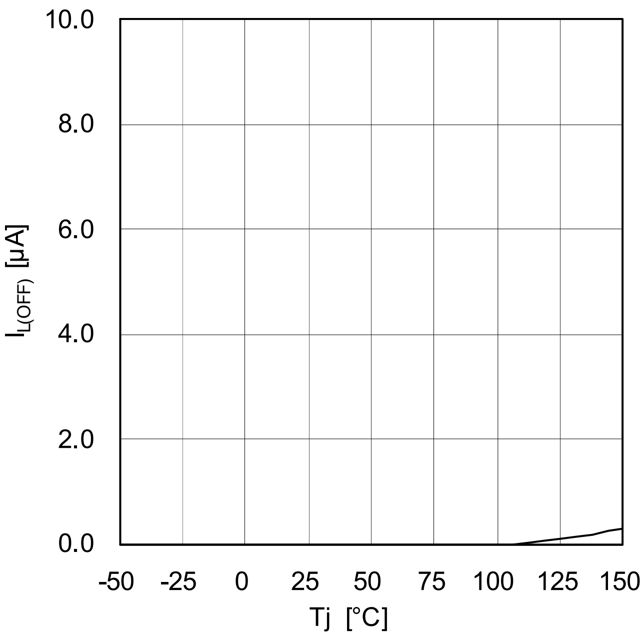


Figure 18. Output Leak Current
[Temperature Characteristic](V_{DS}=30V)

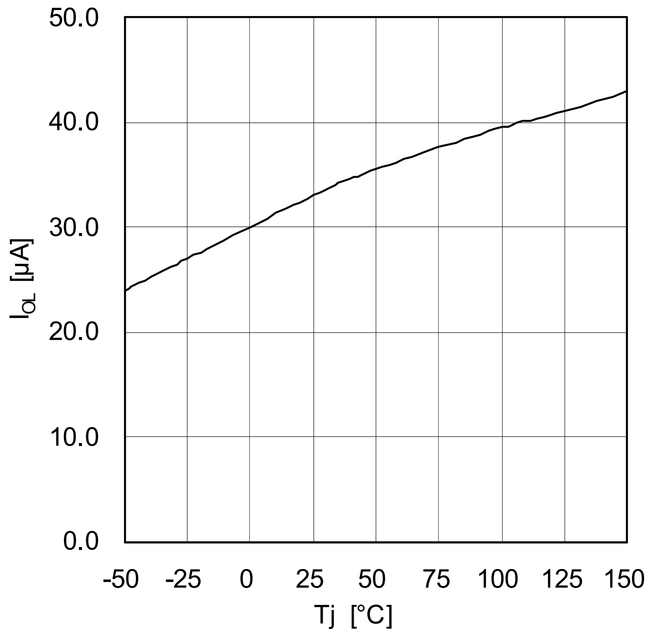


Figure 19. Output Leak Current (Open detect)
［Temperature Characteristic］(V_{DS} =40V)

Switching Time Measurement

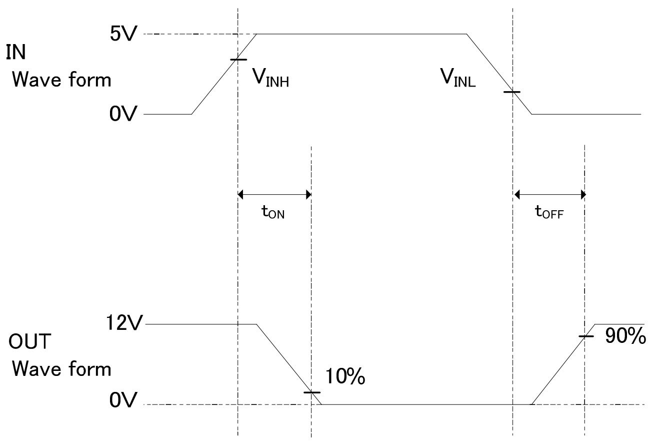


Figure 20. Switching Time

Timing Chart with Inductive Load

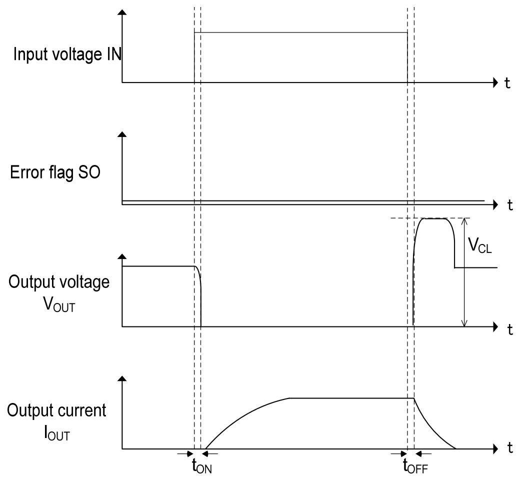
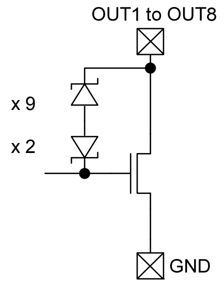
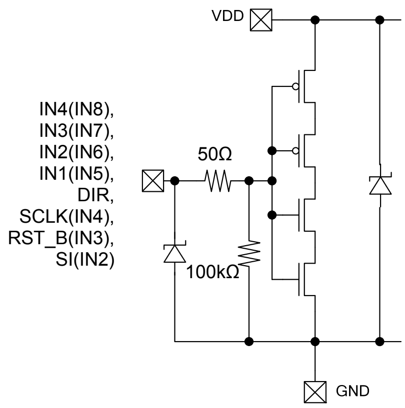
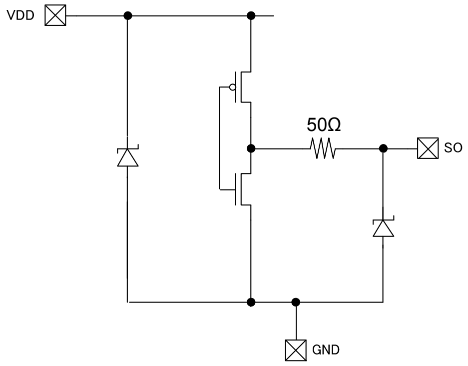
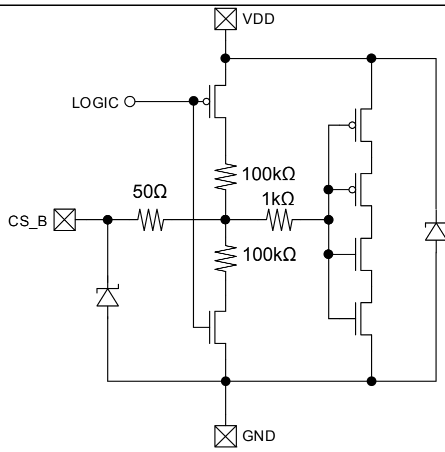


Figure 21. Timing Chart with inductive Load

I/O Equivalent Circuits

Pin	Symbol	I/O Equivalent Circuits
1,2, 11,12	GND	
3 to 10	OUT1 to OUT8	
13	VDD	
14 to 17 18 20 to 22	IN4(IN8), IN3(IN7), IN2(IN6), IN1(IN5), DIR, SCLK(IN4), RST_B(IN3), SI(IN2)	
19	SO	
23	CS_B	
24	VDDA	

SPI mode

When CS_B=H,

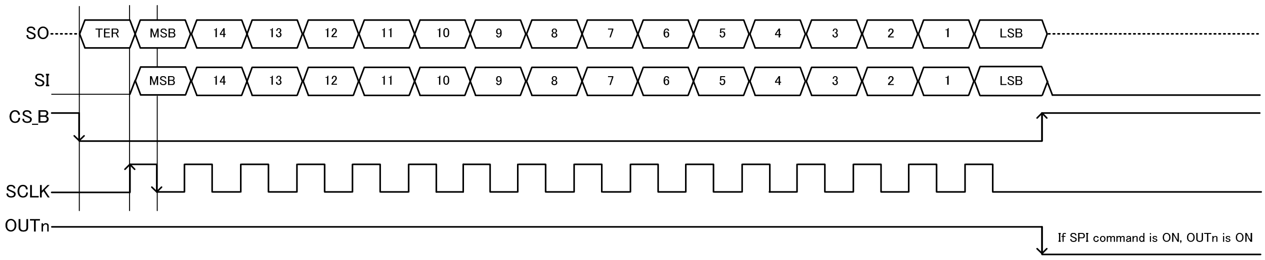
SO Terminal become Hi-Z

When CS_B=L,

Internal state (TSD, OCP, OLD) is latched at falling edge of CS_B, and output to SO at rising edge of SCLK.

SI is taken in register at falling edge of SCLK.

Output corresponding to each resister input is controlled at rising edge of CS_B.



Definitions of SI and SO signals are shown below.

SI signals

Initial:0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH8		CH7		CH6		CH5		CH4		CH3		CH2		CH1	

Bits	CHn	States of output and protective circuits			
		Output	OCP	TSD	OLD
15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0	00	OFF	disable	disable	disable
	01	ON/OFF (Note 1)	enable/disable	enable/disable	disable/enable
	10	ON	enable	enable	disable
	11	OFF	disable	disable	enable

(Note 1) When INn=01, output is controlled by IN terminal.

Output controlled by each input is shown below.

Input	Controlled output
IN1(IN5)	OUT1
IN2(IN6)	OUT2
IN3(IN7)	OUT3
IN4(IN8)	OUT4
IN1(IN5)	OUT5
IN2(IN6)	OUT6
IN3(IN7)	OUT7
IN4(IN8)	OUT8

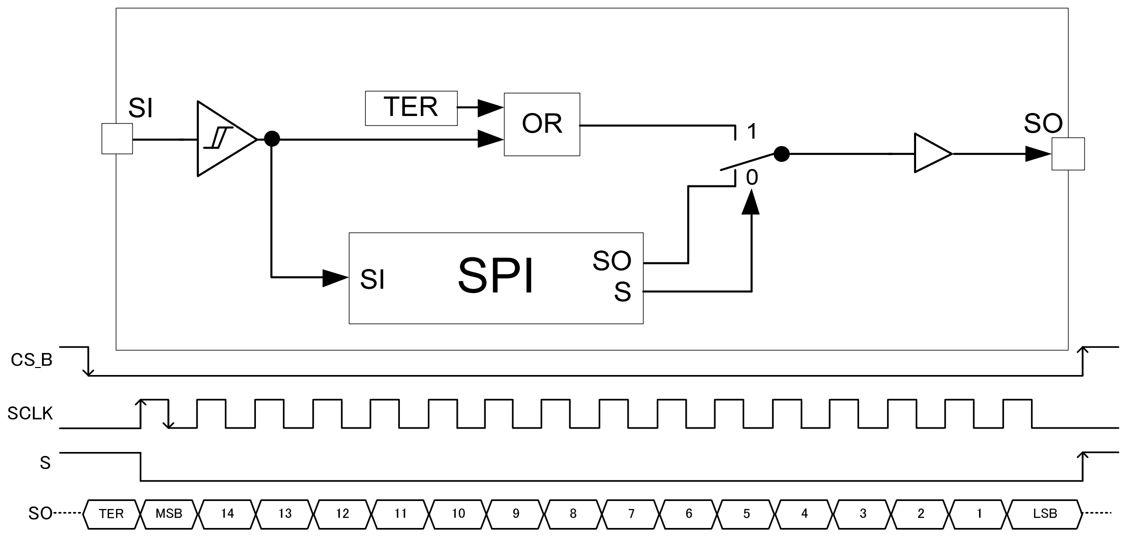
SO signals

When CS_B=H,
SO Terminal become Hi-Z
When CS_B=L,
Explanation of each Bit is shown below.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TER	OL8	D8	OL7	D7	OL6	D6	OL5	D5	OL4	D4	OL3	D3	OL2	D2	OL1	D1
	OUT8		OUT7		OUT6		OUT5		OUT4		OUT3		OUT2		OUT1	

Field	Bits	Data	STATE
TER	16(Note 1)	0	Correspondence just after reset and normal operation
		1	Correspondence error of last time
OLn (n = 8 to1)	15,13,11 9,7,5 3,1	0	Normal operation
		1	Load open
Dn (n = 8 to1)	14,12 10,8,6 4,2,0	0	Normal operation
		1	OCD or TSD

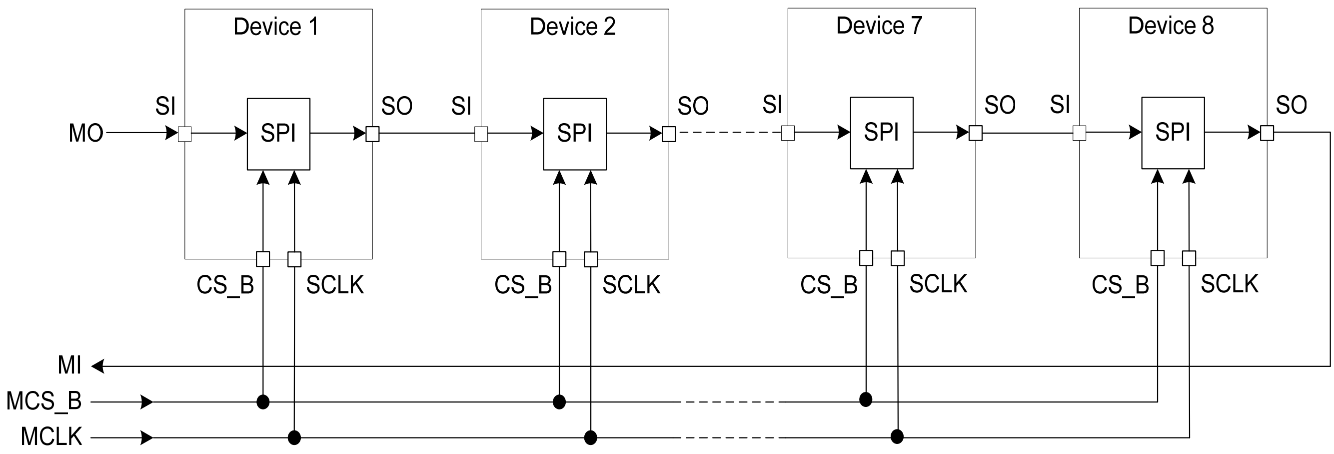
(Note 1) TER bit outputs logical sums of TER signal and input signal of this device with SI signal in the interval from fall of CS_B to rise of SCLK as shown below.
Block diagram and timing chart are shown below.



In order to select whether TER signal is output or SPI data output (OLn, Dn) signal is output, “S” signal is generated within IC and output is switched.

Seroal Daisy Chain

Plurality of devices can be connected as shown in the diagram below.
CS_B signal and SCLK signal connect common signal.
SI/SO line can connect SO of Device 1 to SI of Device 2 as shown in the diagram below.



Timing chart when 8 devices are connected is shown below.

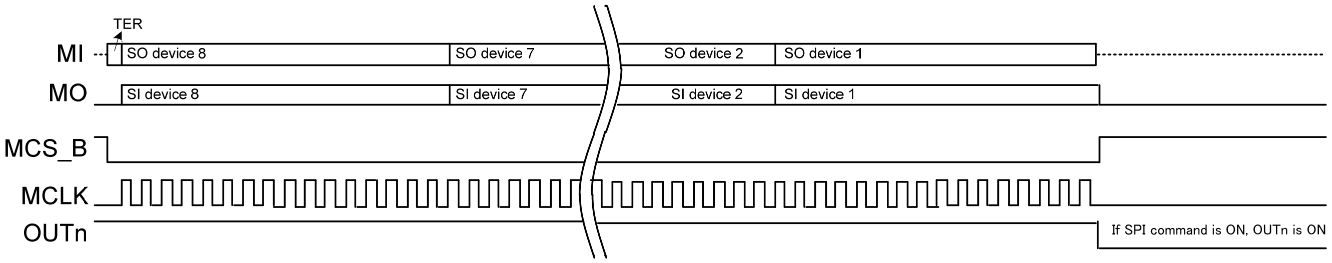
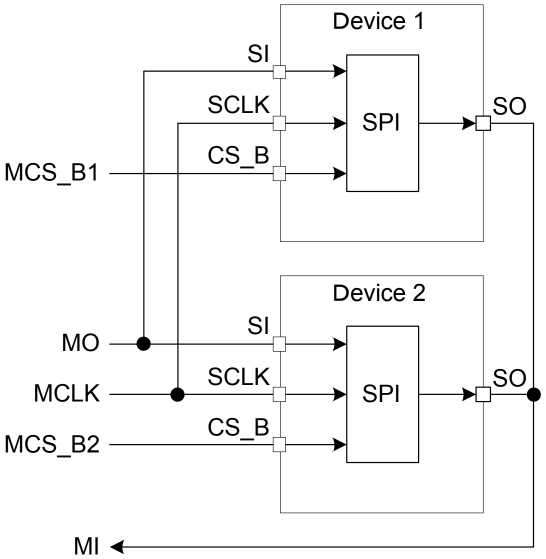


Figure 22. Timing chart when 8 devices are connected

Parallel Connection

Plurality of devices can be connected to parallel as shown in the diagram below.
SI signal, SCLK signal and SO signal connect common signal.
Each signal is necessary every each device for the CS_B signal.



Timing chart when 2 devices are connected is shown below.

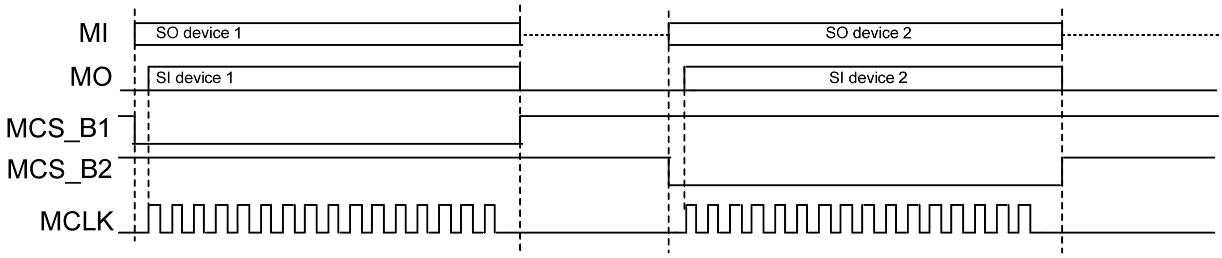


Figure 23. Timing chart when 2 devices are connected

SPI RST_B releasing sequence

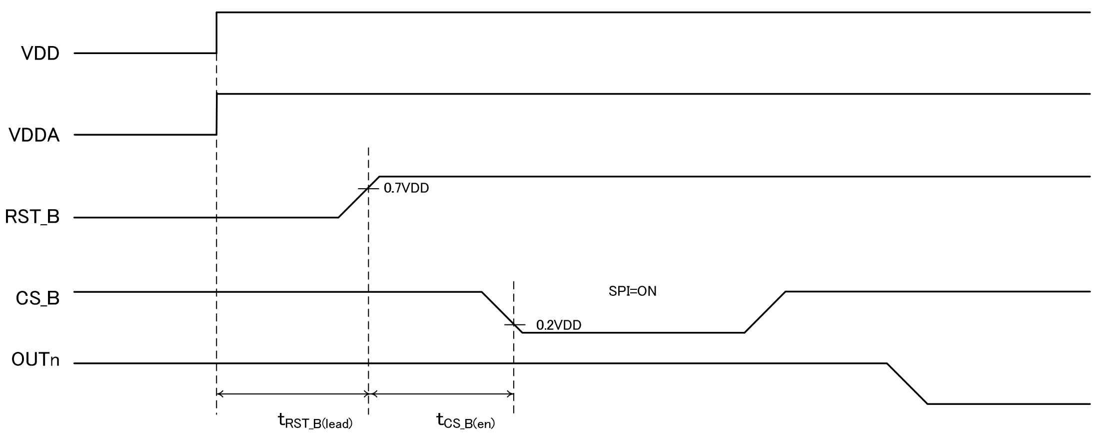


Figure 24. RST_B Releasing Sequence

Item	Symbol	Min	Typ	Max	Unit
RST_B lead time(Note 1) (Note 2)	t_{RST_B} (lead)	1	-	-	ms
CS_B enable time(Note 1)	t_{CS_B} (en)	10	-	-	µs

(Note 1) Not 100% tested

(Note 2) RST_B L time and H time must be over 10µs

SPI timing chart

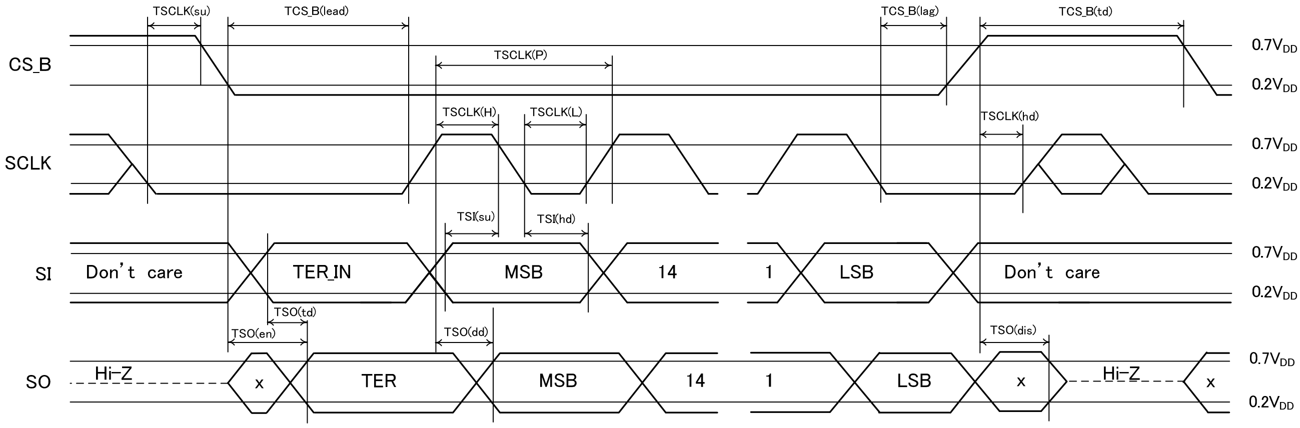


Figure 25. SPI Timing Chart

Item	Symbol	Min	Typ	Max	Unit
SCLK frequency	fSCLK	0	―	5	MHz
SCLK cycle length	TSCLK(P)	200	―	―	ns
SCLK high time	TSCLK(H)	50	―	―	ns
SCLK low time	TSCLK(L)	50	―	―	ns
SCLK setup time	TSCLK(su)	50	―	―	ns
SCLK hold time	TSCLK(hd)	50	―	―	ns
CS_B lead time	TCS_B(lead)	250	―	―	ns
CS_B lag time	TCS_B(lag)	250	―	―	ns
Transfer delay time	TCS_B(td)	250	―	―	ns
Data setup time	TSI(su)	20	―	―	ns
Data hold time	TSI(hd)	20	―	―	ns
SPI Output enable time(Note 1)	TSO(en)	―	―	200	ns
SPI Output disable time(Note 1)	TSO(dis)	―	―	250	ns
SPI Output Data delay time(Note 1), (Note 2)	TSO(dd)	―	―	100	ns
ERR Output Through delay time (Note 1)	TSO(td)	―	―	200	ns

(Note 1) Not 100% tested.
(Note 2) When SO terminal capacity=10pF, 3.0V ≤ V_{DD} ≤ 5.5V. Refer to Figure 25 and Figure 26.

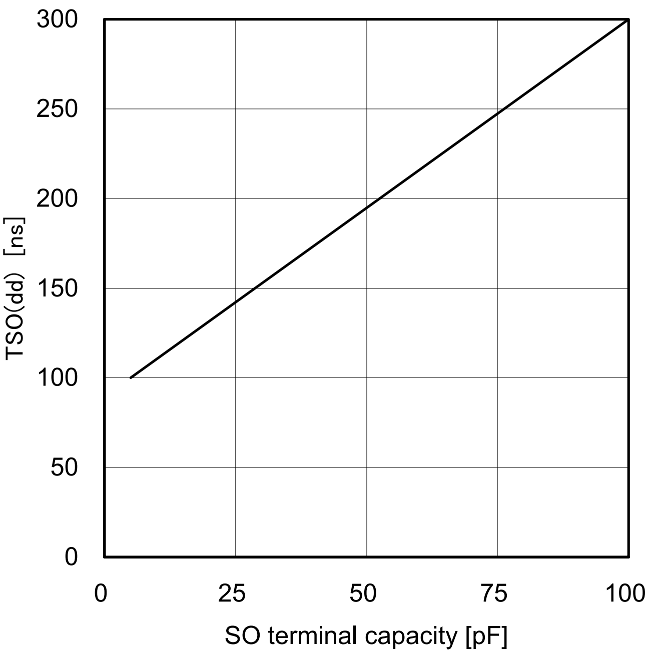


Figure 26. Max of SPI Output Data delay time
(3.0V ≤ V_{DD} < 4.5V)

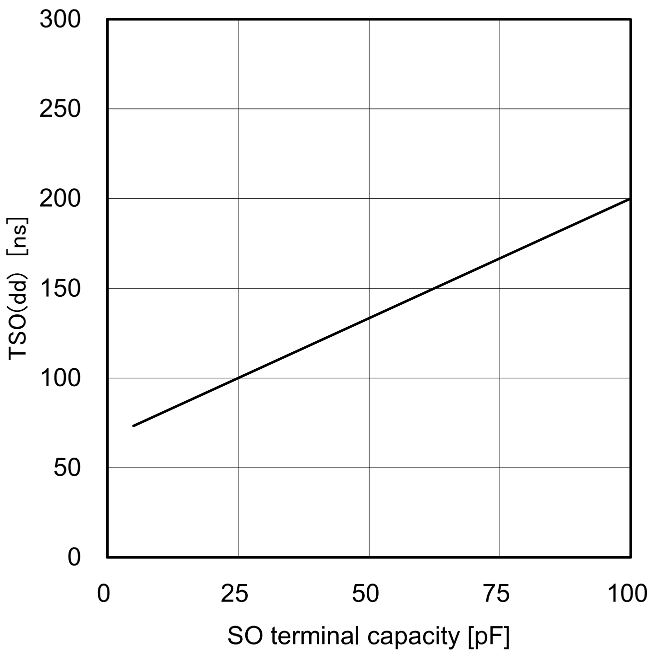


Figure 27. Max of SPI Output Data delay time
(4.5V ≤ V_{DD} ≤ 5.5V)

DIR (direct) mode

Transition to direct mode is brought about by switching DIR terminal to High.
Output controlled for each input is shown below.
Further, SPI input and RST_B input are not accepted during direct mode.

Input Pin	Controlled Output
CS_B(IN1)	OUT1
SI(IN2)	OUT2
RST_B(IN3)	OUT3
SCLK(IN4)	OUT4
IN1(IN5)	OUT5
IN2(IN6)	OUT6
IN3(IN7)	OUT7
IN4(IN8)	OUT8

DIR (direct) mode timing chart (1)

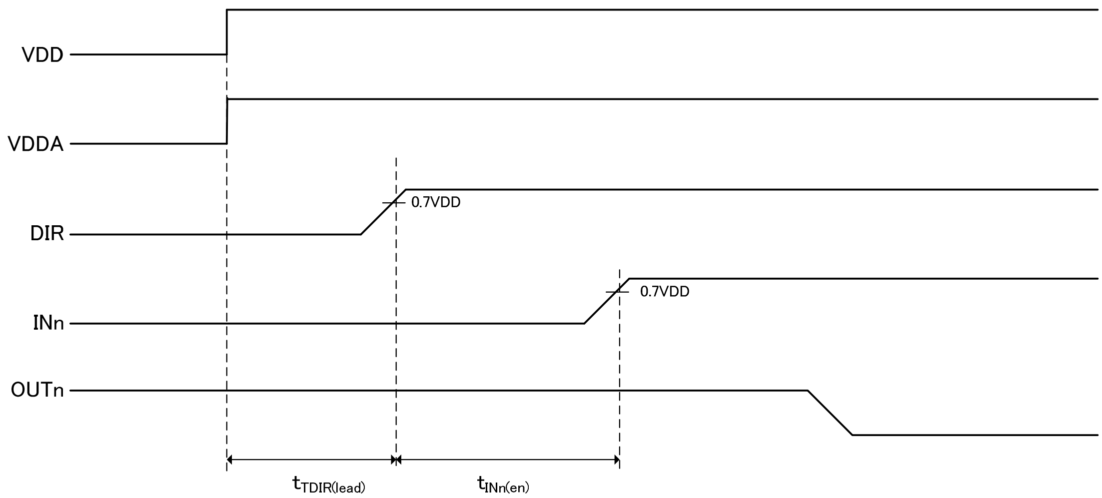


Figure 28. DIR Mode Timing Chart (1)

Item	Symbol	Min	Typ	Max	Unit
DIR lead time(Note 1)	$t_{DIR(lead)}$	1	-	-	ms
INn enable time(Note 1)	$t_{INn\ (en)}$	10	-	-	μs

(Note 1) Not 100% tested.

DIR (direct) mode timing chart (2)

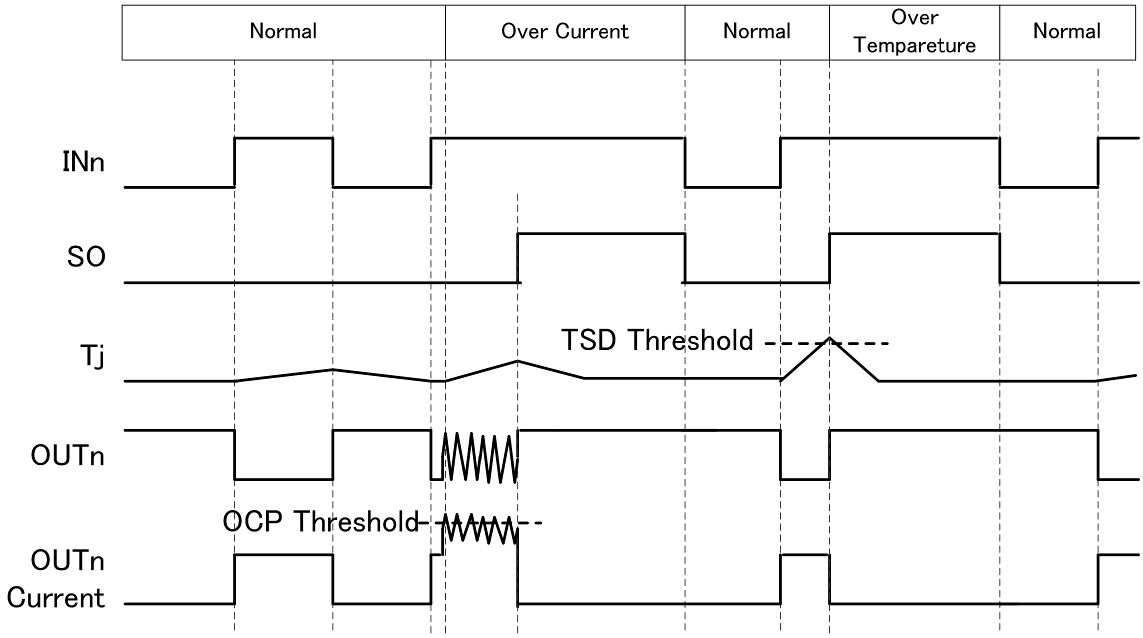


Figure 29. DIR Mode Timing Chart (2)

Direct mode operation current (I_{DDA} + I_{DD}) state transition

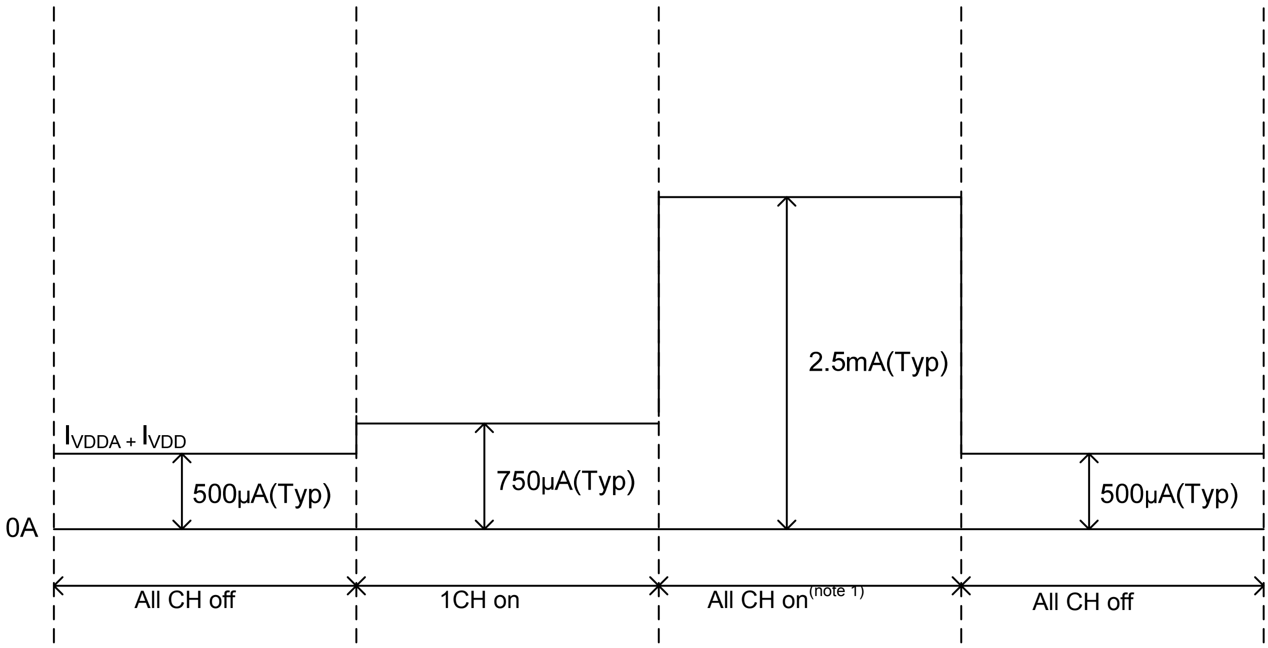
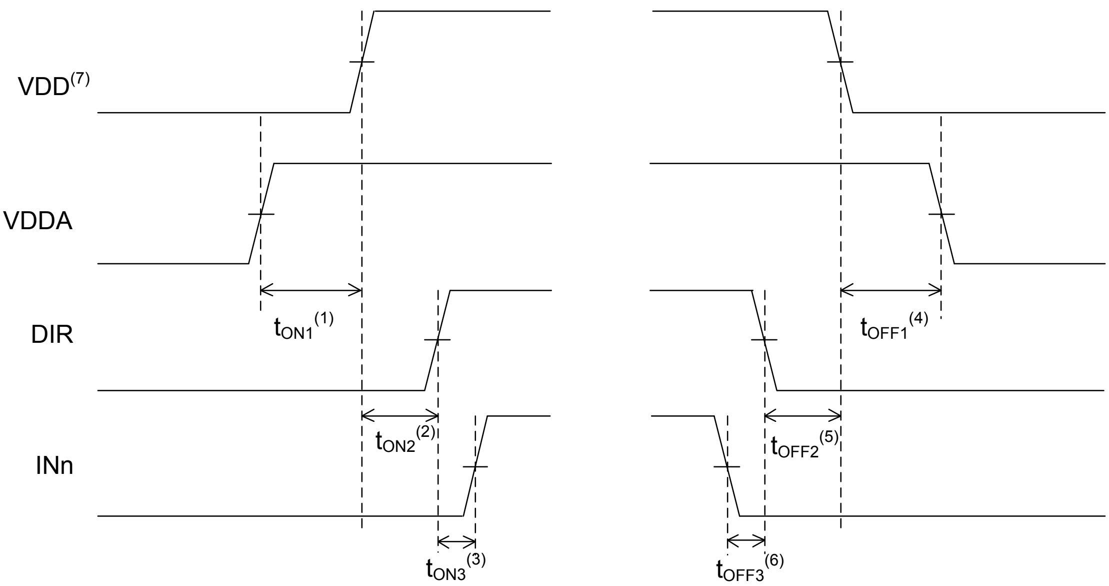


Figure 30. Operation Current State Transition Diagram

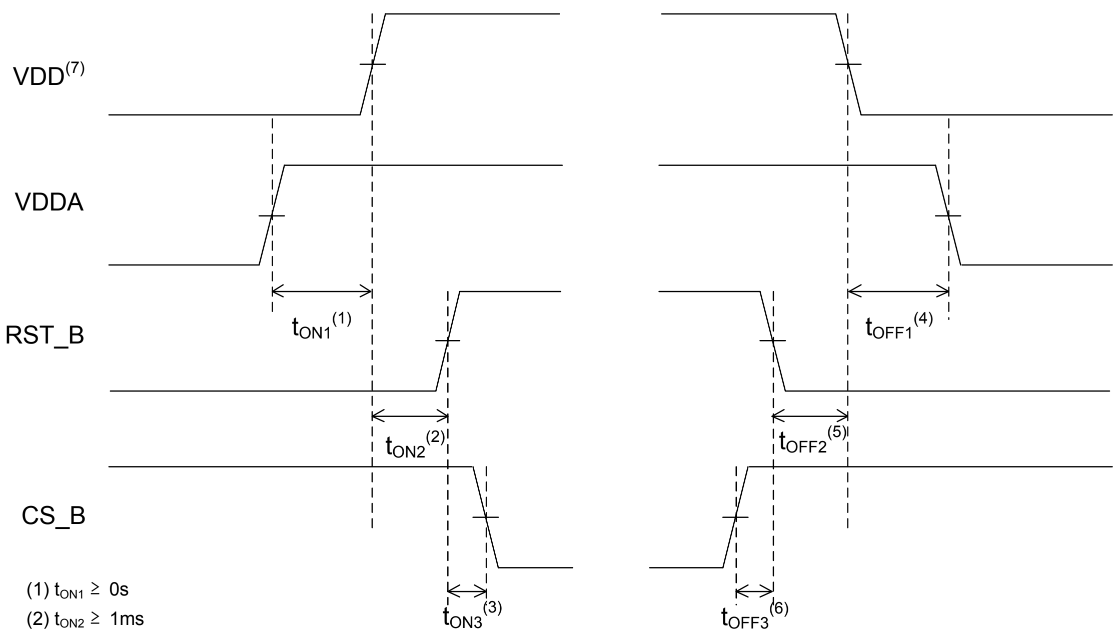
(Note 1) Sum of P.4 VDDA operation current (when all outputs are on) and VDD operation current (when all outputs are on).

Power source ON/OFF sequence



(1) $t_{ON1} \geq$ 0s
(2) $t_{ON2} \geq$ 1ms
(3) $t_{ON3} \geq$ 10us
(4) $t_{OFF1} \geq$ 0s
(5) $t_{OFF2} \geq$ 0s
(6) $t_{OFF3} \geq$ 0s
(7) $V_{DD} < V_{DDA}$+0.3V

Figure 31. Power Source ON/OFF Sequence



(1) $t_{ON1} \geq$ 0s
(2) $t_{ON2} \geq$ 1ms
(3) $t_{ON3} \geq$ 10us
(4) $t_{OFF1} \geq$ 0s
(5) $t_{OFF2} \geq$ 0s
(6) $t_{OFF3} \geq$ 0s
(7) $V_{DD} < V_{DDA}$+0.3V

Figure 32. Power Source ON/OFF Sequence（SPI MODE）

Detection functions

① Overcurrent protection

When current of no less than 1.2A (Typ) is flown in output transistor of from OUT1 to OUT8 in 1000μs (Typ), the error flag is output. The error flag is released by OUTENn(Note 1) becoming L(Note 2).

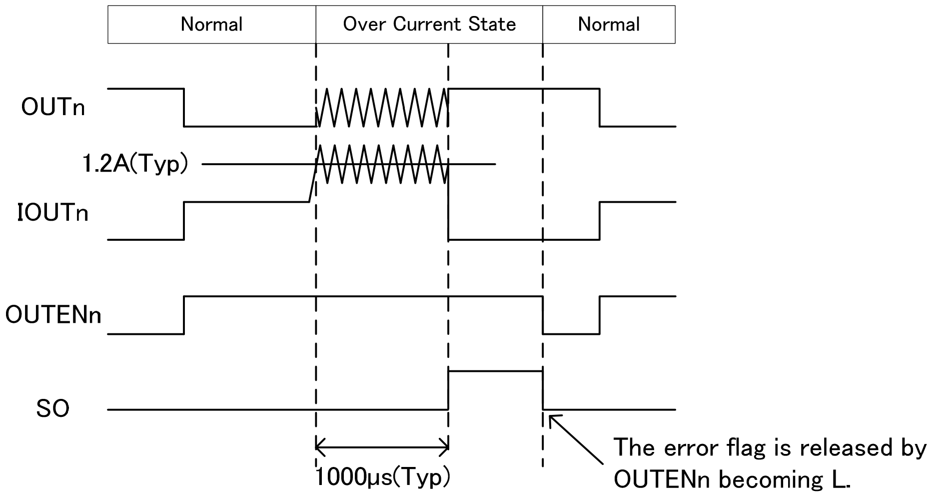


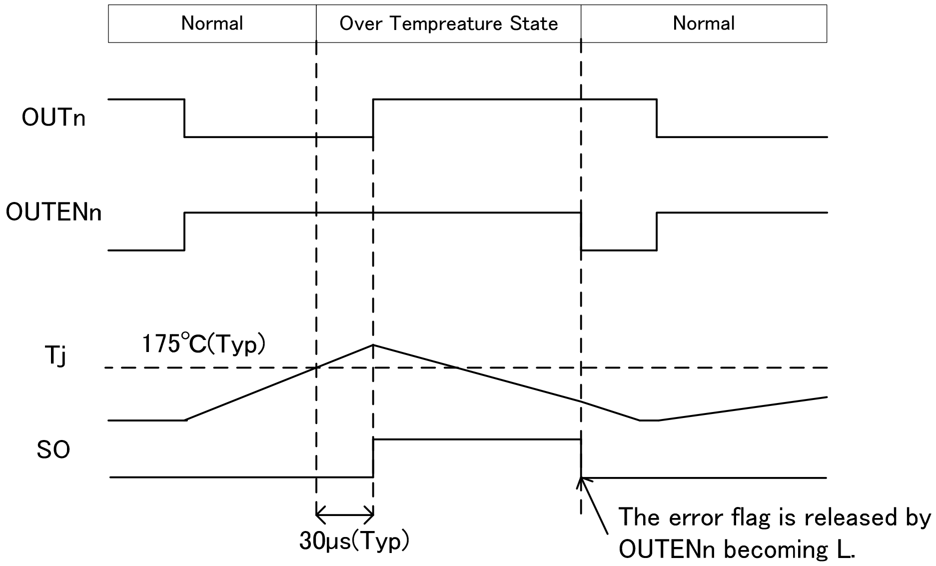
Figure 33. Overcurrent Protection Timing Chart

(Note 1) OUTENn shows the ON/OFF control signal of the OUT terminals." n" shows the channel number.

(Note 2) The over current detection latch timer is cleared, and the error flag is not output when OUTENn become L before Over current detection time(Typ:1000μs Max: 2200μs).

② Overheat protection

When Tj of from OUT1 to OUT8 reaches 175°C (Typ) or above and it passes for 30µs(Typ), output is turned off. The error flag is released by OUTENn(Note 1) becoming L(Note 2).

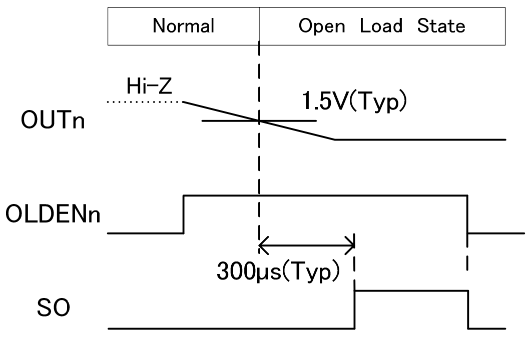


(Note 1) OUTENn shows the ON/OFF control signal of the OUT terminals. n shows the channel number.
(Note 2) The overheat detection latch timer is cleared, and the error flag is not output when OUTENn become L before Overheat detection time(Typ:30µs Max: 65µs).

Figure 34. Overheat Protection Timing Chart

③ Open detection

In case of enable at Open detection function(Note 3), when output voltage of from OUT1 to OUT8 falls below 1.5 V (Typ), open detection is detected and the error flag is output.



(Note 3) As for the DIR mode, OLDENn=H(open detection function becomes effective) in OUTENn =L.
40uA (Typ) is flown from OUT to GND because 60kΩ(Typ) is connected between OUT and GND.
As for the SPI mode, Please refer to Page 13.
"n" shows the channel number.

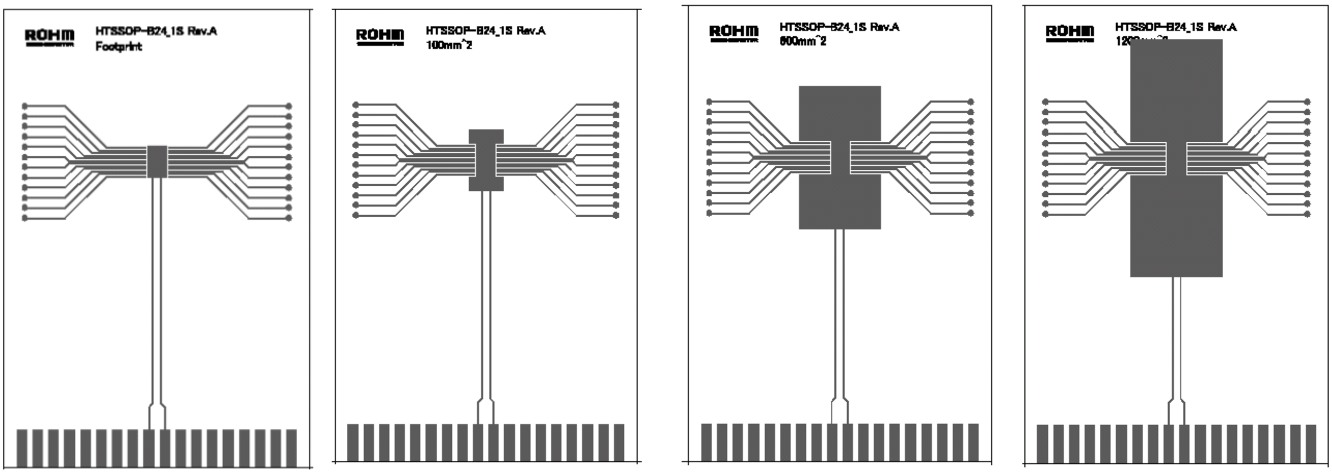
Figure 35. Open Detection Protection Timing Chart

Thermal resistance (Note 1)

Item	Symbol	Typ	Unit	Condition
HTSSOP-B24				
Junction-Ambient thermal resistance	θ_{JA}	42	°C / W	1s (Note 2)
		30	°C / W	2s (Note 3)
		23	°C / W	2s2p (Note 4)
Junction-Package upper side (Note5) thermal characteristic parameter	Ψ_{JT}	4	°C / W	1s (Note 2)

(Note 1) Based on JESD51 - 2A (Still-Air), in case of 8ch ON state
(Note 2) Based on JESD51 - 3 FR4 114.3 mm x 76.2 mm x 1.57 mm 1 layer (1s)
(TOP Cupper layer : ROHM original land pattern + wiring for measurement, copper thickness 2oz, copper area 600mm^2)
(Note 3) Based on JESD51 -5 FR4 114.3 mm x 76.2 mm x 1.60 mm 2 layer(2s)
(TOP Cupper layer : ROHM original land pattern + wiring for measurement, Bottom Cupper area : 74.2 mm x 74.2 mm, Cupper thickness (Top and Bottom layers) 2oz)
(Note 4) Based on JESD51 -5 / -7 FR4 114.3 mm x 76.2 mm x 1.60 mm 4 layers (2s2p)
(TOP Cupper layer : ROHM original land pattern + wiring for measurement / 2nd, 3rd, Bottom layer Cupper area : 74.2 mm x 74.2 mm, Cupper thickness(Top and Bottom layers / Internal layers) 2oz / 1oz)
(Note 5) T_T : The central temperature on the surface of molding is measured.

① PCB Layout 1s

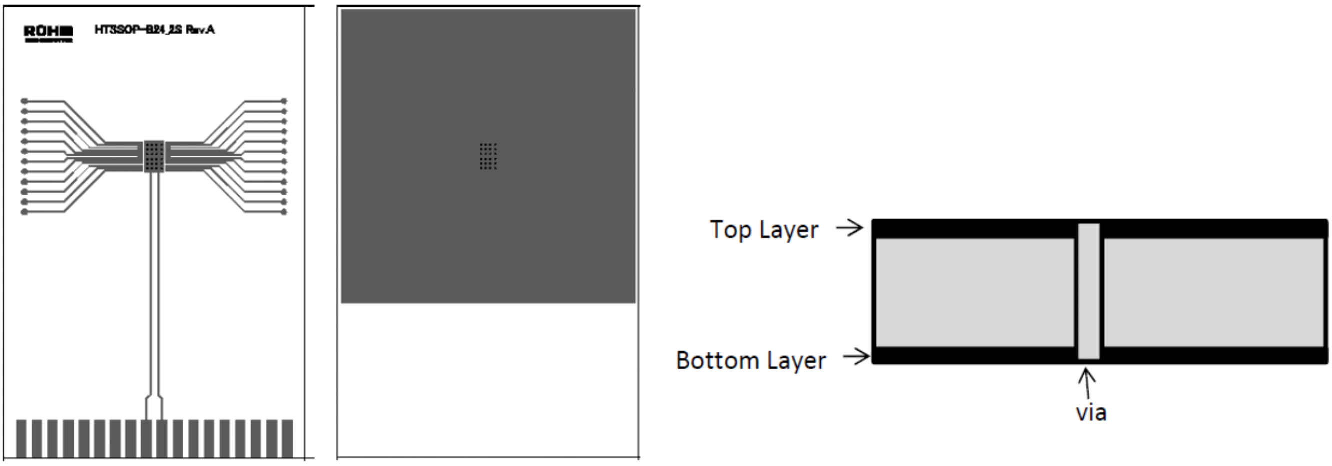


Footprint 100mm^2 600mm^2 1200mm^2

Figure 36. PCB Layout 1s

Dimension	Value
Board finish thickness	1.57 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu:2oz)
Heatsink copper area dimension	Footprint / 100mm^2 / 600mm^2 / 1200mm^2

② PCB Layout 2s

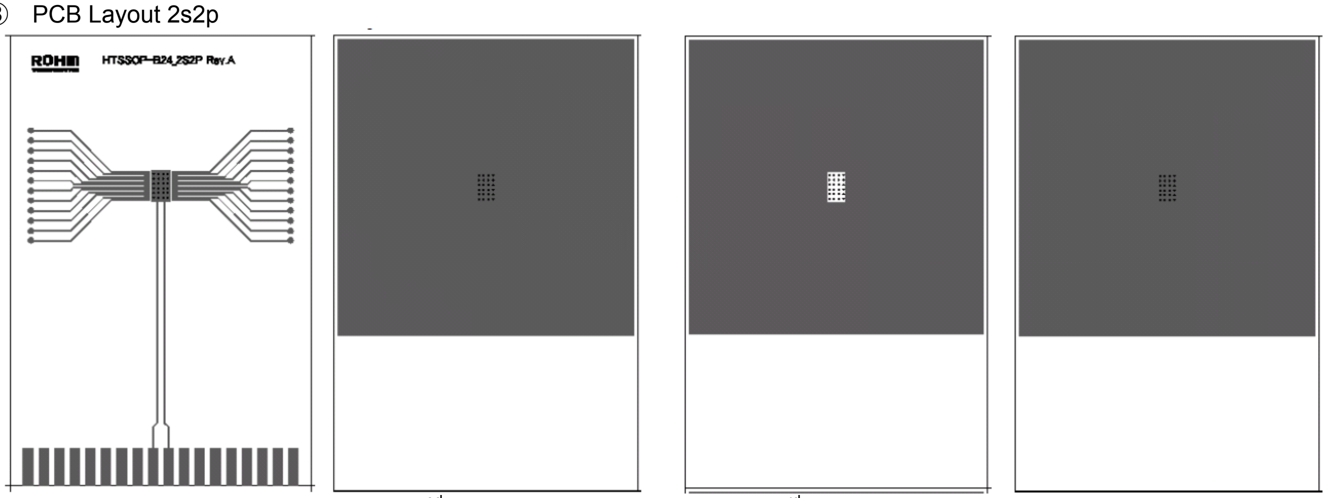


Top Layer Bottom Layer Cross section

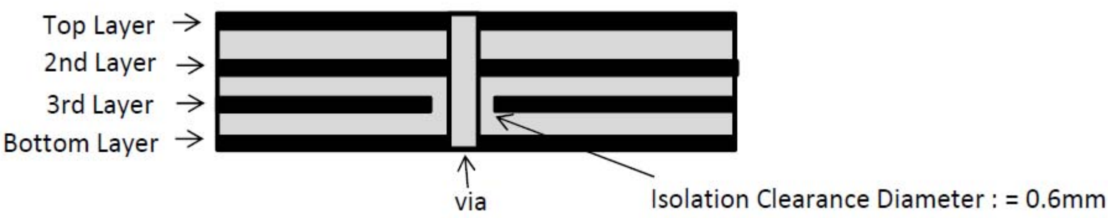
Figure 37. PCB Layout 2s

Dimension	Value
Board finish thickness	1.60 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu + Plating)
Therml vias separation / diameter	1.2mm / 0.3mm

③ PCB Layout 2s2p



TOP Layer 2nd Layer 3rd Layer Bottom Layer



Cross section

Figure 38. PCB Layout 2s2p

Dimension	Value
Board finish thickness	1.60 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu + Plating)
Copper thickness (Inner layers)	0.035mm
Therml vias separation / diameter	1.2mm / 0.3mm

④ Thermal impedance (Single pulse)

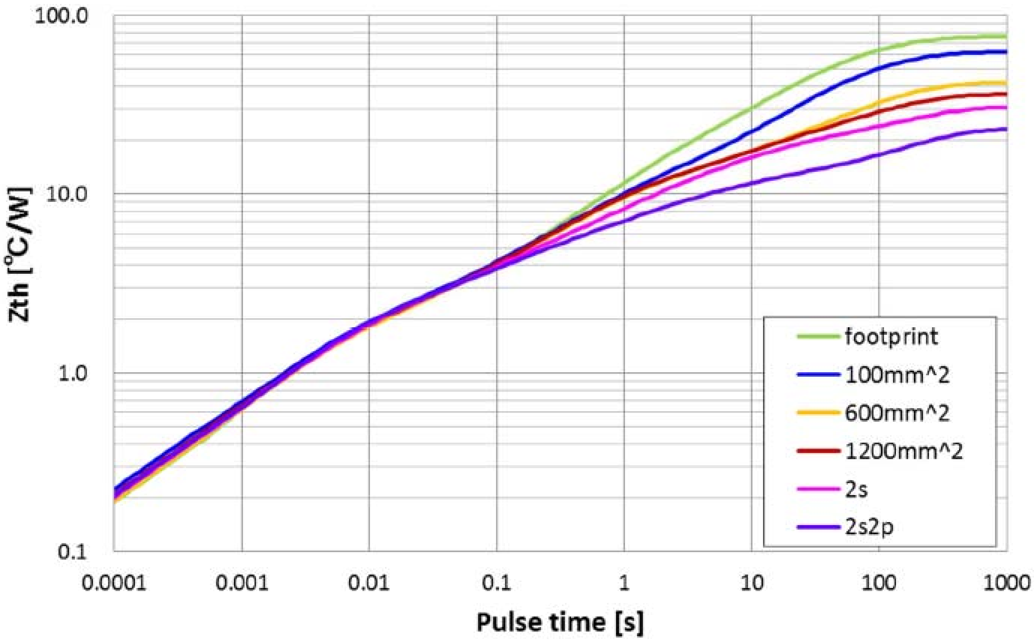


Figure 39. Thermal impedance

⑤ Thermal resistance (θ JA / Ψ JT vs PCB copper area - 1s)

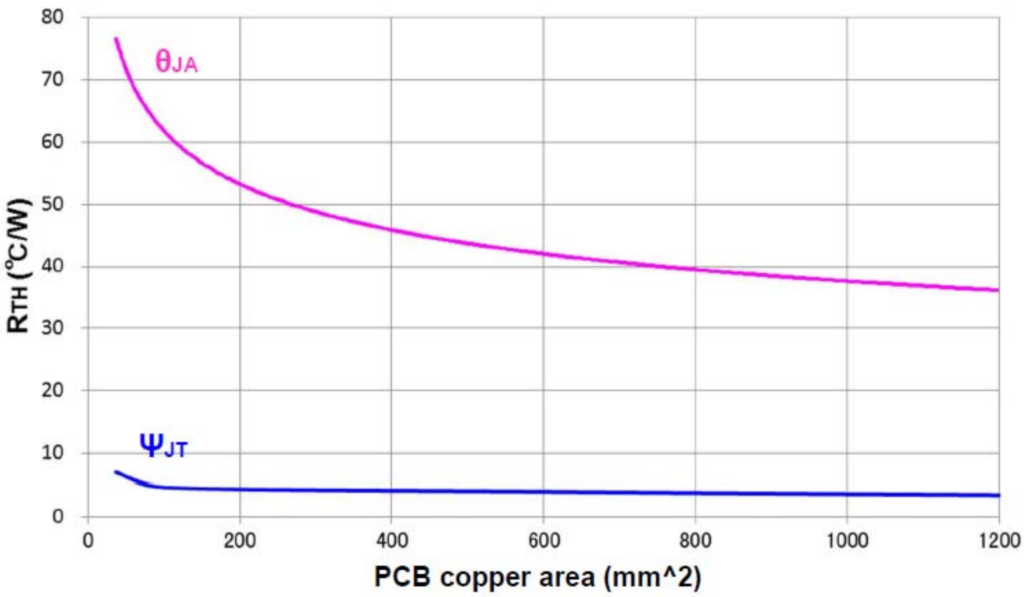


Figure 40. Thermal resistance

Operational Notes

1) Absolute Maximum Ratings
Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes or open circuit modes. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is expected to be operated in a special mode exceeding the absolute maximum ratings.

2) Reverse connection of power supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

3) Power supply lines
Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

4) GND Voltage
The voltage of GND pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

5) Thermal consideration
Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions. Consider Pc that does not exceed Pd in actual operating conditions (Pc≥Pd).

6) Short between pins and mounting errors
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

7) Operation Under Strong Electromagnetic Field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8) Thermal shutdown circuit (TSD)
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches 175°C (25°C hysteresis). It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

9) Over voltage protection (active clamp)
There is a built-in over voltage protection circuit (active clamp) to absorb the induced current when inductive load is off (Power MOS = off). During active clamp and when IN=0V, TSD will not function so keep IC temperature below 150°C.

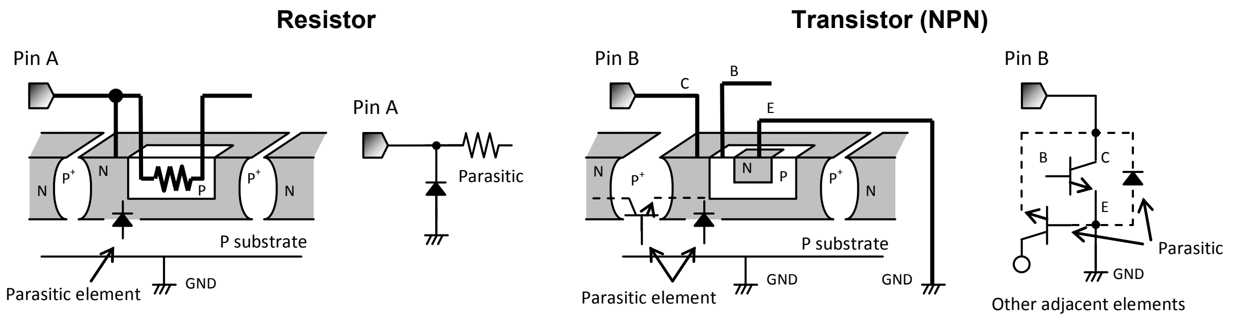
10) Over current protection circuit (OCP)
The IC incorporates an over-current protection circuit that operates in accordance with the rated output capacity. This circuit protects the IC from damage when the load becomes shorted. It is also designed to limit the output current (without latching) in the event of more than 1.2A (typ) flow, such as from a large capacitor or other component connected to the output pin. This protection circuit is effective in preventing damage to the IC in cases of sudden and unexpected current surges. The IC should not be used in applications where the over current protection circuit will be activated continuously.

11) Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

12) Regarding input pins of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

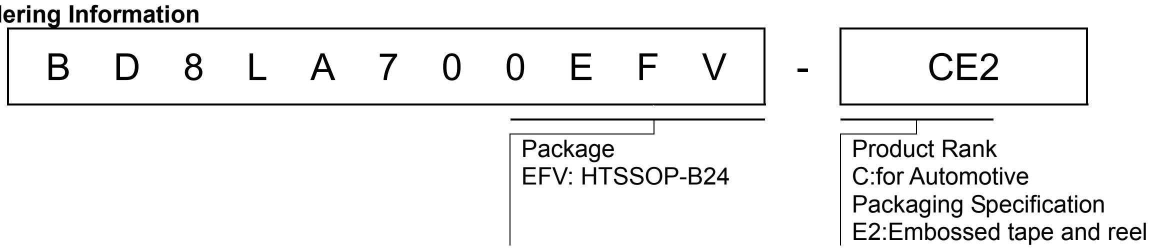


Example of monolithic IC structure

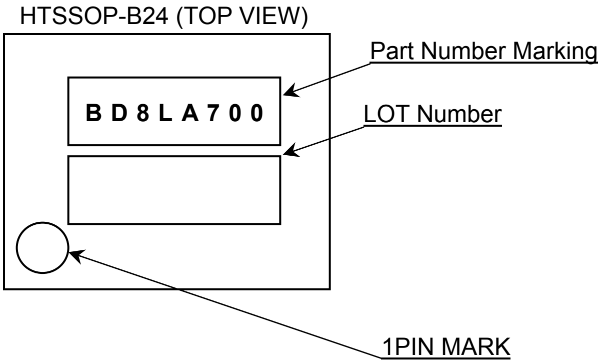
13) GND wiring pattern
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

14) Back electromotive force (BEMF)
There is a possibility that the BEMF is changed by using the operating condition, environment and the individual characteristics of motor. Please make sure there is no problem when operating the IC even though the BEMF is changed.

Ordering Information

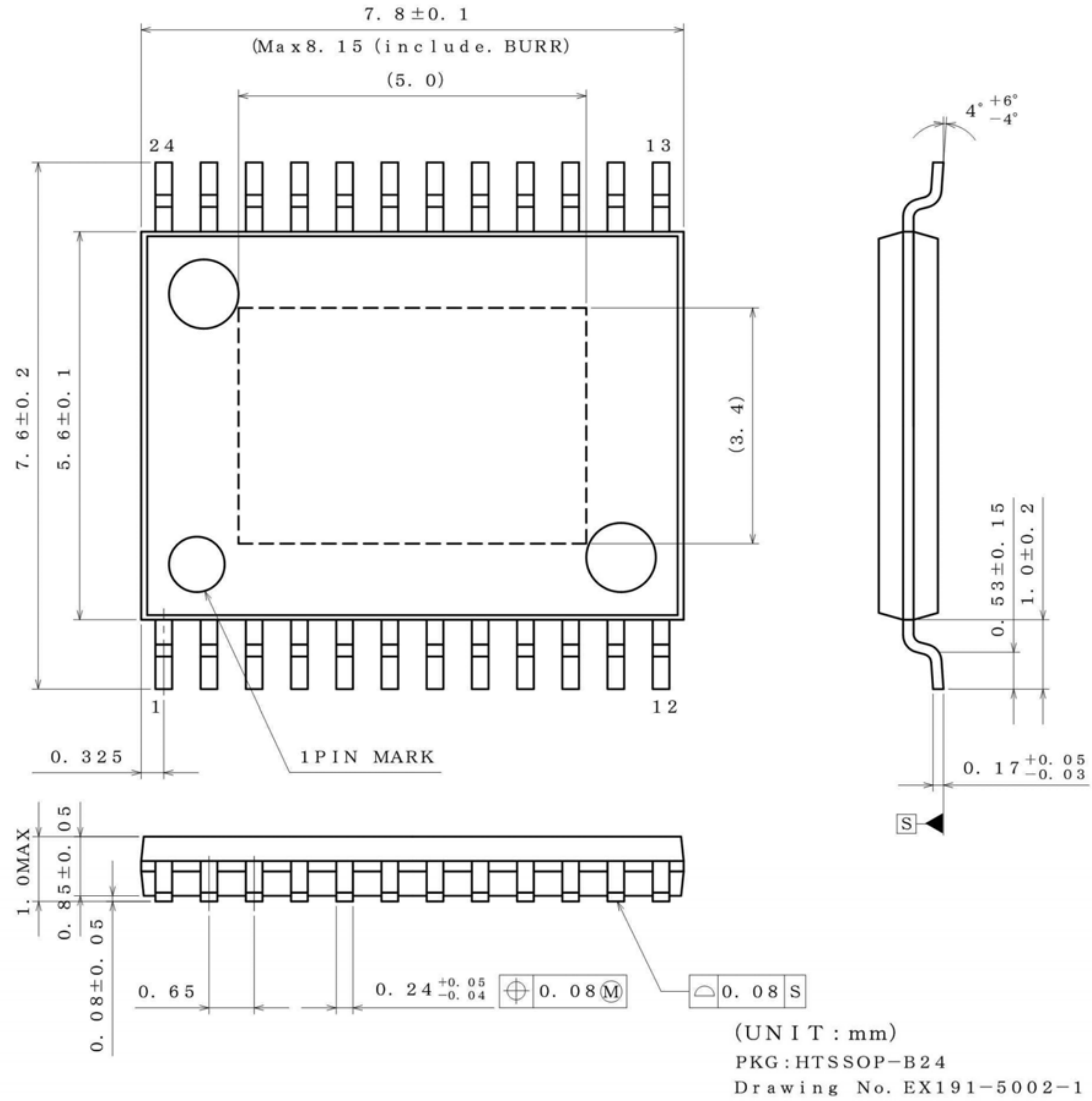


Marking Diagrams



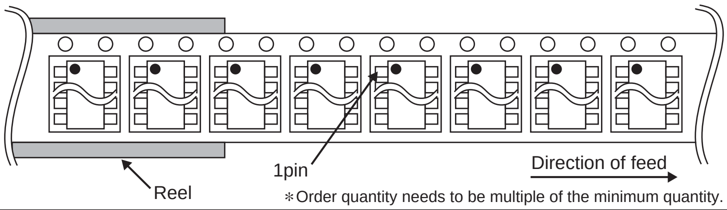
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Rev	Changes
16.Dec.2014	002	New Release
18.Aug.2015	003	P.1 About “Feature”,add a postscript to explanatory note of AEC-Q100. P.3 About “Absolute Maximum Ratings”, add a postscript to explanatory note of Active Clamp Energy(repetitive). P.4 About “Output Sink Current”, change the limit values of Typ & Max. P.4 About “Output Sink Current” & “Output Leak Current, add a postscript to V_{DIR} condition. P.12 About “I/O Equivalent Circuits”, add a postscript to pull-down resistance of input terminal.
23.May.2016	004	P4 About name of Electrical Characteristics items, correct following name. Before: Output sink current ($I_{L(OFF)}$) After: Output leak current($I_{L(OFF)}$) About Output leak current (Open load detected), correct the limit values. P17 About Figure26., correct V_{DD} condition. P22 About Open detection Note of Detection functions, add an explanatory note. P26 About Operational Notes, correct No.5. About Operational Notes, correct No.10. P27 About Ordering Information, correct Package information.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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General Precaution

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