

System Motor Driver Series for CD•DVD Player

4ch System Motor Driver

For Car Audio

BD8226EFV

General Description

BD8226EFV is a 5-input, 4-output BTL driver developed for driving Spindle motor (CH1), Sled/Loading motor (CH2) and the actuator coils (CH3:Tracking coil, CH4:Focus coil). This IC can be used for CD and DVD applications.

Features

- 4CH BTL Driver
- Has wide dynamic range
- Built-in thermal shutdown circuit
- Separating Vcc into Pre and Power (Power divides into CH1/2 and CH3/4) can improve efficiency.
- Switches CH2 input using Control input terminal (CNT)
- Incorporates mute function using CNT and MUTE terminals
- Built-in variable regulator control

Key Specifications

- Power supply voltage 5.5V to 14V
- Operating temperature range -40°C to +85°C
- Maximum output amplitude
 $(V_{PREVCC1}=V_{POWVCC1,2}=8V, R_L=8\Omega)$
 CH1,CH2 6.0V(Typ)
 CH3,CH4 5.3V(Typ)

Package

HTSSOP-B24

W(Typ) D(Typ) H(Max)
 7.80mm x 7.60mm x 1.00mm



HTSSOP-B24

Applications

Car Audio

Typical Application Circuit

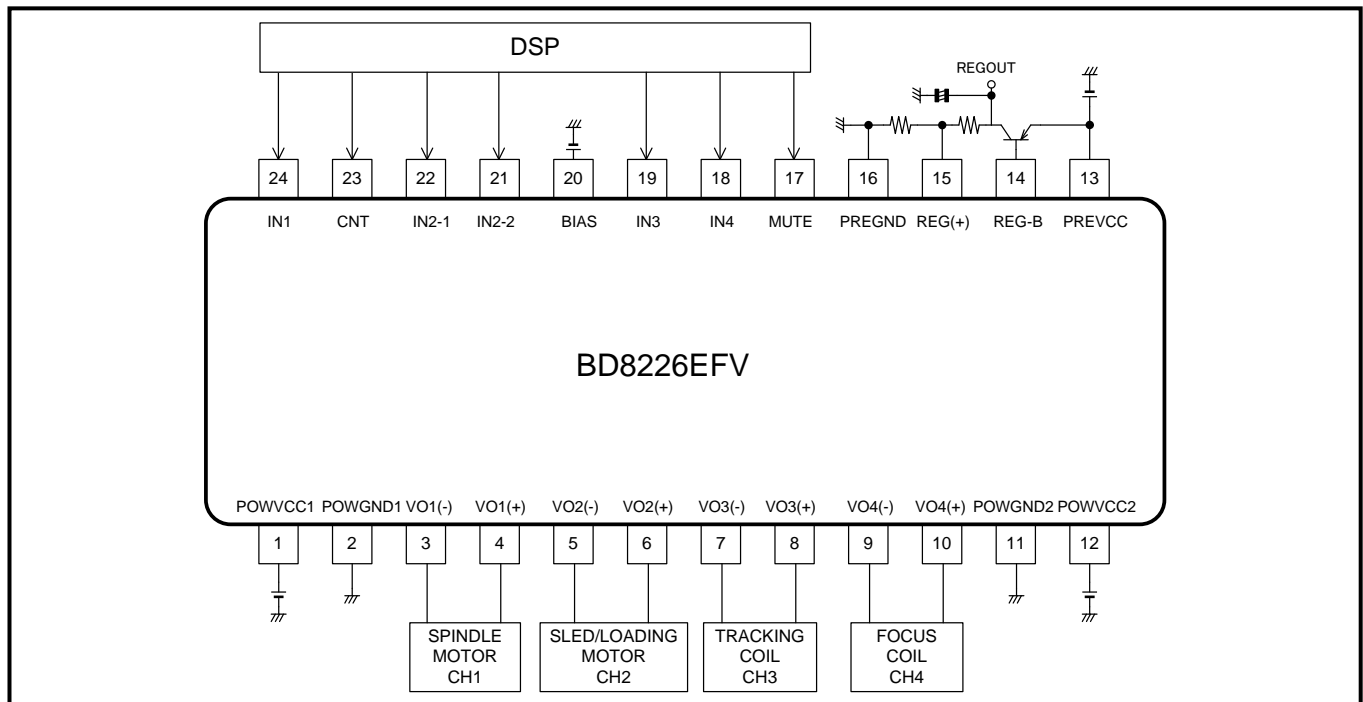


Figure 1. Application Circuit

Pin Configuration

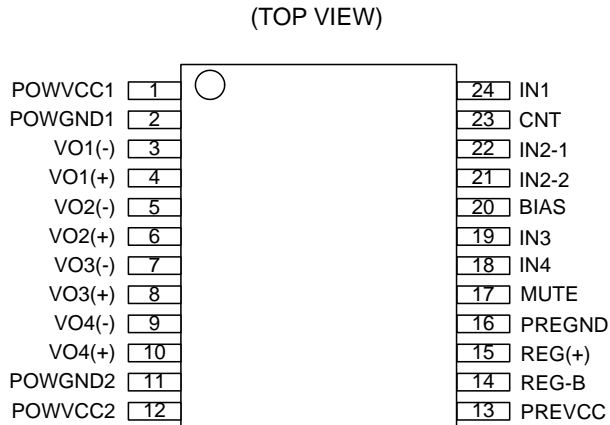


Figure 2. Pin Configuration

Pin Description

Pin No.	Symbol	Function
1	POWVCC1	CH1,2 power supply terminal
2	POWGND1	Power GND1
3	VO1(-)	Driver CH1 negative output
4	VO1(+)	Driver CH1 positive output
5	VO2(-)	Driver CH2 negative output
6	VO2(+)	Driver CH2 positive output
7	VO3(-)	Driver CH3 negative output
8	VO3(+)	Driver CH3 positive output
9	VO4(-)	Driver CH4 negative output
10	VO4(+)	Driver CH4 positive output
11	POWGND2	Power GND2
12	POWVCC2	CH3,4 power supply terminal
13	PREVC	PRE,REG power supply terminal
14	REG-B	Connect to external Tr. Base
15	REG(+)	Regulator terminal of output feedback
16	PREGND	PRE Block and Regulator GND
17	MUTE	MUTE terminal
18	IN4	CH4 input
19	IN3	CH3 input
20	BIAS	BIAS input terminal
21	IN2-2	CH2-2 input
22	IN2-1	CH2-1 input
23	CNT	Control input terminal
24	IN1	IN1 input

Block Diagram

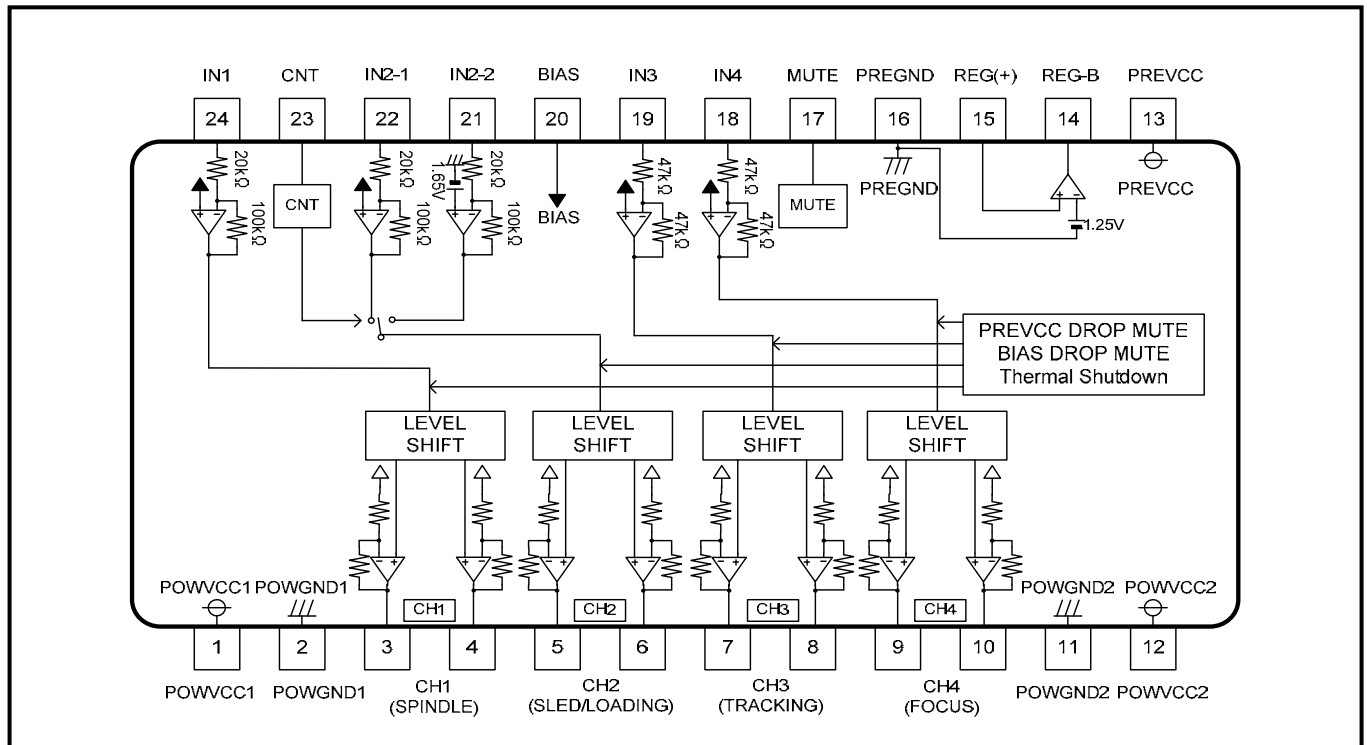


Figure 3. Block Diagram

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V _{PREVCC} , V _{POWVCC1} , V _{POWVCC2}	15	V
Input Terminal Voltage	V _{in1} ⁽¹⁾	V _{PREVCC}	V
Power Dissipation	Pd	1.1 ⁽²⁾	W
		4.0 ⁽³⁾	
Operating Temperature Range	T _{opr}	-40 to +85	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Junction Temperature	T _{jmax}	+150	°C

(1) Vin1 supplies the following terminals: IN1, CNT, IN2-1, IN2-2, BIAS, IN3, IN4, MUTE, REG(+)

(2) Rated for 70mm×70mm×1.6mm, one layer substrate (back copper foil 0mm×0mm),
Derated by 8.8mW/°C when operating above Ta=25°C.

(3) Rated for 70mm×70mm×1.6mm, four layer substrate (back copper foil 70mm×70mm),
Derated by 32.0mW/°C when operating above Ta=25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

Recommended Operating Ratings (Ta=-40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
PRE Driver Block Power Supply Voltage ⁽⁴⁾	V _{PREVCC}	4.5	8.0	14	V
DC Motor Driver Power Supply Voltage ⁽⁴⁾	V _{POWVCC1}	4.5	8.0	V _{PREVCC}	V
Actuator Driver Power Supply Voltage ⁽⁴⁾	V _{POWVCC2}	4.5	8.0	V _{PREVCC}	V

(4) Consider power consumption when deciding power supply voltage.

Electrical Characteristics (Unless otherwise noted, Ta=25°C, V_{PREVCC}=V_{POWVCC1}=V_{POWVCC2}=8V, V_{BIAS}=1.65V, R_L=8Ω)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Quiescent Dissipation Current	I _Q	—	30	45	mA	No load
< Driver >						
Output Offset Voltage (CH1,2)	V _{OOF12}	-100	0	100	mV	
Output Offset Voltage (CH3,4)	V _{OOF34}	-50	0	50	mV	
Maximum Output Amplitude (CH1,2)	V _{OM12}	5.4	6.0	—	V	
Maximum Output Amplitude (CH3,4)	V _{OM34}	4.7	5.3	—	V	
Closed-loop Voltage Gain (CH1,2)	G _{V12}	24.0	25.7	27.4	dB	
Closed-loop Voltage Gain (CH3,4)	G _{V34}	15.5	17.5	19.5	dB	
MUTE Terminal Low Level Input Voltage	V _{ML}	—	—	0.5	V	
MUTE Terminal High Level Input Voltage	V _{MH}	2.0	—	—	V	
CNT Terminal Low Level Input Voltage	V _{CNTL}	—	—	0.5	V	
CNT Terminal High Level Input Voltage	V _{CNTH}	2.0	—	—	V	
LDIN Terminal Voltage (SLED Input)	V _{LDIN}	—	0.1	0.3	V	CNT='Low'
Internal Bias Voltage	V _{BIN}	1.53	1.65	1.77	V	CNT='High'
< Regulator >						
Output Voltage	V _{REGOUT}	4.75	5.0	5.25	V	I _{REG} =150mA
Load Regulation	ΔV _{RL}	-40	0	20	mV	I _{REG} =0mA to 500mA, 5V setting
Supply Voltage Regulation	ΔV _{VCC}	-40	20	80	mV	V _{PREVCC} =5.5V to 14V, 5V setting
REG(+) Terminal Voltage	V _{REGP}	1.19	1.25	1.31	V	

Application Information

1. Driver Control

The mute function of the driver can be used by switching the MUTE and CNT terminals to High and Low levels. The table below shows the logic.

INPUT		OUTPUT	
MUTE	CNT	CH1,3,4	CH2
H	H	ACTIVE	LD ON
H	L	ACTIVE	SL ON
L	H	MUTE	LD ON
L	L	MUTE	MUTE

SL : SLED LD : LOADING

2. BIAS Drop Mute

If BIAS terminal (Pin 20) voltage becomes 0.7V (Typ) or less, output of all channels turns OFF.

Please set it to a minimum of 1.3V for typical use.

(However, the mute function doesn't work for CH2 when CNT=High.)

3. PREVCC Drop Mute

If PREVCC terminal voltage becomes 3.8V (Typ) or less, output of all channels turns OFF.

If PREVCC terminal voltage becomes 4.0V (Typ) or more, output of all channels turns ON.

4. Thermal shutdown circuit (TSD)

Thermal shutdown circuit is designed to turn off output of all channels when the junction temperature (Tj) reaches 175°C (Typ) (with 25°C (Typ) hysteresis).

5. Regulator

Output voltage of the regulator (V_{REGOUT}) is set according to the following expression.

$$V_{REGOUT} = V_{REGP} \times \frac{R1 + R2}{R2}$$

Please disable the oscillation prevention beforehand, and use the capacitor connected between the regulator output (V_{REGOUT}) and PREGND after confirming parameters such as temperature characteristics in actual operation.

The power supply voltage fluctuation described in the Electrical Characteristics is obtained when V_{REGOUT} is 5V.

Please note that fluctuation bands increase from the described values if V_{REGOUT} is set to a value bigger than 5V.

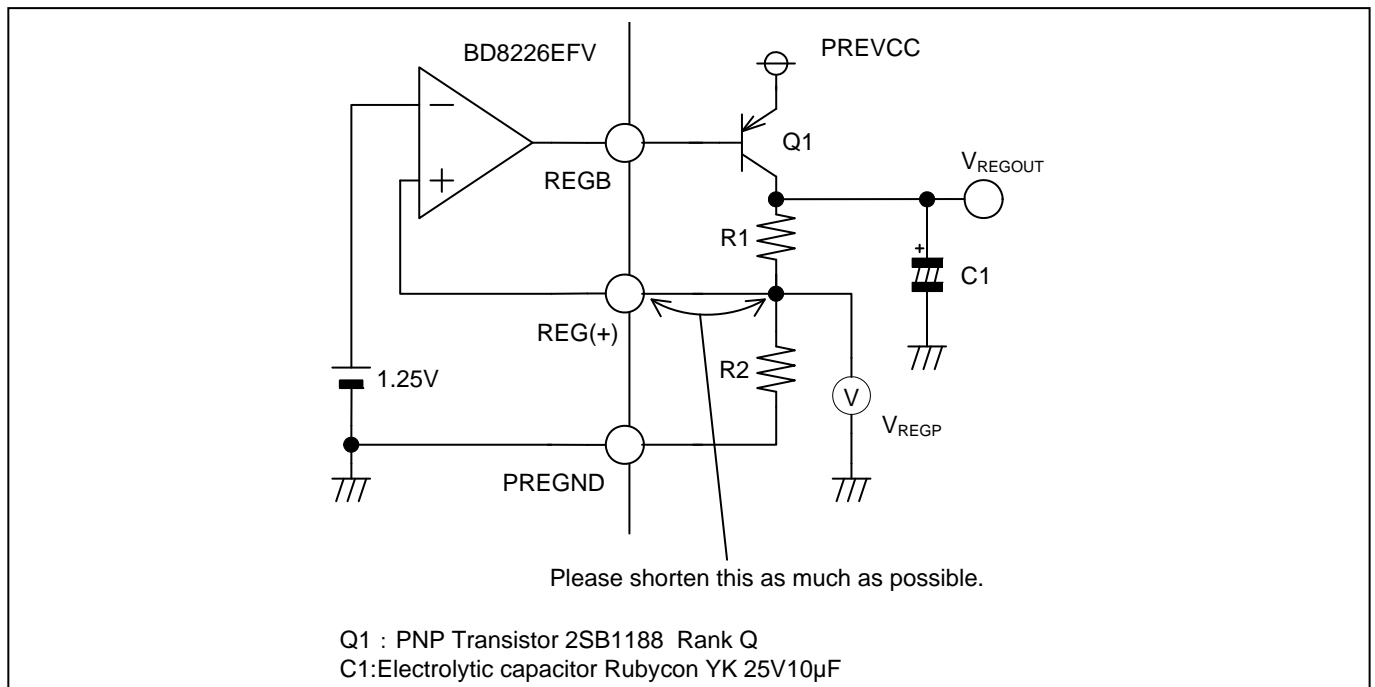


Figure 4. Regulator Block Diagram

6. Input Sequence

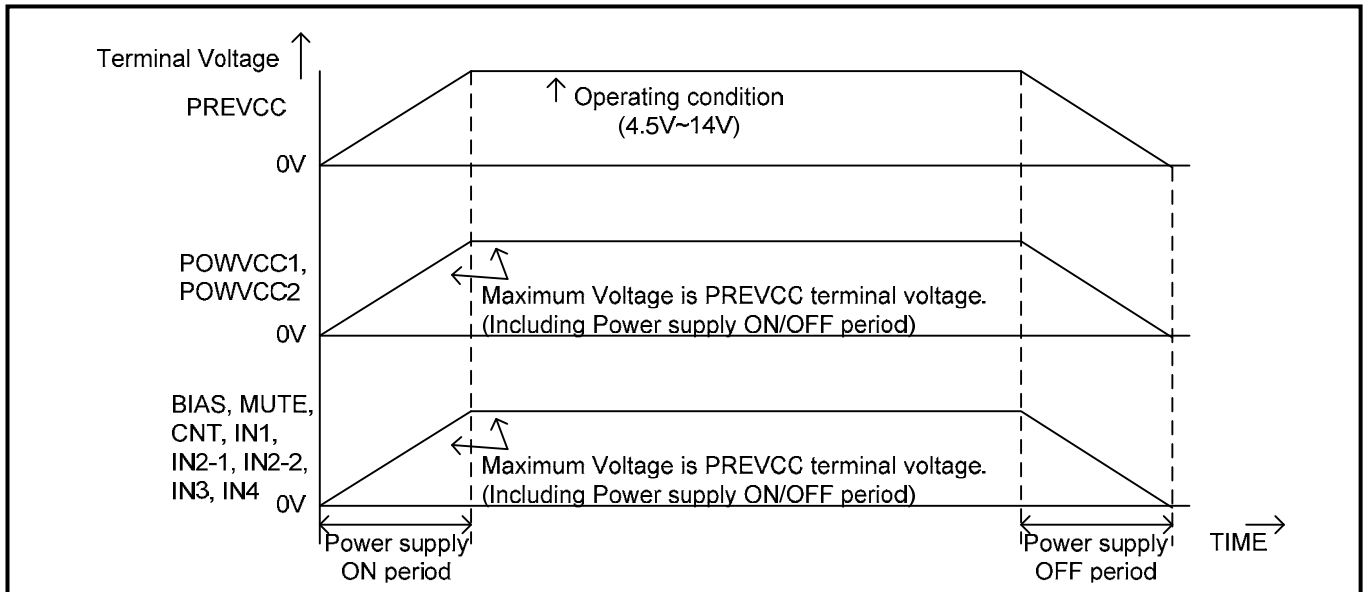


Figure 5. Input sequence

Please use the below formula to determine the power supply voltage and the voltage for each input terminal.

$$\text{PREVCC} \geq \text{POWVCC1, POWVCC2, BIAS, MUTE, CNT, IN1, IN2-1, IN2-2, IN3, IN4}$$

There is no special rule for power-up sequence if inputs are within the range of the above formula.

It is not recommended that terminal voltage for BIAS, MUTE, CNT, IN1, IN2-1, IN2-2, IN3, and IN4 exceed PREVCC voltage.

If these voltages exceed PREVCC, overcurrent is generated in the internal ESD protection diode. (refer to Figure 6)

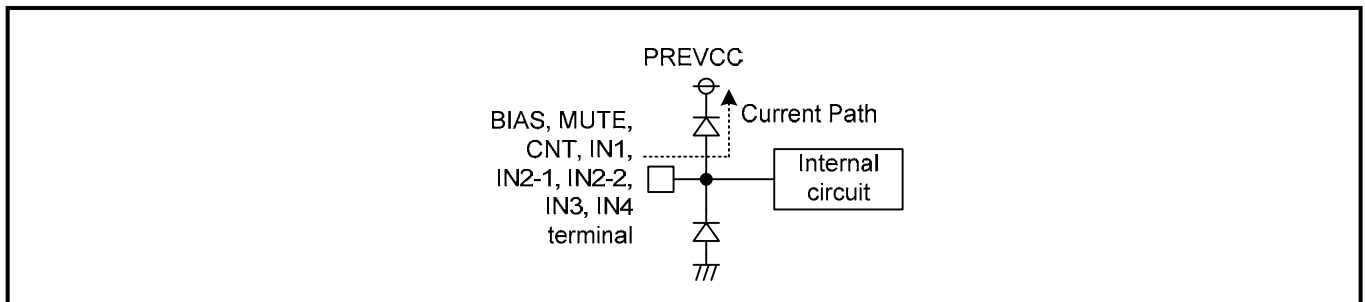


Figure 6. Internal Circuit Current

Typical Application Circuit

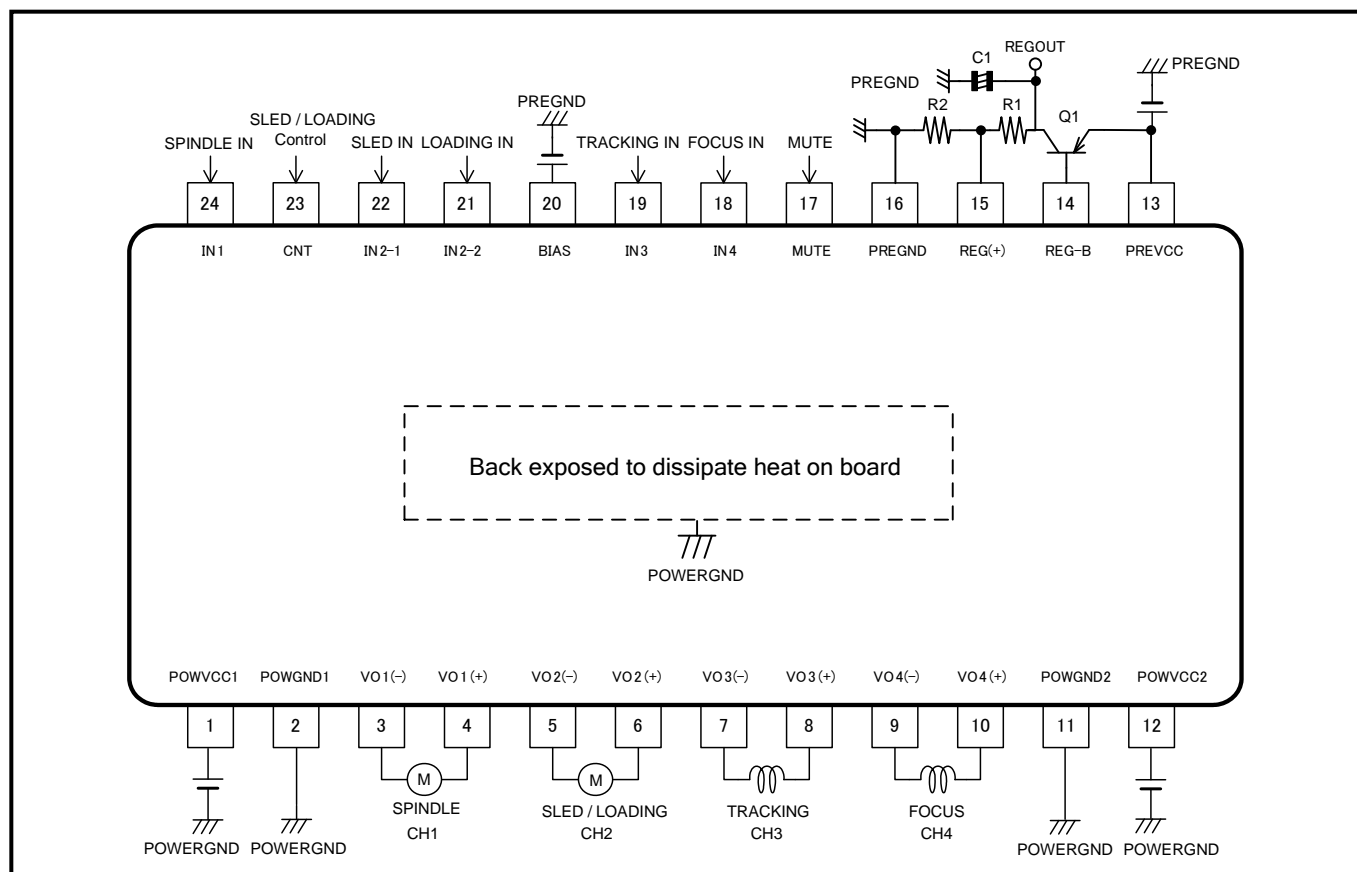


Figure 7. Typical Application Circuit

Channel Example

Channel Example	
CH1	SPINDLE
CH2	SLED/LOADING
CH3	TRACKING
CH4	FOCUS

External Part List

Component Name	Component Value	Product Name	Manufacturer
C1	10μF	YK25V Series	Rubycon
Q1	Rank Q	2SB1188	Rohm
R1	33kΩ	MCR03 Series	Rohm
R2	11kΩ	MCR03 Series	Rohm

Power Dissipation

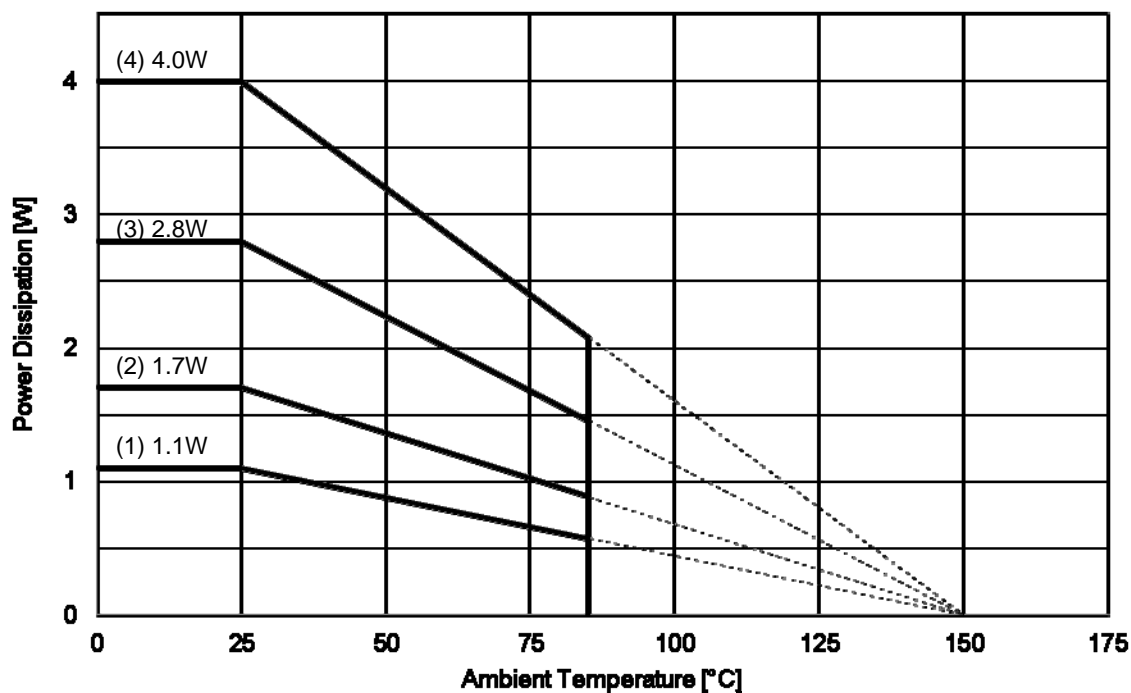


Figure 8. Power Dissipation

Board size : 70mm×70mm×1.6mm

The board and the back exposure heat radiation board part of package are connected with solder.

Board (1): 1 layer board (copper foil 0mm × 0mm)

Board (2): 2 layer board (copper foil 15mm × 15mm)

Board (3): 2 layer board (copper foil 70mm × 70mm)

Board (4): 4 layer board (copper foil 70mm × 70mm)

Board (1) : $\theta_{ja} = 113.6 \text{ }^{\circ}\text{C/W}$

Board (2) : $\theta_{ja} = 73.5 \text{ }^{\circ}\text{C/W}$

Board (3) : $\theta_{ja} = 44.6 \text{ }^{\circ}\text{C/W}$

Board (4) : $\theta_{ja} = 31.3 \text{ }^{\circ}\text{C/W}$

For $T_a=85^{\circ}\text{C}$:

Board (1) : $P_d = 0.57\text{W}$

Board (2) : $P_d = 0.88\text{W}$

Board (3) : $P_d = 1.46\text{W}$

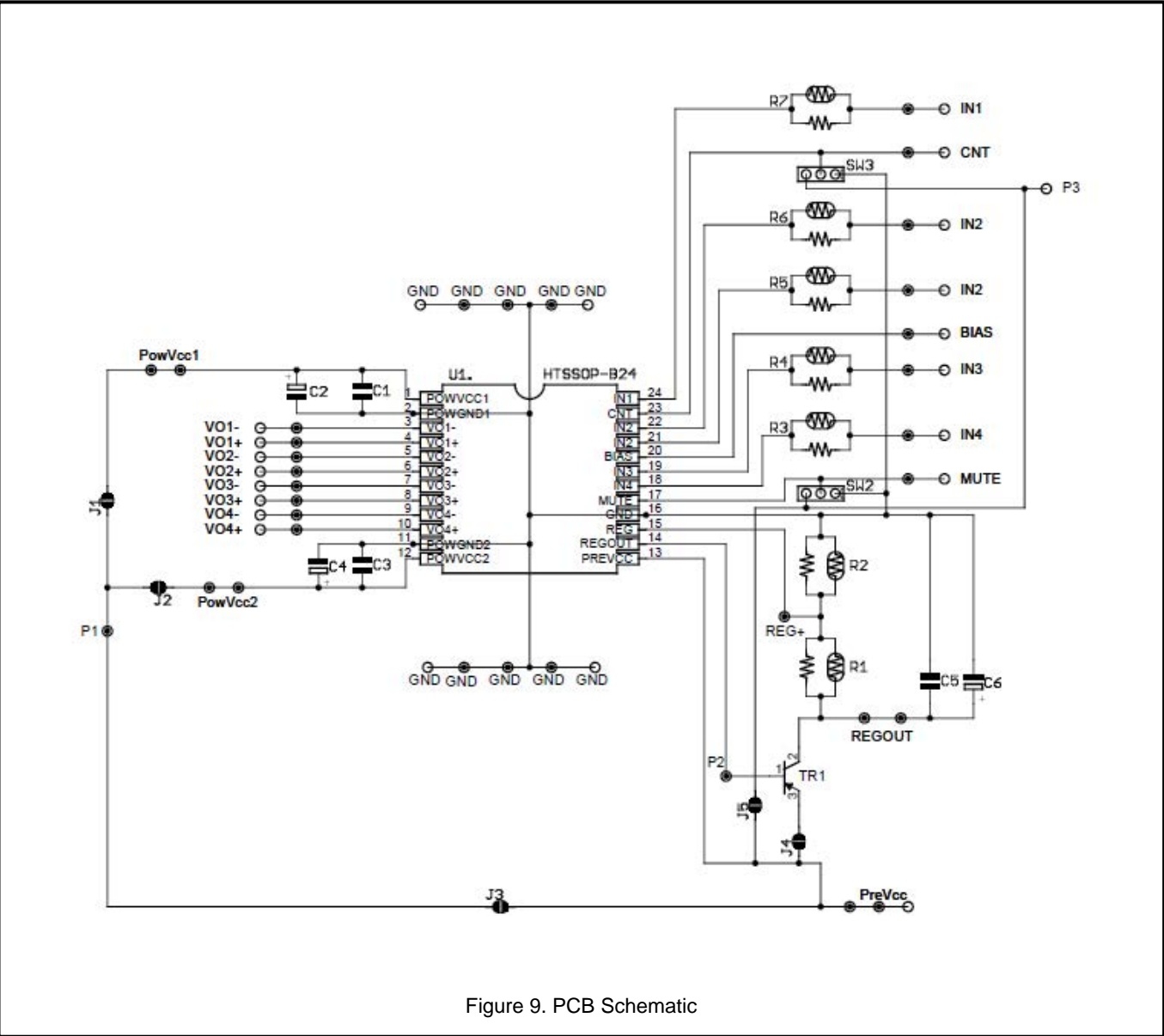
Board (4) : $P_d = 2.08\text{W}$

CAUTION: P_d depends on the number of the PCB layers and area. P_d values are determined through measurement.

Terminal Equivalent Circuit (with typical resistance and capacitance values)

BIAS input		Driver input	
Driver output		Driver input	
MUTE input		Driver input	
CNT input		Driver input	
Driver output		Regulator	
Regulator			

Application Board Schematic



Application Board Pattern

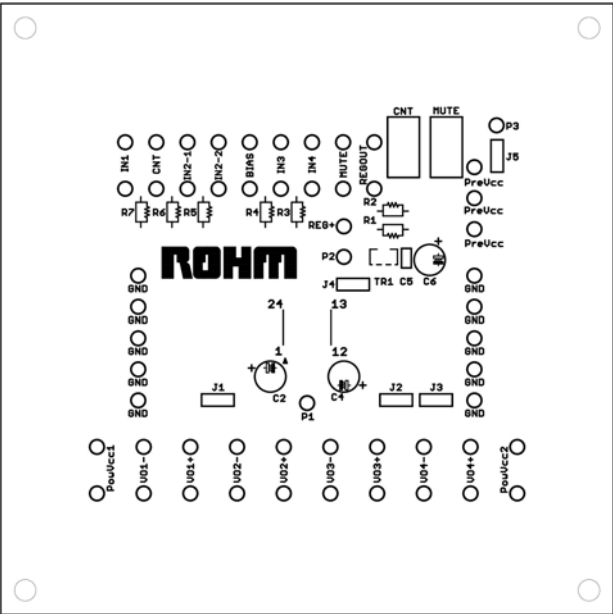


Figure 10. Top Silkscreen Overlay

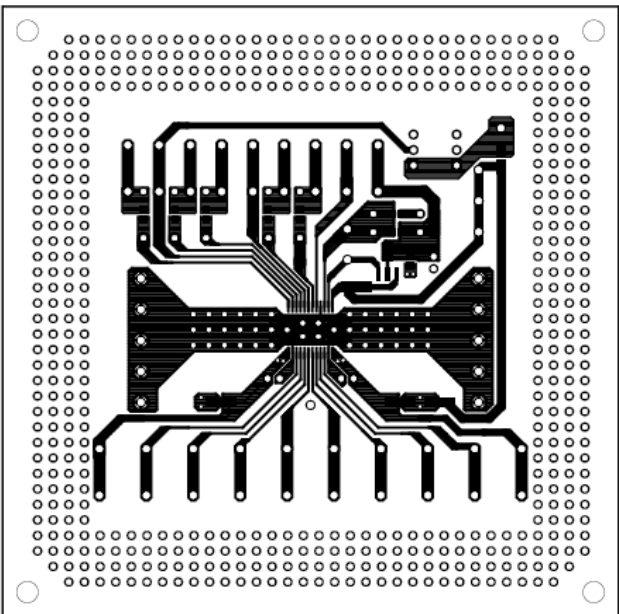


Figure 11. Top Layer

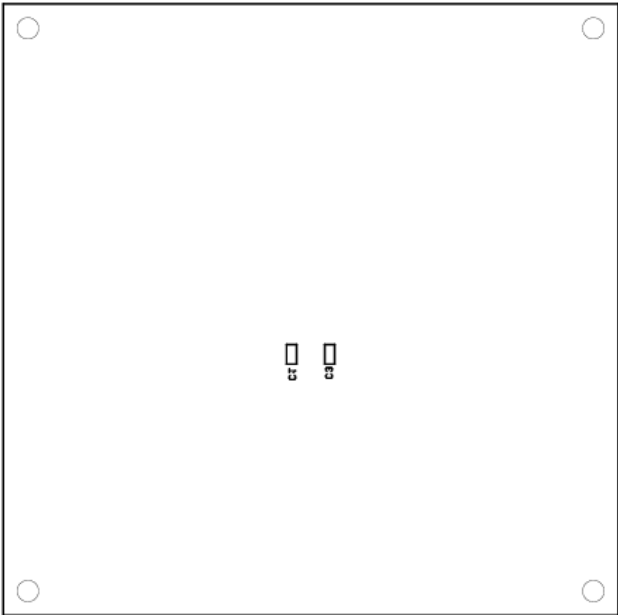


Figure 12. Bottom Silkscreen Overlay

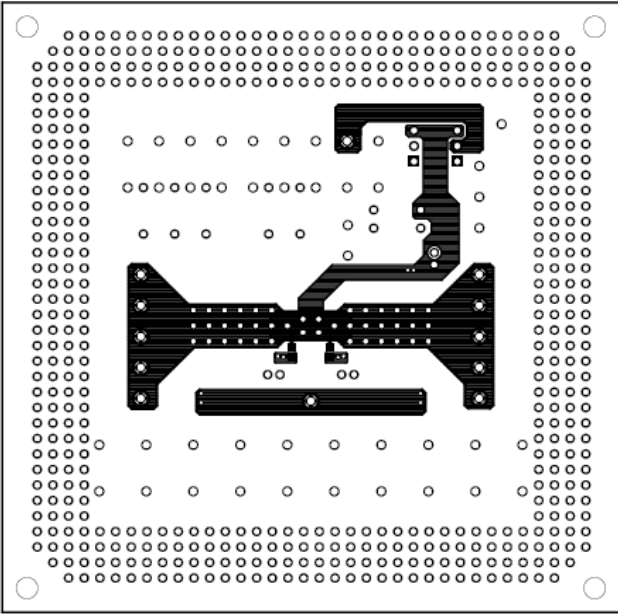


Figure 13. Bottom Layer

Operational Notes**1. Reverse Connection of Power Supply**

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Rush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes - continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

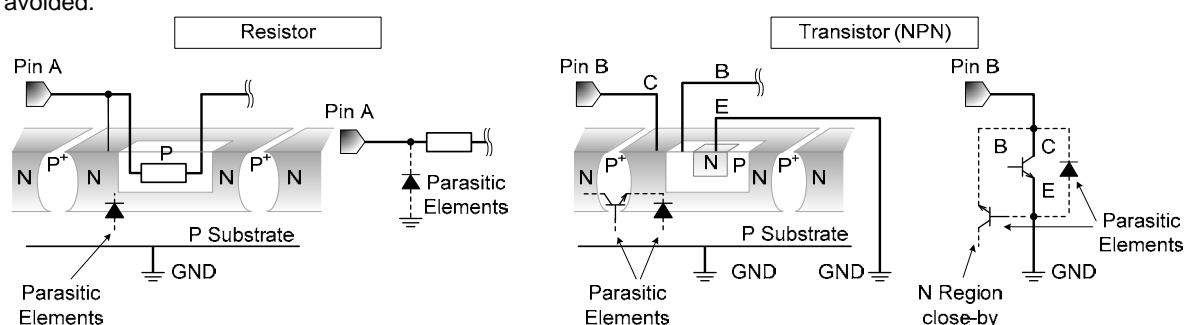


Figure 14. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit (TSD)

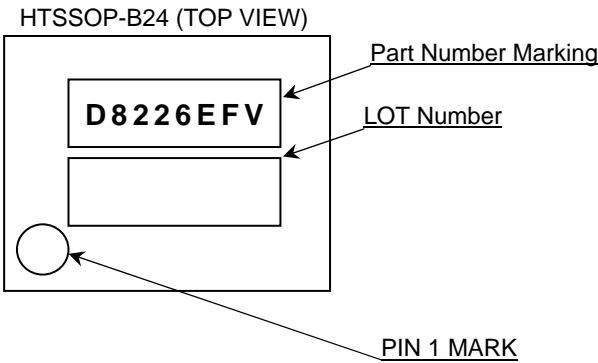
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

B D 8 2 2 6 E F V										-	E 2	
Product name					Package EFV : HTSSOP-B24					Packaging and forming specification E2: Embossed tape and reel (HTSSOP-B24)		

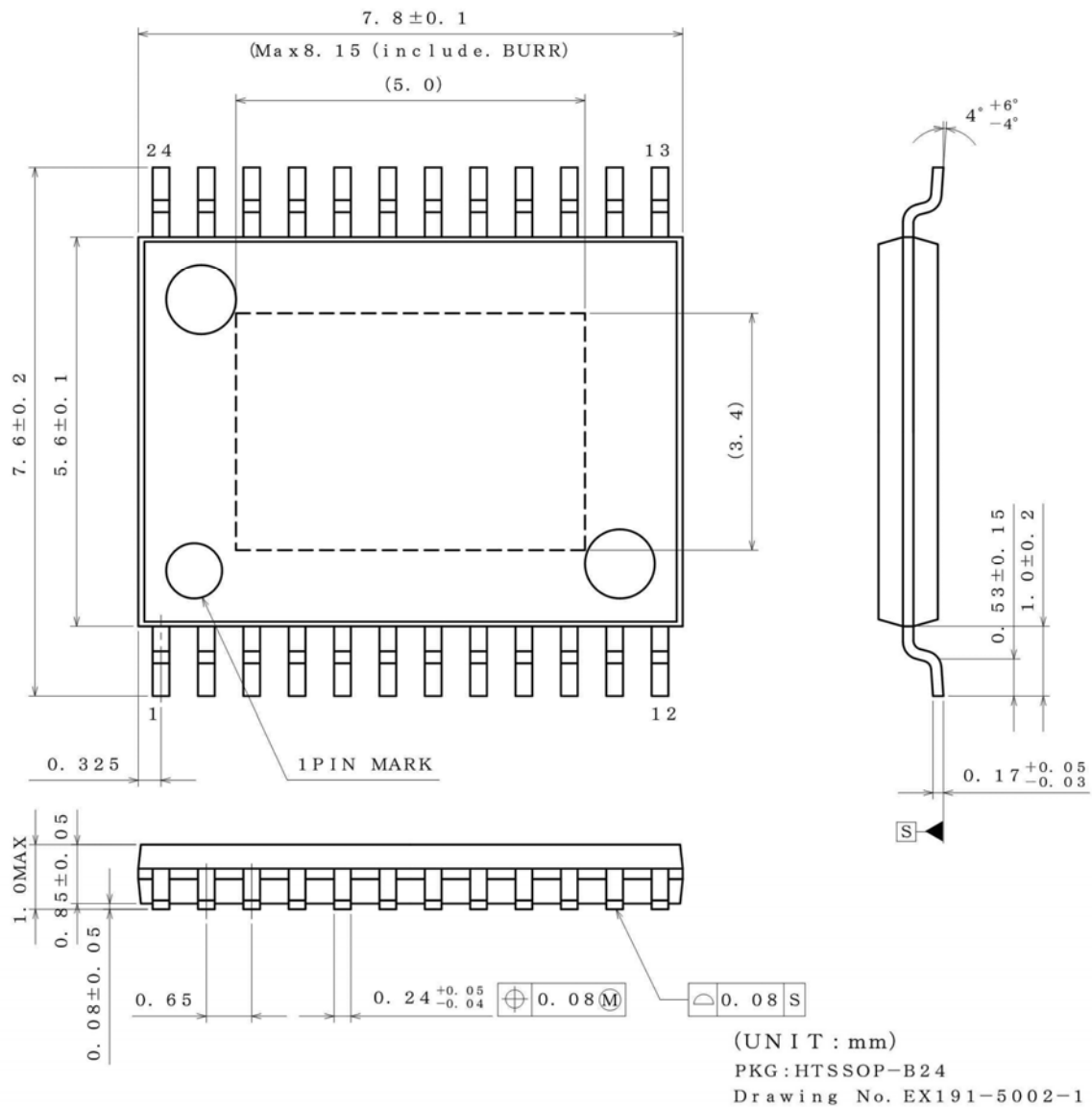
Marking Diagram



Physical Dimension, Tape and Reel Information

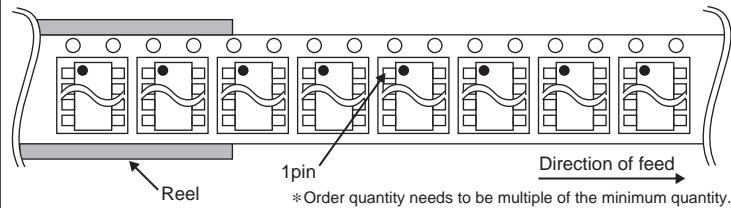
Package Name

HTSSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
3.JUL.2013	002	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
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2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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