

PART NUMBER:

KXCNL-1010 Rev 3.0

Product Description

The KXCNL-1010 is a tri-axis +/-2g, +/-4g, +/-6g, or +/-8g silicon micromachined accelerometer with integrated programmable state machines. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning, and intelligent user-programmable state machines. The accelerometer is delivered in a 3 x 3 x 0.9 mm LGA plastic package operating from a 1.8 – 3.6V DC supply. I²C interface is used to communicate to the chip to load state programs, configure settings, and check updates to the acceleration data.

Functional Diagram





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Product Specifications

Table 1. Mechanical

| (specifications are for 12-bit operation at 2.5V and T = 25C unless stated otherwise |
|--|
|--|

| P | Units | Min | Typical | Max | |
|--------------------------|-----------------------|-------------|----------|----------------------|--|
| Operating Temperatu | °C | -40 | - | 85 | |
| Zero-g Offset | | mg | | ±25 | |
| Zero-g Offset Variatio | on from RT over Temp. | mg/⁰C | | 0.5 (xy), 0.8 (z) | |
| | SC_1=0, SC_0=0 (± 2g) | | | 1024 | |
| Sanaitivity ¹ | SC_1=0, SC_0=1 (± 4g) | agunto/a | | 5 <u>12</u> | |
| Sensitivity | SC_1=1, SC_0=0 (± 6g) | counts/g | | 341 | |
| | SC_1=1, SC_0=1 (± 8g) | | | 256 | |
| Sensitivity Variation f | rom RT over Temp. | %/°C | | 0.01 | |
| | | | | 0.5 (x) | |
| Self Test Output char | nge on Activation | g | | 0.7 (y) | |
| | | | | 0.7 (z) | |
| Mechanical Resonan | $ce (-3dB)^2$ | H7 | | 3500 (xy) | |
| Moonanioa Robonan | 112 | | 1800 (z) | | |
| Non-Linearity | % of FS | | 0.5 | | |
| Cross Axis Sensitivity | / | % | | 2 | |
| Noise ³ | | µg/sqrt(Hz) | | 400 | |

Notes:

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- 1. Acceleration ranges are user selectable via I²C.
- 2. Resonance as defined by the dampened mechanical sensor.
- 3. Measured in \pm 2g range and including variation over operating temperature range at ODR5 (100Hz).



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Table 2. Electrical

| (specifications are for operation at 2.5V and T = 25C unless stated otherwise) | | | | | | |
|--|-----------------------|-------|-----------------------|-----------------------|-----------------------|--|
| Para | Units | Min | Typical | Max | | |
| Supply Voltage (V _{dd}) | Operating | V | 1.7 | 2.5 | 3.6 | |
| I/O Pads Supply Voltag | ge (V _{IO}) | V | 1.12 | 2.5 | V _{dd} | |
| | Active-mode ODR7 | | | 150 | * | |
| | Active- mode ODR5 | | | 125 | | |
| Current Consumption | Active-mode ODR0 | μA | | 35 | | |
| | Standby-mode | | | 0.2 | | |
| | Off-mode Leakage | | | 0.2 | | |
| Output Low Voltage (V | V | | | 0.2 * V _{IO} | | |
| Output High Voltage (V | / _{ОН}) | V | 0.8 * V _{IO} | | | |
| Input Low Voltage (VIL |) | V | 0 | | 0.3 * V _{IO} | |
| Input High Voltage (V _{II} | 4) | V | 0.7 * V _{IO} | | V _{IO} | |
| Input Pull-down Currer | nt | μA | | 0 | | |
| Power Up Time ² | | ms | | 3 | | |
| Start Up Time ³ | | ms | | 2 | | |
| Turn Off Time ⁴ | ms | | 1 | | | |
| Interrupt Pulse Width (| μs | | 100 | | | |
| I ² C Communication Ra | MHz | | | 3.4 | | |
| Output Data Rate (OD | Hz | 3.125 | 100 | 1600 | | |
| Bandwidth (-3dB) ⁷ | | Hz | r | ODR/2 | | |
| | | | | | | |

Notes:

- Assuming I²C communication and minimum 1.5Kohm pull-up resistor on SCL and SDA pins.
- 2. Power up time is from V_{IO} and Vdd valid to device boot completion. (Off-mode to Standby-mode)
- Start up time is from Standby-mode to Active-mode.
- 4. Turn off time is from Active-mode to Standby-mode
- 5. Supports I²C Standard speed (100kHz), Fast speed (400kHz), and High speed (3.4MHz)
- 6. User selectable through I^2C .
- 7. User selectable and dependant on ODR.



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Table 3. Environmental

| Parar | neters | Units | Min | Typical | Max |
|-----------------------------------|-----------------|-------|------|-----------------------------------|------|
| Supply Voltage (V _{dd}) | Absolute Limits | V | -0.3 | - | 4.0 |
| Operating Temperatur | °C | -40 | - | 85 | |
| Storage Temperature | °C | -55 | - | 150 | |
| Mech. Shock (powere | g | - | | 5000 for 0.5ms 10000 for 0.2ms | |
| НВМ | | | - | | 2000 |
| ESD | MM | V | - | | 200 |
| | CDM | | - | - | 500 |



Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.



This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of omposition throughout "

uniform composition throughout."



This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Floor Life

Factory floor life exposure of the KXCNL reels removed from the moisture barrier bag should not exceed a maximum of 168 hours at 30C/70%RH. If this floor life is exceeded, the parts should be dried per the IPC/JEDEC J-STD-033A standard.





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Terminology

g

A unit of acceleration equal to the acceleration of gravity at the earth's surface.

$$1g = 9.8 \frac{m}{s^2}$$

One thousandth of a g (0.0098 m/ s^2) is referred to as 1 milli-g (1 mg)

Sensitivity

The sensitivity of an accelerometer is the change in output per unit of input acceleration at nominal V_{dd} and temperature. The term is essentially the gain of the sensor expressed in counts per g (counts/g) or LSB's per g (LSB/g). Occasionally, sensitivity is expressed as a resolution, i.e. milli-g per LSB (mg/LSB) or milli-g per count (mg/count). Sensitivity for a given axis is determined by measurements of the formula:

 $Sensitivity = \frac{(Output @+1g - Output @-1g)}{2a}$

The sensitivity tolerance describes the range of sensitivities that can be expected from a large population of sensors at room temperature and over life. When the temperature deviates from room temperature (25°C), the sensitivity will vary by the amount shown in Table 1.

Zero-g offset

Zero-g offset or 0-g offset describes the actual output of the accelerometer when no acceleration is applied. Ideally, the output would always be in the middle of the dynamic range of the sensor (content of the OUTX, OUTY, OUTZ registers = 00h, expressed as a 2's complement number). However, because of mismatches in the sensor, calibration errors, and mechanical stress, the output can deviate from 00h. This deviation from the ideal value is called 0-g offset. The zero-g offset tolerance describes the range of 0-g offsets of a population of sensors over the operating temperature range.

Self-test

Self-test allows a functional test of the sensor without applying a physical acceleration to it. When activated, an electrostatic force is applied to the sensor, simulating an input acceleration. The sensor outputs respond accordingly. If the output signals change within the amplitude specified in Table 1, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.



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Functionality

Sense element

The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. This process technology allows Kionix to create mechanical silicon structures which are essentially mass-spring systems that move in the direction of the applied acceleration. Acceleration sensing is based on the principle of a differential capacitance arising from the acceleration-induced motion. Capacitive plates on the moving mass move relative to fixed capacitive plates anchored to the substrate. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit.

ASIC interface

A separate ASIC device packaged with the sense element provides all of the signal conditioning and communication with the sensor. The complete measurement chain is composed by a low-noise capacitance to voltage amplifier which converts the differential capacitance of the MEMS sensor into an analog voltage that is sent through an analog-to-digital converter. The acceleration data may be accessed through the I²C digital communications provided by the ASIC. In addition, the ASIC contains all of the logic to allow the user to choose data rates, g-ranges, filter settings, and interrupt logic. Plus, there are two programmable state machines which allow the user to create unique embedded functions based on changes in acceleration.

Factory calibration

Kionix trims the offset and sensitivity of each accelerometer by adjusting gain (sensitivity) and 0-g offset trim codes stored in non volatile memory (OTP). Additionally, all functional register default values are also programmed into the non volatile memory. Every time the device is turned on or a software reset command is issued, the trimming parameters and default register values are downloaded into the volatile registers to be used during active operation. This allows the device to function without further calibration.





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Application Schematic



Table 4. KXCNL Pin Descriptions

| Pin | Name | Description |
|-----|-----------------|--|
| 1 | V _{IO} | The power supply input for the digital logic and communication bus. Decouple this pin to ground with a 0.001 - 0.01uF ceramic capacitor. |
| 2 | NC | Not Connected Internally. |
| 3 | NC | Not Connected Internally. |
| 4 | SCL | I ² C Serial Clock |
| 5 | GND | Ground |
| 6 | SDA | I ² C Serial Data |
| 7 | ADDR | I^2C Address selection. Connect to V_{I0} or GND to select I^2C slave address. |
| 8 | NC | Not Connected Internally. |
| 9 | INT2 | Physical Interrupt 2 |
| 10 | NC | Not Connected Internally. |
| 11 | INT1 | Physical Interrupt 1 / Data Ready |
| 12 | GND | Ground |
| 13 | NC | Not Connected Internally. |
| 14 | Vdd | The main power supply input. Decouple this pin to ground with a 0.1 - 0.47uF ceramic capacitor. |
| 15 | NC | Not Connected Internally. |
| 16 | NC | Not Connected Internally. |



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Test Specifications



Special Characteristics:

These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

Table 5. Test Specifications

| Parameter | Specification | Test Conditions | |
|--------------------------|---------------|------------------|--|
| Current consumption ODR7 | <250uA | 25C, Vdd = 2.5 V | |
| Offset | 150mg | 25C, Vdd = 2.5 V | |
| ODR clock accuracy | 10% | 25C, Vdd = 2.5 V | |

All specifications in Tables 1, 2, and 3 which are not listed in Table 5 (above) are tested on an audit or validation basis only and are not guaranteed to be within the minimum and maximum values prior to shipment.

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Static X/Y/Z Output Response versus Orientation to Earth's surface (1g): SC_1=0, SC_0=0 (± 2g)

| Position | 1 | 2 | 3 | 4 | 5 | 6 |
|------------|-------|-------|------|------|---------------|---------------|
| Diagram | | | | | Top Bottom | Bottom Top |
| X (counts) | 0 | -1024 | 0 | 1024 | 0 | 0 |
| Y (counts) | -1024 | 0 | 1024 | 0 | 0 | 0 |
| Z (counts) | 0 | 0 | 0 | 0 | 1024 | -1024 |
| | | | | | | |
| X-Polarity | 0 | - | 0 | + | 0 | 0 |
| Y-Polarity | - | 0 | + | 0 | 0 | 0 |
| Z-Polarity | 0 | 0 | 0 | 0 | + | - |

(1g)

Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

SC_1=0, SC_0=1 (± 4g)

| Position | 1 | 2 | 3 | 4 | 5 | 6 |
|------------|------|------|------|-----|--------|--------|
| | | | | | Тор | Bottom |
| Diagram | | • | | | Bottom | Тор |
| X (counts) | 0 | -512 | 0 | 512 | 0 | 0 |
| Y (counts) | -512 | 0 | 512 | 0 | 0 | 0 |
| Z (counts) | 0 | 0 | 0 | 0 | 512 | -512 |
| | | | | | | |
| X-Polarity | 0 | - | 0 | + | 0 | 0 |
| Y-Polarity | - | 0 | + | 0 | 0 | 0 |
| Z-Polarity | 0 | 0 | 0 | 0 | + | - |
| | | | (1g) | | | |

Earth's Surface



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Static X/Y/Z Output Response versus Orientation to Earth's surface (1g): SC_1=1, SC_0=0 (± 6g)

| Position | 1 | 2 | 3 | 4 | 5 | 6 |
|------------|------|------|-----|-----|---------------|---------------|
| Diagram | | | | | Top Bottom | Bottom Top |
| X (counts) | 0 | -341 | 0 | 341 | 0 | 0 |
| Y (counts) | -341 | 0 | 341 | 0 | 0 | 0 |
| Z (counts) | 0 | 0 | 0 | 0 | 341 | -341 |
| | | | | | | |
| X-Polarity | 0 | - | 0 | + | 0 | 0 |
| Y-Polarity | - | 0 | + | 0 | 0 | 0 |
| Z-Polarity | 0 | 0 | 0 | 0 | + | - |

(1g)

Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

| SC_ | 1=1 | , SC_ | _0=1 | (± | 8g) |
|-----|-----|-------|------|----|-----|
|-----|-----|-------|------|----|-----|

| Position | 1 | 2 | 3 | 4 | 5 | 6 |
|------------|------|------|-----|-----|--------|--------|
| | | | | | Тор | Bottom |
| Diagram | | | | | | |
| | | | | | Bottom | Гор |
| X (counts) | 0 | -256 | 0 | 256 | 0 | 0 |
| Y (counts) | -256 | 0 | 256 | 0 | 0 | 0 |
| Z (counts) | 0 | 0 | 0 | 0 | 256 | -256 |
| | | | | | | |
| X-Polarity | 0 | - | 0 | + | 0 | 0 |
| Y-Polarity | - | 0 | + | 0 | 0 | 0 |
| Z-Polarity | 0 | 0 | 0 | 0 | + | - |

Earth's Surface



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State Programs

The most important feature of the KXCNL is that it has two independent State Programs which can be programmed by the user to produce interrupts and peak values.

A State Program follows a structure of successive states. From each state (n) it is only possible to have a transition to the next state (n+1) or to the state pointed to by the Reset Pointer (state 1). Transition to the Reset Point happens when the "RESET condition" is true. Transition to the next step happens when "NEXT condition" is true. An interrupt is sent when the Output/Stop/Continue state is reached.



In the KXCNL, a State Program is a series of states, parameters and internal memories running an algorithm in its own logic machine. Two independent State Program areas are defined (State Program 1 and State Program 2).

- Each program can be one shot run or continuously running.
- Outputs of program are internal interrupt signal and interrupt source information.
- Program code steps and parameter sets are loaded into fixed register memory space by the host.
- Input data comes from measurement/signal blocks according ODR and DES2 timing definitions.

One sample is the timing base for the NEXT and RESET conditions. State Programs 1 and 2 are running independently or synchronized but with same input data.

Interrupts are the main output of the State Programs. According program flow, the channel that triggered the interrupt also memorizes its peak (highest or lowest) value.



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State Program 1 and 2 are identical and exactly working same manners with some exceptions as extra sub functionalities:

- State Program 2 has decimator functionality.
- State Program 2 has a difference (DIFF) functionality/filter. The DIFF filter can be configured with two settings:
 - Difference between current and previous data values (X,Y,Z)
 - Difference between current data values and a constant
- When DIFF functionality selected in State Program 2, vector calculated value (V) is left intact.

State Programs can be debugged with simple step method and host assistance. When register /CNTL1, bit DEBUG == 1, normal measurement data is not fed to the State Programs. Instead, the host feeds manual data to the debug input registers (/*X*, *Y*,*Z*_DEBUG) to imitate measurement data. This debug data is sent to the state programs after writing the /*Z*_DEBUG register (stepping command like clock).



Debug (input) data is feed to State Programs via registers:

- /X_DEBUG = debug feed for x channel
- /Y_DEBUG = debug feed for y channel
- /Z_DEBUG = debug feed for z channel



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Signal path

The acceleration measurement data flows through several paths according customizable setup of the KXCNL.



Real acceleration measurement data is available to external applications through the 12-bit /OUT_X, /OUT_Y, and /OUT_Z registers. Data is provided at the selected ODR.

The Integrated Functions of the KXCNL are not using the raw 12-bit data. There are several other data forms available for the Integrated Interrupt Functions (State Programs). Internal data sets in 8-bit format for State Programs usage are:

- Raw (X,Y,Z) acceleration data limited in range from -127 to +127
- Vector (V), calculated and filtered (if enabled), limited to range from -127 to +127
- DIFF is data process method which calculates the difference of the current (X,Y,Z) data measurement to the previous (X,Y,Z) data measurement or the difference of the current (X,Y,Z) data measurement to set of constants. (Available only for State Program 2)

Vector calculation and filter

Total (3D) vector length is calculated with an approximation formula. The calculated vector length result is filtered with an adjustable Band Pass filter. The vector approximation formulas are the following:

$$a1 = |x| + |y| + |z|$$

$$a2 = \max(|x|, |y|, |z|)$$

$$v_{raw} = (45 * a1 + 77 * a2)/256$$



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- x, y, z are the 8-bit measured acceleration values limited in range from -127 to +127.
- *a*1 and *a*2 are temporary maximum 16-bit values.
- 45 and 77 are fixed 8-bit constants.
- 256 is the scale factor for the calculation.
- v_{raw} is the vector length, maximum 16-bit scalar temporary value.
- If filtering is not enabled, v_{raw} is fed to the State Programs as V after a limiter of -127 to +127.

Vector filter:

When enabled, the 16-bit vector scalar (v_{raw}) data from the vector calculation phase is passed through a band pass filter. The target corner frequency for the band pass filter is 0.5Hz to 10Hz (in ODR5, 100Hz). ODR selection affects the corner frequencies so ODR5 as 100Hz is the main time base for the vector filter. Filter coefficients are adjustable. The calculation is performed with maximum 16-bit temporary values.

FIR filter, 7 orders (8 taps)

- 4 asymmetric coefficients (8b wide constants)
- 8 tap filter as 4x2 structure
 - /VFC_1, /VFC_2, /VCF_3, /VCF_4 and
 - -/VFC_1, -/VFC_2, -/VCF_3, -/VCF_4
 - o Reference construction: (53,127,127,53, -53,-127,-127,-53)
- Scale factor for filter output (temporary value) is 256 (16b to 8b) and it is limited to range from -127 to +127
- Output is 8b filtered vector scalar (V) data (/V_I internal memory)
- Last 8 input values are kept in /BUF1 to /BUF8 (8b) internal memories

Vector filter can be enabled or disable via register /CNTL4, bit VFILT setting.





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Power Modes

The KXCNL has three power modes: Off, Stand-by, and Active. The part exists in one of these three modes at any given time. Off and Stand-by modes have very low current consumptions.

| Power Mode | Bus State | V _{IO} | V _{dd} | Function | Outputs |
|---------------|-----------|-----------------|-----------------|-------------------------------|---------------|
| Off | - | OFF | OFF | No sensor activity | Not available |
| Off | - | ON | OFF | No sensor activity | Not available |
| Off | - | OFF | ON | No sensor activity | Not available |
| Stand-by | Active | ON | ON | Waiting activation command | Not available |
| Active | Active | ON | ON | All functionalities available | Available |

Off mode

One or both of the power supplies (V_{dd} or V_{IO}) are not powered. The sensor is completely inactive and not reporting or communicating. Bus communication actions of other devices are not disturbed if they are using the same bus interface as this component.

Initial Startup

The preferred startup sequence is to turn on V_{IO} before V_{dd} , but if V_{dd} is turned on first, the component will not affect the bus communications (no latch-up or other problems during engine system level wake-up).

Power On Reset (POR) is performed every time when:

- 1. V_{IO} supply is valid
- 2. V_{dd} power supply is going to valid level

OR

 V_{IO} power supply is going to valid level V_{dd} supply is valid

When POR occurs, the following registers and signals are set and the part is put into Stand-by mode:

- Interrupt (INT1/DRDY and INT2) signals are set to inactive (high Z)
- Registers set to default:
 - o /STAT
 - o /CNTL1 (14h)
 - o /CNTL2
 - o /CNTL3
 - o /CNTL4
 - Offset registers (/OFF_X, /OFF_Y, /OFF_Z)
 - o /OUTS1, OUTS2



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Stand-by mode

The primary function of the stand-by mode is to ensure fast wake-up to active mode and to minimize current consumption. This mode is set as default when both power supplies are applied and the POR function occurs. A Soft Reset command also performs the POR function and puts the part into Stand-by mode.

Stand-by mode is a low power waiting state for fast turn on time. All time critical functionalities are ready to start measurement. Bus communication actions of other components are not disturbed if they are using the same bus. There is only one possible way to change to active mode – a register command via the l^2C bus.

Active mode

Stand-by-mode can be changed to Active mode by writing to register /CNTL1, bit PC = 1.

Active mode engages the full functionality of accelerometer measurements. The host also has the ability to change settings in the control registers, readback status registers, and program state machines.

Active mode to Stand-by mode transitions

Two possible methods for transition from Active mode to Stand-by mode can be used.

- 1. Register /CNTL1, PC =0 command:
 - a. Status register /STAT1 is set to default value
 - b. Interrupt (*INT1/DRDY* and *INT2*) signals are set to inactive (High Z/High impedance)
 - c. Register memory is kept intact
- 2. Register /CNTL4, STRT=1 command:
 - a. changes are performed to physical signal and register values as POR sequence

When a transition from Active mode to Stand-by mode and back to Active mode has been done by the host:



If State Program 1 /CNTL2, SM1_EN = 1 (State Program 1 was running in earlier Active mode session), then State Program 1 is disabled during the Stand-by mode and re-enabled when the component is returned to Active mode. However, this resets State Program 1 to its Default Initial position.

• If State Program 2 /CNTL3, SM2_EN = 1 (State Program 2 was running in earlier Active mode session), then State Program 2 is disabled during the Stand-by mode and re-enabled when the component is returned to Active mode. However, this resets State Program 1 to its Default Initial position.



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KXCNL Digital Interface

The Kionix KXCNL digital accelerometer has the ability to communicate on the I²C digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 6 below will be observed throughout this document.

| Term | Description |
|-------------|---|
| Transmitter | The device that transmits data to the bus. |
| Receiver | The device that receives data from the bus. |
| Master | The device that initiates a transfer, generates clock signals, and terminates a transfer. |
| Slave | The device addressed by the Master. |

Table 6. Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KXCNL has the ability to communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KXCNL always operates as a Slave device during standard Master-Slave I²C operation.

 I^2C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I^2C bus is considered free when both lines are high.

I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The Slave Address associated with the KXCNL is:

| ADDR pin status | SAD | SAD + Read | SAD + Write |
|-----------------|---------------|----------------|----------------|
| ADDR = 0 | 0011110 (1Eh) | 00111101 (3Dh) | 00111100 (3Ch) |
| ADDR = 1 | 0011101 (1Dh) | 00111011 (3Bh) | 00111010 (3Ah) |

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it 36 Thornwood Dr. - Ithaca, NY 14850 tel: 607-257-1080 - fax:607-257-1146 © 2013 Kionix - All Rights Reserved 1.0 Page 20 of 51



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remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I²C bus is now free.

Writing to a KXCNL 8-bit Register

Upon power up, the KXCNL enters into stand-by mode. The I²C Master must write to the KXCNL's control registers to set its operational mode. Therefore, when writing to a control register on the I²C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KXCNL ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KXCNL to which 8-bit register the Master will be writing the data. The KXCNL acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KXCNL acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KXCNL is now stored in the appropriate register. The KXCNL automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

Reading from a KXCNL 8-bit Register

When reading data from a KXCNL 8-bit register on the I²C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KXCNL acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KXCNL again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KXCNL with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KXCNL automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page.

If a receiver cannot transmit or receive another complete byte of data until it has performed some other function, it can hold SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases SCL.





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Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the l^2C bus and how the Master and Slave interact during these transfers. Table 7 defines the l^2C terms used during the data transfers.

| Term | Definition | |
|------|---------------------------|-------------------|
| S | Start Condition | |
| Sr | Repeated Start Condition | |
| SAD | Slave Address | |
| W | Write Bit | |
| R | Read Bit | |
| ACK | Acknowledge | |
| NACK | Not Acknowledge | |
| RA | Register Address | |
| Data | Transmitted/Received Data | |
| Р | Stop Condition | $\mathbf{\Sigma}$ |

Table 7. I²C Terms

Sequence 1. The Master is writing one byte to the Slave.

| Master | S | SAD + W | | _ (F | RA | | DA | TA | | Ρ |
|--------|---|---------|-----|------|----|-----|----|----|-----|---|
| Slave | | | ACK | | | ACK | | | ACK | |

Sequence 2. The Master is writing multiple bytes to the Slave.

| Master | S | SAD + W | RA | DATA | | DATA | | Ρ |
|--------|---|---------|-----|------|-----|------|-----|---|
| Slave | | ACK | ACK | | ACK | | ACK | |

Sequence 3. The Master is receiving one byte of data from the Slave.

| Master S | SAD + W | | RA | | Sr | SAD + R | | | NACK | Ρ |
|----------|---------|---|----|-----|----|---------|-----|------|------|---|
| Slave | AC | K | | ACK | | | ACK | DATA | | |

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

| Master | S | SAD + W | | RA | | Sr | SAD + R | | | ACK | | NACK | Р |
|--------|---|---------|-----|----|-----|----|---------|-----|------|-----|------|------|---|
| Slave | | | ACK | | ACK | | | ACK | DATA | | DATA | | |



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HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5. HS-mode data transfer of the Master writing one byte to the Slave.

| Speed | | FS-mode | Э | | | | HS-m | ode | | | | FS-mode |
|--------|---|---------|------|---|---------|-----|------|-----|------|-----|---|---------|
| Master | S | M-code | NACK | S | SAD + W | | RA | | DATA | | Ρ | |
| Slave | | | | | | ACK | | ACK | • | ACK | | |
| | | | | | | | | | | | | |



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KXCNL Register Map

| | Type | I ² C | Read/Write | |
|------------------------|-------------|------------------|-------------|--|
| Register Name | Read/Write | / | Address | |
| | iteau/witte | Hex | Binary | |
| Reserved ¹ | | 00h – | 0000 0000 - | |
| | D | 0Ch | 0000 1100 | |
| /INFO1 | R R | 0Dh | 0000 1101 | |
| /INFO2 | R | OEh | 0000 1111 | |
| | P | 10h | 0001 0000 | |
| | R | 10h | 0001 0001 | |
| | R | 12h | 0001 0001 | |
| /OUTY H | R | 13h | 0001 0011 | |
| /OUTZ L | R | 14h | 0001 0100 | |
| /OUTZ_H | R | 15h | 0001 0101 | |
| /LC_L | R/W | 16h | 0001 0110 | |
| /LC_H | R/W | 17h | 0001 0111 | |
| /STAT | R | 18h | 0001 1000 | |
| /PEAK1 | R | 19h | 0001 1001 | |
| /PEAK2 | Ŕ | 1Ah | 0001 1010 | |
| /CNTL1 | R/W | 1Bh | 0001 1011 | |
| /CNTL2 | R/W | 1Ch | 0001 1100 | |
| /CNTL3 | R/W | 1Dh | 0001 1101 | |
| /CNTL4 | R/W | 1Eh | 0001 1110 | |
| /THRS3 | R/W | 1Fh | 0001 1111 | |
| /OFF_X | R/W | 20h | 0010 0000 | |
| /OFF_Y | R/W | 21h | 0010 0001 | |
| /OFF_Z | R/W | 22h | 0010 0010 | |
| Reserved | | 23h | 0010 0011 | |
| /CS_X | R/W | 24h | 0010 0100 | |
| <u>/US_Y</u> | R/W | 25h | 0010 0101 | |
| | R/W | 26h | 0010 0110 | |
| | DAM/ | 270 | 0010 0111 | |
| | R/W | 2011 20h | 0010 1000 | |
| | | 2911 | 0010 1001 | |
| /Z_DEB0G | | 2Rh | 0010 1010 | |
| | | 2011 201 | 0010 1011 | |
| | R/W | 2011 2Dh | 0010 1100 | |
| WEC 3 | R/W | 2Eh | 0010 1101 | |
| ///FC_4 | R/W | 2Eh | 0010 1111 | |
| | | 30h - | 0011 0000 - | |
| Reserved | | 3Fh | 0011 1111 | |
| /ST1_1 | W | 40h | 0100 0000 | |
| /ST2_1 | W | 41h | 0100 0001 | |
| /ST3_1 | W | 42h | 0100 0010 | |
| /ST4_1 | W | 43h | 0100 0011 | |
| /ST5_1 | W | 44h | 0100 0100 | |
| /ST6_1 | W | 45h | 0100 0101 | |
| /ST7_1 | W | 46h | 0100 0110 | |
| /ST8_1 | W | 47h | 0100 0111 | |
| /ST9_1 | W | 48h | 0100 1000 | |
| /ST10_1 | W | 49h | 0100 1001 | |
| /ST11_1 | W | 4Ah | 0100 1010 | |
| /ST12_1 | W | 4Bh | 0100 1011 | |
| /ST13_1 | W | 4Ch | 0100 1100 | |
| /SI14_1 | W | 4Dh | 0100 1101 | |
| /SI15_1 | W | 4Eh | 0100 1110 | |
| /5116_1 | W NY | 4Fh | 0100 1111 | |
| / T IIVI4_1 /TIM2_4 | VV | 500 | 0101 0000 | |
| /111/13 1 | V V | 1 310 | | |



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| Image: Time 1. Near Mark 1. Hex Binary /TIM2_1_H W 52h 0101 0010 /TIM1_1_L W 53h 0101 0100 /TIM1_1_H W 53h 0101 0101 /TIM5_1_L W 56h 0101 0101 /THRS2_1 W 56h 0101 0101 /THRS1_1 W 57h 0101 0101 /THRS1_1 W 57h 0101 1001 /MA1 W 58h 0101 1000 //MA1 W 58h 0101 1100 //CC1_L R 50h 0101 1100 //CC1_H R 52h 0101 0100 //C1_H R 52h 0101 0000 /ST1_2 W 63h 0110 0000 /ST2_2 W 63h 0110 0000 /ST5_2 W 63h 0110 0000 /ST6_2 W 63h 0110 0001 /ST8_2 W 63h 0110 0101 /ST1_2 <th>Register Name</th> <th>Type Road/Write</th> <th>I²C</th> <th>Read/Write Address</th> | Register Name | Type Road/Write | I ² C | Read/Write Address |
|--|---|--------------------|------------------|-----------------------|
| /TIM2_1_L W 52h 0101 0011 /TIM1_1_L W 53h 0101 0011 /TIM1_1_H W 55h 0101 0101 /TIM2_2_1 W 56h 0101 0111 /THRS1_1 W 56h 0101 0011 /THRS1_1 W 57h 0101 0111 /Not used -fixed content R 58h 0101 1001 //KA1 W 59h 0101 1001 //KA1 W 58h 0101 1101 //RET1 W 58h 0101 1101 //C1_L R 55h 0101 0010 //S1_2_2 W 65h 0110 0001 //S1_2_2 W 65h 0110 0010 //S1_2_2 W 66h 0110 0010 //S1_2_2 W 66h 0110 0010 //S | | Reau/write | Hex | Binary |
| /TIM2_1_H W 53h 0101 0010 /TIM1_1_L W 54h 0101 0100 /TIM1_1_H W 55h 0101 0110 /TIRS2_1 W 55h 0101 0111 /TIRS1_1 W 57h 0101 0111 /TIRS1_1 W 57h 0101 0111 /NA1 W 57h 0101 0111 /NA1 W 58h 0101 1001 /SST1 W 58h 0101 1100 /SETT1 W 68h 0101 1110 /PPRP1 R 5Ch 0101 1100 /TC1_L R 5Ch 0101 1100 /TC1_H R 5Eh 0101 1100 /ST2_2 W 63h 0110 0000 /ST4_2 W 63h 0110 0010 /ST5_2 W 63h 0110 0101 /ST6_2 W 63h 0110 0101 /ST7_2 W 68h 0110 0101 /ST12_2 W | /TIM2_1_L | W | 52h | 0101 0010 |
| /TIM1_1_L W 54h 0101 0100 /THRS2 1 W 56h 0101 0111 /THRS1_1 W 57h 0101 0111 Not used - fixed content R 58h 0101 1001 //MA1 W 58h 0101 1001 //MA1 W 58h 0101 1001 //MA1 W 58h 0101 1001 //SETT1 W 58h 0101 1100 //SETT1 W 58h 0101 1101 //PPRP1 R 5Ch 0101 1100 //CLL R 5Dh 0101 1101 //CUTS1 R 5Fh 0101 1101 //ST3.2 W 62h 0110 0000 //ST4.2 W 68h 0110 0000 //ST6.2 W 68h 0110 0101 //ST7.2 W 66h 0110 0101 //ST8.2 W 67h 0110 0101 //ST8.2 W 68h 0110 0101 //ST16.2 <td>/TIM2_1_H</td> <td>W</td> <td>53h</td> <td>0101 0011</td> | /TIM2_1_H | W | 53h | 0101 0011 |
| //TIM1_1_H W 55h 0101_0101 /THRS1_1 W 57h 0104_0110 //THRS1_1 W 57h 0104_0110 //NA1 W 59h 0101_001 //SST1 W 59h 0101_1001 //MA1 W 58h 0101_1011 //SET11 W 58h 0101_1011 //PPRP1 R 5Ch 0101_1011 //CC1_L R 5Ch 0101_1011 //CC1_H R 5Ch 0101_10000 //ST2_2 W 60h 0110_00001 //ST4_2 W 63h 0110_0001 //ST5_2 W 65h 0110_0100 //ST6_2 W 66h 0110_0101 //ST8_2 W 66h 0110_0101 //ST8_2 W 66h 0110_0101 //ST8_2 W 66h 0110_0101 //ST1_2 W 66h 0110_0101 //ST1_2 <t< td=""><td>/TIM1_1_L</td><td>W</td><td>54h</td><td>0101 0100</td></t<> | /TIM1_1_L | W | 54h | 0101 0100 |
| //HRS2_1 W 56h 0101 0110 //HRS1_1 W 57h 0104 00114 Not used – fixed content R 58h 0101 1001 //KA1 W 58h 0101 1001 //MA1 W 58h 0101 1011 //PPRP1 R 56h 0101 1100 //TC1_L R 56h 0101 1100 //TC1_H R 56h 0101 1110 //UUTS1 R 57h 0101 0111 //JUUTS1 R 57h 0101 0111 //ST2_2 W 63h 0110 0001 //ST3_2 W 63h 0110 0001 //ST4_2 W 63h 0110 0001 //ST6_2 W 66h 0110 0010 //ST8_2 W 66h 0110 0100 //ST9_2 W 66h 0110 0101 //ST9_2 W 66h 0110 0101 //ST14_2 W 66h 0110 0101 //ST14_ | /TIM1_1_H | W | 55h | 0101 0101 |
| //THRS1_1 W 57h 01(0) 011000 //SA1 W 59h 01011001 //MA1 W 59h 01011001 //////////////////////////////////// | /THRS2_1 | W | 56h | 0101 0110 |
| Not used = fixed content R 58h 0101 1000 //MA1 W 5Ah 0101 1001 //SETT1 W 5Bh 0101 1010 //PPRP1 R 5Ch 0101 1101 //PPRP1 R 5Ch 0101 1101 //TC1_L R 5Ph 0101 1101 //OUTS1 R 5Ph 0101 1111 //ST1_2 W 60h 0110 0000 //ST3_2 W 62h 0110 0001 //ST4_2 W 62h 0110 0010 //ST5_2 W 63h 0110 0010 //ST4_2 W 63h 0110 0010 //ST5_2 W 66h 0110 0101 //ST6_2 W 66h 0110 0101 //ST8_2 W 66h 0110 1001 //ST10_2 W 66h 0110 1010 //ST11_2 W 66h 0110 1010 //ST14_2 W 62h 0110 1010 //ST14_ | /THRS1_1 | W | 57h | 0101 0111 |
| /SA1 W 59h C101 1001 //SETT1 W 6Bh O001 1011 //PPRP1 R 5Ch Ord1 1100 //C1_L R 5Dh O101 1101 //C1_L R 5Dh O101 1101 //C1_H R 5Fh O101 1101 //OUTS1 R 5Fh O101 0000 //ST1_2 W 60h O110 0000 //ST2_2 W 61h O110 0010 //ST4_2 W 63h O110 0010 //ST5_2 W 63h O110 0010 //ST6_2 W 66h 0110 0101 //ST6_2 W 66h 0110 0101 //ST7_2 W 66h 0110 1010 //ST1_2 W | Not used – fixed content | R | 58h | 0101 1000 |
| //MA1 W SAh Or01 1010 //PPRP1 R 5Ch Of01 1011 //PPRP1 R 5Ch Of01 1010 //TC1_L R 5Ch Of01 1100 //TC1_L R 5Ch Of01 1100 //CUTS1 R 5Fh Of01 100000 //ST2_2 W 60h Of10 0010 //ST3_2 W 62h Of10 0010 //ST4_2 W 63h Of10 0010 //ST4_2 W 63h Of10 0010 //ST6_2 W 66h Of10 0010 //ST8_2 W 66h Of10 0011 //ST8_2 W 66h Of10 0011 //ST8_2 W 66h Of10 0011 //ST12_2 W 66h Of10 0011 //ST14_2 W 66h Of10 0101 //ST14_2 W 66h Of10 1100 //ST14_2 W 66h Of10101100 //ST14_2 | /SA1 | W | 59h | 0101 1001 |
| /SETT1 W SBh 0.001 1100 //PPRP1 R 5Ch 0.001 1100 //TC1_L R 5Ch 0.001 1100 //TC1_H R 5Eh 0.001 1110 //OUTS1 R 5Fh 0.001 1117 //ST2_2 W 60h 0.010 0000 //ST3_2 W 62h 0.010 0010 //ST4_2 W 63h 0.010 0010 //ST6_2 W 63h 0.010 0010 //ST6_2 W 63h 0.010 0010 //ST6_2 W 66h 0.010 0010 //ST6_2 W 66h 0.010 0010 //ST6_2 W 66h 0.010 0010 //ST1_2 W 68h 0.010 0101 //ST1_2 W 68h 0.010 0101 //ST14_2 W 60h 0.010 1010 //ST14_2 W 60h 0.010 1010 //TIM2_2_H W 70h 0.0110 1000 // | /MA1 | W | 5Ah | 0101 1010 |
| /PPRP1 R 5Ch 0f01 1100 /TC1_H R 6Dh 0101 1101 /TC1_H R SEh 0101 1101 /ST12 W 60h 0110 0000 /ST2.2 W 61h 0110 0000 /ST3.2 W 62h 0110 0000 /ST4.2 W 63h 0110 0000 /ST5.2 W 63h 0110 0010 /ST6.2 W 63h 0110 0101 /ST5.2 W 63h 0110 0101 /ST7.2 W 66h 0110 0101 /ST8.2 W 65h 0110 0101 /ST8.2 W 66h 0110 1001 /ST12.2 W 68h 0110 1001 /ST14.2 W 68h 0110 1001 /ST14.2 W 68h 0110 1110 /ST16.2 W 66h 0110 1110 /ST16.2 W 67h 0110 1001 /TIM3.2 W | /SETT1 | W | 5Bh | 0101 1011 |
| Image: constraint of the system R Sph Ottol 1101 Image: constraint of the system R Sph Ottol 1110 Image: constraint of the system R Sph Ottol 1110 Image: constraint of the system R Sph Ottol 1110 Image: constraint of the system R Sph Ottol 1110 Image: constraint of the system R Sph Ottol 1110 Image: constraint of the system R Sph Ottol 000 Image: constraint of the system R Sph Ottol 000 Image: constraint of the system R Sph Ottol 000 Image: constraint of the system R Sph Ottol 000 Image: constraint of the system R Sph Ottol 000 Image: constraint of the system R Sph Ottol 000 Image: constraint of the system R Sph Ottol 000 Image: constraint of the system R Sph Ottol 000 Image: constraint of the system R Sph Ottol 000 | /PPRP1 | R | 5Ch | 0101 1100 |
| /TC1_H R SEh 0101 1110 /OUTS1 R SFh 0101 1117 /ST1_2 W 80h 0110 0000 /ST2_2 W 61h 0110 0000 /ST4_2 W 63h 0110 0001 /ST5_2 W 63h 0110 0011 /ST5_2 W 63h 0110 0101 /ST5_2 W 63h 0110 0101 /ST5_2 W 63h 0110 0101 /ST7_2 W 68h 0110 0101 /ST8_2 W 67h 0110 1001 /ST8_2 W 68h 0110 1001 /ST1_2 W 68h 0110 1001 /ST14_2 W 68h 0110 1011 /ST14_2 W 68h 0110 1011 /ST14_2 W 68h 0110 1011 /ST14_2 W 68h 0110 1010 /ST14_2 W 68h 0110 1010 /TIM4_2 W | /TC1_L | R | 5Dh | 0101 1101 |
| /OUTS1 R SFh 01011111 /ST1_2 W 60h 0110 0000 /ST2_2 W 61h 0110 0001 /ST3_2 W 62h 0110 0011 /ST5_2 W 63h 0110 0011 /ST5_2 W 63h 0110 0101 /ST6_2 W 66h 0110 0101 /ST7_2 W 66h 0110 0101 /ST8_2 W 67h 0110 0101 /ST8_2 W 66h 0110 1001 /ST1_2 W 66h 0110 1001 /ST11_2 W 66h 0110 1010 /ST14_2 W 68h 0110 1010 /ST14_2 W 68h 0110 1010 /ST14_2 W 61h 0110 1010 /ST14_2 W | /TC1_H | R | 5Eh | 0101 1110 |
| /ST1_2 W 60h 0110 0000 /ST2_2 W 61h 0110 0010 /ST3_2 W 63h 0110 0010 /ST4_2 W 63h 0110 0010 /ST6_2 W 63h 0110 0101 /ST6_2 W 66h 0110 0101 /ST7_2 W 66h 0110 0101 /ST8_2 W 67h 0110 0101 /ST8_2 W 68h 0110 1000 /ST1_2 W 68h 0110 1001 /ST1_2 W 68h 0110 1001 /ST1_2 W 68h 0110 1010 /ST1_2 W 68h 0110 1010 /ST1_2 W 68h 0110 1101 /ST1_2 W 68h 0110 1101 /ST1_2 W 68h 0110 1101 /ST1_2 W 70h 0111 1000 /ST1_2 W 70h 0111 1010 /ST1_2 W | /OUTS1 | R | 5Fh | 0101 1111 |
| /S12_2 W 61h 0110 0001 /ST3_2 W 62h 0110 0010 /ST5_2 W 63h 0110 0011 /ST6_2 W 65h 0110 0101 /ST6_2 W 66h 0110 0101 /ST7_2 W 66h 0110 0111 /ST8_2 W 67h 0110 0110 /ST9_2 W 68h 0110 1001 /ST12_2 W 68h 0110 1010 /ST12_2 W 68h 0110 1011 /ST12_2 W 68h 0110 1010 /ST12_2 W 68h 0110 1011 /ST12_2 W 68h 0110 1010 /ST14_2 W 60h 0110 1010 /ST14_2 W 60h 0110 1010 /ST16_2 W 67h 0111 0000 /TIM3_2 W 71h 0111 0000 /TIM3_2 W 73h 0111 0001 /TIM4_2_H W | /ST1_2 | W | 60h | 0110 0000 |
| /S13_2 W 62h 0110 0010 /ST4_2 W 63h 0110 0010 /ST5_2 W 64h 0110 0100 /ST6_2 W 66h 0110 0101 /ST7_2 W 66h 0110 1001 /ST9_2 W 66h 0110 1001 /ST12_2 W 68h 0110 1001 /ST12_2 W 66h 0110 1010 /ST13_2 W 66h 0110 1101 /ST14_2 W 66h 0110 1101 /ST16_2 W 66h 0110 1101 /ST16_2 W 66h 0110 1101 /ST16_2 W 71h 0111 0000 /TIM3_2 W 73h 0111 0010 /TIM2_2_H W 73h 0111 0010 /TIM3_2 W | /ST2_2 | W | 61h | 0110 0001 |
| /S14_2 W 63h 0110 0011 /ST5_2 W 64h 0110 0100 /ST6_2 W 65h 0110 0101 /ST7_2 W 66h 0110 0110 /ST8_2 W 67h 0110 0110 /ST9_2 W 68h 0110 1001 /ST10_2 W 68h 0110 1001 /ST12_2 W 68h 0110 1001 /ST14_2 W 70h 0111 0001 /TIM2_2 L W <td>/ST3_2</td> <td>W</td> <td>62h</td> <td>0110 0010</td> | /ST3_2 | W | 62h | 0110 0010 |
| /ST5_2 W 64h 01100100 /ST6_2 W 66h 01100101 /ST7_2 W 66h 01100110 /ST8_2 W 67h 01100111 /ST9_2 W 68h 01101000 /ST10_2 W 68h 01101000 /ST11_2 W 68h 01101010 /ST12_2 W 68h 01101010 /ST12_2 W 68h 01101010 /ST12_2 W 68h 01101010 /ST14_2 W 60h 01101101 /ST16_2 W 66h 01101111 /ST16_2 W 66h 01101111 /TIM3_2 W 70h 01110000 /TIM3_2 W 70h 01110010 /TIM2_2_L W 73h 01110011 /TIM2_2_W W 73h 01110010 /TIM2_2_W W 73h 01110010 /TIM2_2_W W 73h 01110011 /TIM2_2_W W 73h 011110101 <td>/ST4_2</td> <td>W</td> <td>63h</td> <td>0110 0011</td> | /ST4_2 | W | 63h | 0110 0011 |
| /ST6_2 W 66h 0110 0110 /ST7_2 W 66h 0110 0111 /ST8_2 W 67h 0410 0111 /ST9_2 W 68h 0110 1000 //ST10_2 W 68h 0110 1001 //ST11_2 W 68h 0110 1011 //ST12_2 W 68h 0110 1011 //ST12_2 W 68h 0110 1011 //ST12_2 W 68h 0110 1011 //ST14_2 W 68h 0110 1011 //ST15_2 W 66h 0110 1111 //ST16_2 W 67h 0111 0001 //TIM3_2 W 70h 0111 0001 //TIM3_2 W 70h 0111 0001 //TIM2_2_H W 73h 0111 0010 //TIM2_2_H W 73h 0111 0010 //THRS1_2 W 73h 0111 0010 //THRS2_2 W 78h 01111 000 //SA2 <td>/ST5_2</td> <td>W</td> <td>64h</td> <td>0110 0100</td> | /ST5_2 | W | 64h | 0110 0100 |
| /S17.2 W 66h 0110 0110 /ST8.2 W 67h 0110 0100 /ST10_2 W 68h 0110 1000 /ST11_2 W 68h 0110 1011 /ST12_2 W 68h 0110 1011 /ST12_2 W 6Ah 0110 1011 /ST12_2 W 6Bh 0110 1101 /ST12_2 W 6Bh 0110 1101 /ST13_2 W 6Ch 0110 1101 /ST14_2 W 6Dh 0110 1101 /ST15_2 W 6Ch 0110 1111 /ST16_2 W 70h 0111 0000 /TIM3_2 W 70h 0111 0000 /TIM3_2 W 72h 0111 0010 /TIM2_2_H W 72h 0111 0010 /TIM3_2 P W 76h 0111 0110 /THRS1 2 W 77h 0111 0010 /THRS2 2 W 76h 01111 0010 /THRS2 2 | /ST6_2 | W | 65h | 0110 0101 |
| /S18_2 W 67h 01100111 /ST9_2 W 68h 01101000 /ST10_2 W 69h 01101001 /ST11_2 W 6Ah 01101010 /ST12_2 W 6Ah 01101010 /ST12_2 W 6Ah 01101010 /ST3_2 W 6Ch 01101101 /ST16_2 W 6Ch 01101101 /ST16_2 W 6Ch 01101101 /ST16_2 W 6Ch 01101101 /ST16_2 W 6Ch 01101101 /TIM4_2 W 70h 01110000 /TIM2_2_L W 70h 01110010 /TIM2_2_H W 73h 01110101 /TIM2_2_H W 73h 01110100 /TIM2_2_H W 73h 01110101 /THRS1_2 W 73h 01110101 /THRS2_2 W 73h 011110101 /THRS2_2 W | /S17_2 | W | 66h | 0110 0110 |
| /S19.2 W 68h 01101000 /ST10_2 W 69h 01101001 /ST11_2 W 6Ah 01101010 /ST12_2 W 6Bh 01101011 /ST13_2 W 6Bh 01101011 /ST13_2 W 6Bh 01101101 /ST13_2 W 6Ch 01101101 /ST15_2 W 6Ch 01101101 /ST16_2 W 6Fh 01101111 /ST16_2 W 6Fh 01101000 /TIM3_2 W 70h 01110000 /TIM3_2 W 70h 01110000 /TIM3_2 W 70h 01110000 /TIM3_2 W 73h 01110010 /TIM2_2_H W 73h 01110010 /TIM3_2 W 76h 01110100 /TIM3_2_W W 76h 01110100 /TIM2_2_H W 76h 01110101 /THRS2_2 W 76h 01111010 /THRS2_W W 78h 01111000 <td>/ST8_2</td> <td>W</td> <td>67h</td> <td>0110 0111</td> | /ST8_2 | W | 67h | 0110 0111 |
| /S110_2 W 69h 0110 1001 /ST11_2 W 6Ah 0110 1010 /ST12_2 W 6Bh 0110 1011 /ST3_2 W 6Ch 0110 1010 /ST14_2 W 6Ch 0110 1100 /ST15_2 W 6Ch 0110 1111 /ST16_2 W 6Fh 0110 1111 /ST16_2 W 6Fh 0110 000 /TIM2_2_L W 70h 0111 0000 /TIM2_2_L W 72h 0111 0010 /TIM2_2_H W 72h 0111 0010 /TIM2_2_H W 73h 0111 0010 /TIM2_2_H W 76h 0111 0100 /TIM2_2_H W 76h 0111 0101 /THRS2_2 W 78h 0111 1010 /THRS2_2 W 78h 0111 1001 /SET2 W 78h </td <td>/ST9_2</td> <td>W</td> <td>68h</td> <td>0110 1000</td> | /ST9_2 | W | 68h | 0110 1000 |
| /S111_2 W 6Ah 0110 1010 /ST12_2 W 6Bh 0110 1011 /ST13_2 W 6Ch 0110 1100 /ST14_Z W 6Ch 0110 1101 /ST15_Z W 6Ch 0110 1101 /ST16_2 W 6Eh 0110 1111 //ST16_2 W 6Fh 0110 1111 //TIM2_2_L W 70h 0111 0010 /TIM2_2_L W 72h 0111 0010 /TIM2_2_H W 73h 0111 0010 /TIM2_2_H W 76h 0111 0101 /THRS2_2 W 76h 0111 0101 /THRS2_2 W 76h 0111 0101 /THRS2_2 W 78h 0111 1001 //SA2 W 78 | /S110_2 | W | 69h | 0110 1001 |
| /S112_2 W 6Bh 0110 1011 /ST13_2 W 6Ch 0110 1100 /ST14_2 W 6Dh 0110 1101 /ST15_2 W 6Eh 0110 1111 //ST16_2 W 6Eh 0110 1111 //TIM4_2 W 70h 0111 0000 /TIM3_2 W 70h 0111 0001 //TIM2_2_L W 72h 0111 0010 //TIM2_2_H W 73h 0111 0010 //TIM2_2_H W 73h 0111 0101 //TIM1_2_H W 73h 0111 0101 //TIM2_2 W 76h 0111 0110 //TIM2_2_H W 77h 0111 0101 //TIM2_2_H W 78h 0111 0101 //TIM2_2_H W 78h 0111 0101 //THRS1_2 W 78h 0111 0101 //THRS1_2 W 78h 0111 1010 //THRS1_2 W 78h 0111 1010 //EA2 W 78h 0111 1010 //SA2 W | /SI11_2 | W | 6Ah | 0110 1010 |
| /S113 2 W 6Ch 0110 1100 /ST14_2 W 6Dh 0110 1101 /ST15 2 W 6Eh 0110 1110 /ST16_2 W 6Eh 0110 1110 /ST16_2 W 6Eh 0110 1110 /TIM2_2 W 70h 0111 0000 /TIM3_2 W 70h 0111 0000 /TIM2_2_H W 72h 0111 0010 /TIM1_2_H W 73h 0111 0010 /TIM1_2_H W 73h 0111 0100 /TIM1_2_H W 75h 0111 0101 /THR52_2 W 76h 01110 100 /THR52_2 W 76h 0111 0101 /THR52_2 W 76h 0111 010 /THR51_2 W 77h 0111 0101 /THR52_2 W 78h 0111 1000 /THR52_2 W 78h 0111 1000 /THR52_2 W 78h 01111 1000 /SA2 | /S112_2 | VV | 6Bh | 0110 1011 |
| /S114_2 W 6Dn 0110 1101 /ST15_2 W 6Eh 0110 1110 /ST16_2 W 6Fh 0110 1110 //TIM2_2 W 70h 0111 0000 //TIM2_2_L W 70h 0111 0010 //TIM2_2_L W 72h 0111 0010 //TIM2_2_H W 73h 0111 0010 //TIM1_2_H W 73h 0111 0010 //THRS2_2 W 76h 0111 0101 //THRS1_2 W 76h 0111 0101 //THRS1_2 W 78h 0111 1010 //AA2 W 78h 0111 1010 //AA2 W 78h 0111 1010 //MA2 W 78h 0111 1001 //MA2 W 78h 0111 1001 //PPRP2 R 7Ch 0111 1100 //C2_L R 7Dh 0111 1101 //C2_L R 7Dh 0111 1101 | /5113_2 | VV | 6Ch | 0110 1100 |
| /S115_2 W 6Eh 0110 1110 /ST16_2 W 6Fh 0110 1111 /TIM4_2 W 70h 0111 0000 /TIM2_2_L W 71h 0111 0010 /TIM2_2_L W 72h 0111 0010 /TIM2_2_H W 73h 0111 0010 /TIM1_2_L W 73h 0111 0101 /TIM1_2_H W 73h 0111 0101 /THRS2_2 W 76h 0111 0101 /THRS1_2 W 77h 0111 0101 /THRS2_2 W 78h 0111 1010 /THRS2_2 W 78h 0111 1010 /THRS1_2 W 77h 0111 1010 /MA2 W 7Ah 0111 1001 /SETT2 W 78h 0111 1001 /PPRP2 R 7Ch 0111 1100 /TC2_L R 7Dh 0111 1101 /TC2_L R 7Eh 0111 1110 | /S114_2 | VV | 6Dh | 0110 1101 |
| /S116_2 W 6Fh 011011111 /TIM4_2 W 70h 0111 0000 /TIM3_2 W 71h 0111 0010 /TIM2_2_L W 72h 0111 0010 /TIM2_2_H W 73h 0111 0010 /TIM2_2_H W 73h 0111 0011 /TIM1_2_H W 73h 0111 0100 /TIM1_2_H W 75h 0111 0101 /THRS2_2 W 76h 0111 0101 /THRS1_2 W 77h 0111 0101 /THRS1_2 W 77h 0111 1010 /ZS2 W 78h 0111 1010 /ZHRS2 W 78h 01111 1010 /ZEL <t< td=""><td>/\$115_2</td><td>VV</td><td>6Eh</td><td>0110 1110</td></t<> | /\$115_2 | VV | 6Eh | 0110 1110 |
| Image: Nime_2 W 70h 0111 0000 7TIM3_2 W 71h 0111 0001 7TIM2_2_L W 72h 0111 0010 7TIM2_2_H W 73h 0111 0010 7TIM2_2_H W 73h 0111 0010 7TIM2_2_H W 73h 0111 0011 7TIM1_2_H W 73h 0111 0100 7THRS2_2 W 76h 0111 0101 7THRS1_2 W 77h 0111 0101 7SA2 W 78h 0111 1000 7SA2 W 78h 0111 1000 7SETT2 W 78h 0111 1001 7FC2_L R 7Ch 0111 1010 7FC2_L R 7Ch 0111 1101 7FC2_L R 7Dh 0111 1101 | /5116_2 | VV | 6FN 705 | 0110 1111 |
| Image: Normal Sector Image: No | //IIM4_2 | | 70n | 0111 0000 |
| //IIM2_2_L W 72n 0111 0010 /TIM2_2_H W 73h 0111 0011 /TIM2_2_H W 74h 0111 0101 /TIM1_2_H W 74h 0111 0101 /THRS2_2 W 76h 0111 0101 /THRS1_2 W 76h 0111 0101 /DES2 W 78h 0111 1000 /SA2 W 78h 0111 1001 /MA2 W 78h 0111 1001 /SETT2 W 78h 0111 1010 /PPRP2 R 7Ch 0111 1010 //TC2_L R 7Dh 0111 1010 | | VV VV | 710 | 0111 0001 |
| Viiii Viiiii Viiii Viiiii Viiii Viiii < | /11M2_2_L | VV VV | 72h | 0111 0010 |
| Imm_2_L vv 74n 0111 0100 /TIMI_2_H W 75h 0111 0101 /THRS2_2 W 76h 0111 0101 /THRS1_2 W 76h 0111 0101 /THRS1_2 W 77h 0111 0101 /DES2 W 78h 0111 1000 /SA2 W 79h 0111 1001 /MA2 W 7Ah 0111 1001 /SETT2 W 78h 0111 1011 /PPRP2 R 7Ch 0111 1011 /PC2_L R 7Dh 0111 1101 /TC2_L R 7Eh 0111 1110 //TC2_H R 7Eh 0111 1110 | | VV \\/ | 74h | 0111 0100 |
| VIIINT_2_1V VV 7311 0111 0101 /THRS2_2 W 76h 0111 0110 /THRS1_2 W 77h 0111 0111 /DES2 W 78h 0111 1000 /SA2 W 78h 0111 1001 /MA2 W 78h 0111 1001 /SETT2 W 78h 0111 1010 /PPRP2 R 7Ch 0111 1010 /TC2_L R 7Dh 0111 1110 /TC2_H R 7Eh 0111 1110 | | VV \\/ | 7411 75b | 0111 0100 |
| VITHNS2_2 VV 76h 0111 0110 VTHRS1_2 W 77h 0111 0111 VDES2 W 78h 0111 1000 VSA2 W 79h 0111 1001 VMA2 W 78h 0111 1001 VMA2 W 78h 0111 1010 V/MA2 W 78h 0111 1010 V/PRP2 R 7Ch 0111 1101 //PPRP2 R 7Ch 0111 1101 //TC2_L R 7Eh 0111 1110 //TC2_H R 7Eh 0111 1110 | | VV \\/ | 70H | 0111 0101 |
| View View <th< td=""><td></td><td><u>۷۷</u> ۱۸/</td><td>7011</td><td>0111 0111</td></th<> | | <u>۷۷</u> ۱۸/ | 7011 | 0111 0111 |
| VV 7611 0111 1000 /SA2 W 79h 0111 1001 /MA2 W 7Ah 0111 1010 /SETT2 W 7Bh 0111 1010 /PPRP2 R 7Ch 0111 1100 /TC2_L R 7Dh 0111 1101 /TC2_H R 7Eh 0111 1110 | | ۷۷ ۱۸/ | 726 | 0111 1000 |
| Image: Weight of the second | /0632 | V V \// | 70h | 0111 1000 |
| Mr2 W 72h1 0111 1010 /SETT2 W 7Bh 0111 1011 /PPRP2 R 7Ch 0111 1100 /TC2_L R 7Dh 0111 1101 /TC2_H R 7Eh 0111 1110 | /ΜΔ2 | \// | 74h | 0111 1010 |
| //PRP2 R 7Ch 0111 1011 //PPRP2 R 7Ch 0111 1100 /TC2_L R 7Dh 0111 1101 /TC2_H R 7Eh 0111 1110 //UTS2 R 7Eh 0111 1111 | //V/C2 /SETT2 | \// | 7Rh | 0111 1010 |
| /TC2_L R 7Dh 0111 1101 /TC2_H R 7Eh 0111 1110 /TC2_H R 7Eh 0111 1110 | /PPRP2 | R | 7Ch | 0111 1100 |
| /TC2_H R 7Eh 0111 1110 //OLTS2 R 7Eh 0111 1111 | /////////////////////////////////////// | R | 7Dh | 0111 1101 |
| //OLTS2 R 7Eb 0111111 | /тс.2 н | R | 7Eh | 0111 1110 |
| | /0///////////////////////////////////// | R | 7Eh | 0111 1111 |

Notes:

1. Reserved registers should not be written to.



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KXCNL Register Descriptions

Information registers

/INFO1

This register can be used for optional supplier information.

| R | R | R | R | R | R | R | R | |
|------|------|------|------|------|------|------------------------|----------|-------------|
| Х | Х | Х | Х | Х | Х | Х | X | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | ľ | ² C Addres: | s: 0x0Dh | |

/INFO2

A second register can be used for optional supplier information.

| R | R | R | R | R | R | R | R | |
|------|------|------|------|------|------|------------------------|---------|-------------|
| Х | Х | Х | Х | Х | Х | X | X | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | | ² C Address | : 0x0Eh | |

/WIA

This register can be used for supplier recognition (Who I Am ID), as it can be factory written to a known byte value. The default value is 0x0Bh.

| R | R | R | R | R | R | R | R | |
|------|------|------|------|------|------|-------------------------|-------|-------------|
| WIA7 | WIA6 | WIA5 | WIA4 | WIA3 | WIA2 | WIA1 | WIA0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00001011 |
| | | | | | ľ | ² C Address: | 0x0Fh | |

Accelerometer Outputs

These registers contain up to 12-bits of valid acceleration data for each axis. The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per Table 8 below. If /**CNTL1**, **DEBUG** == 0, data is used for State Programs. If /**CNTL1**, **DEBUG** == 1, data is not fed to State Programs. Data is provided as a signed value (upper part of MSB is sign adjusted) in little Endian form.

| 12-bit Data | Range = +/-2g | Range = +/-4g | Range = +/-6g | Range = +/-8g |
|----------------|---------------|---------------|---------------|---------------|
| 0111 1111 1111 | +1.999g | +3.998g | +5.997g | +7.996g |
| 0111 1111 1110 | +1.998g | +3.996g | +5.994g | +7.992g |
| | | | | |
| 0000 0000 0001 | +0.001g | +0.002g | +0.003g | +0.004g |
| 0000 0000 0000 | 0.000g | 0.000g | 0.000g | 0.000g |
| 1111 1111 1111 | -0.001g | -0.002g | -0.003g | -0.004g |
| | | | | |



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| 12-bit Data | Range = +/-2g | Range = +/-4g | Range = +/-6g | Range = +/-8g |
|----------------|---------------|---------------|---------------|---------------|
| 1000 0000 0001 | -1.999g | -3.998g | -5.997g | -7.996g |
| 1000 0000 0000 | -2.000g | -4.000g | -6.000g | -8.000g |

Table 8. Acceleration (g) Calculation

/OUTX_L

X-axis accelerometer output least significant byte

| R | R | R | R | R | R | R | R |
|--------|--------|--------|--------|--------|--------|------------|--------|
| XOUTD7 | XOUTD6 | XOUTD5 | XOUTD4 | XOUTD3 | XOUTD2 | XOUTD1 | XOUTD0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | | C Addross: | 0v10h |

/OUTX_H

X-axis accelerometer output most significant byte

| R | R | R | R | R | R | R | R |
|---------|---------|---------|---------|---------|---------|-----------|--------|
| XOUTD11 | XOUTD11 | XOUTD11 | XOUTD11 | XOUTD11 | XOUTD10 | XOUTD9 | XOUTD8 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | 12 | C Address | 0v11h |

/OUTY_L

Y-axis accelerometer output least significant byte

| R | R | R | R | R | R | R | R |
|--------|--------|--------|--------|--------|--------------|-------------------------|--------|
| YOUTD7 | YOUTD6 | YOUTD5 | YOUTD4 | YOUTD3 | YOUTD2 | YOUTD1 | YOUTD0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | ² | ² C Address: | 0x12h |

/OUTY_H

Y-axis accelerometer output most significant byte

| R | R | R | R | R | R | R | R |
|---------|---------|---------|---------|---------|----------------|------------|--------|
| YOUTD11 | YOUTD11 | YOUTD11 | YOUTD11 | YOUTD11 | YOUTD10 | YOUTD9 | YOUTD8 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| • | | | | | l ² | C Address: | 0x13h |

/OUTZ_L

Z-axis accelerometer output least significant byte

| R | R | R | R | R | R | R | R |
|--------|--------|--------|--------|--------|--------|-------------------------|--------|
| ZOUTD7 | ZOUTD6 | ZOUTD5 | ZOUTD4 | ZOUTD3 | ZOUTD2 | ZOUTD1 | ZOUTD0 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | ľ | ² C Address: | 0x14h |



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/OUTZ_H

Z-axis accelerometer output most significant byte

| R | R | R | R | R | R | R | R |
|---------|---------|---------|---------|---------|--------------|------------|--------|
| ZOUTD11 | ZOUTD11 | ZOUTD11 | ZOUTD11 | ZOUTD11 | ZOUTD10 | ZOUTD9 | ZOUTD8 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | ² | C Address: | 0x15h |

Long Counter

These two registers contain up to 16-bits of long counter information.

/LC_L

Long counter least significant byte

| R | R | R | R | R | R | R | R | |
|------|------|------|------|------|------|------|------|-------------|
| LC7 | LC6 | LC5 | LC4 | LC3 | LC2 | LC1 | LC0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 11111111 |
| | | | | | | 2 | | |

C Address: 0x16h

/LC H

Long counter most significant byte

| R | R | R | R | Ŕ | R | R | R | |
|------|------|------|------|------|------|-------------------------|-------|-------------|
| LC15 | LC14 | LC13 | LC12 | LC11 | LC10 | LC9 | LC8 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 11111111 |
| | | | | | ľ | ² C Address: | 0x17h | |

/LC counter = -01h, Status: /LC is not valid, counting stopped Status: /LC counter is full, interrupt happens and -01h will be set to counter /LC counter = 00h, /LC counter > 00h,

Status: /LC counting

Reading of the /LC counter resets the /STAT, LONG flag to default (0).



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/STAT

This register reports the status of the accelerometer output.

| R | R | R | R | R | R | R | R | |
|------|-------|-------|-------|---------|--------------|------------|-------|-------------|
| LONG | SYNCW | SYNC1 | SYNC2 | INT_SM1 | INT_SM2 | DOR | DRDY | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | ² | C Address: | 0x18h | |

LONG is the long counter interrupt and is common to both State Programs. Reset to default value by reading /LC register.

LONG = 0 - no interrupt

LONG = 1 – Long Counter /LC interrupt flag

SYNCW provides common information for OUTW host action waiting. Reset to default value when OUTSy register (State Program 1 or 2) is read. SYNCW = 0 – no actions are waiting from the Host

SYNCW = 1 - Host action is waiting after OUTW command.

SYNC1 reports the synchronization status of State Program 1.

SYNC1 = 0 – State Program 1 running normally.

SYNC1 = 1 – State Program 1 stopped and waiting for restart request from State Program 2.

SYNC2 reports the synchronization status of State Program 2.

SYNC2 = 0 - State Program 2 running normally.

SYNC2 = 1 – State Program 2 stopped and waiting for restart request from State Program 1.

INT_SM1 reports the interrupt status of State Program 1. Interrupt infomation is released/reset when /OUTS1 register read.

 $INT_SM1 = 0 - No$ State Program 1 interrupt.

INT_SM1 = 1 – State Program 1 interrupt.

INT_SM2 reports the interrupt status of State Program 2. Interrupt infomation is released/reset when /OUTS2 register read. INT_SM2 = 0 - No State Program 2 interrupt. INT_SM2 = 1 - State Program 2 interrupt.

DOR reports a data overrun condition when the stream data is not read from the output registers before the next data samples are starting to be measured. This data overrun bit is reset when the next sample is ready.
DOR = 0 - No data overrun.
DOR = 1 - Data overrun.

DRDY reports the data ready condition of the streaming data. DRDY = 0 - Data not ready. DRDY = 1 - Data ready.



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/PEAK1

Peak detector value for Next condition of State Program 1. State Program 1 stores the highest/lowest peak data value to this register. /PEAK1 value is reset when REL command occurs or new initial start occurs.

| R | R | R | R | R | R | R | R | |
|---------|---------|---------|---------|---------|--------------|-----------|---------|-------------|
| PEAK1_7 | PEAK1_6 | PEAK1_5 | PEAK1_4 | PEAK1_3 | PEAK1_2 | PEAK1_1 | PEAK1_0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | ² | C Address | 0x19h | |

/PEAK2

Peak detector value for Next condition of State Program 2. State Program 2 stores the highest/lowest peak data value to this register. /PEAK2 value is reset when REL command occurs or new initial start occurs.

| R | R | R | R | R | R | R | R | |
|---------|---------|---------|---------|---------|---------|-----------|---------|-------------|
| PEAK2_7 | PEAK2_6 | PEAK2_5 | PEAK2_4 | PEAK2_3 | PEAK2_2 | PEAK2_1 | PEAK2_0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | C Address | 0x1Ah | |

/CNTL1

Read/write control register that controls the main feature set.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|------|------|------|-------|-------|-------|-------------------------|-------|-------------|
| PC | SC_1 | SC_0 | ODR_2 | ODR_1 | ODR_0 | DEBUG | IEN | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00010100 |
| | | | | | ľ | ² C Address: | 0x1Bh | |

PC controls the operating mode of the KXCNL.

PC = 0 - stand-by mode

PC = 1 - operating (active) mode

SC_1, SC_0 sets the g-range for the accelerometer outputs per Table 12. The default g-range is 2 g.

| SC_1 | SC_0 | g-range |
|------|------|---------|
| 0 | 0 | 2 g |
| 0 | 1 | 4 g |
| 1 | 0 | 6 g |
| 1 | 1 | 8 g |

Table 12. g-range

ODR_2, ODR_1, ODR_0 sets the output data rate for the accelerometer outputs per Table 12. The default ODR is 100Hz.



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| Name | ODR_2 | ODR_1 | ODR_0 | Output Data Rate | Filter cf |
|------|-------|-------|-------|------------------|-----------|
| ODR0 | 0 | 0 | 0 | 3.125 Hz | None |
| ODR1 | 0 | 0 | 1 | 6.25 Hz | None |
| ODR2 | 0 | 1 | 0 | 12.5 Hz | None |
| ODR3 | 0 | 1 | 1 | 25 Hz | None |
| ODR4 | 1 | 0 | 0 | 50 Hz | None |
| ODR5 | 1 | 0 | 1 | 100 Hz | 50 Hz |
| ODR6 | 1 | 1 | 0 | 400 Hz | 200 Hz |
| ODR7 | 1 | 1 | 1 | 1600 Hz | 800 Hz |

Table 12. Output Data Rate

DEBUG controls the State Program Step Debug mode of the KXCNL. DEBUG = 0 – normal operation of State Programs with /OUTX, /OUTY, and /OUTZ stream data registers are fed to State Programs.

DEBUG = 1 – debug stepping of State Programs with /OUTX, /OUTY, and /OUTZ stream data registers <u>not</u> fed to State Programs. Debug inputs are fetched from /X, Y, Z_DEBUG registers. One step of the State Programs is processed with the write of /Z_DEBUG.

IEN is the main interrupt enable switch to allow State Programs to route interrupts to INT1/DRDY and INT2 pads.

IEN = 0 - physical interrupts disabled.IEN = 1 - physical interrupts enabled.

/CNTL2

Read/write control register that controls the State Program 1.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---------|---------|---------|------|---------|------|-------------------------|--------|-------------|
| HYST2_1 | HYST1_1 | HYST0_1 | 0 | SM1_PIN | 0 | 0 | SM1_EN | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | ľ | ² C Address: | 0x1Ch | |

HYST2_1, HYST1_1, HYST0_1 sets the (unsigned) hysteresis limit which is added or subtracted from the threshold value in State Program 1.

000 = 0 LSB (default)

111 = 7 LSB (maximum hysteresis)

SM1_PIN controls the routing of the State Program 1 interrupt. SM1_PIN = 0 – State Program 1 interrupt routed to INT1 SM1_PIN = 1 – State Program 1 interrupt routed to INT2

SM1_EN enables State Program 1. Changing this bit from a 0 to a 1 initiates State Program 1. State Program 1 can control this bit according to the program code.



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SM1_EN = 0 – State Program 1 disabled. All State Program 1 related temporary memories and registers are left intact.

SM1_EN = 1 – State Program 1 enabled. Default Initial Start-task of State Program 1 is started.

/CNTL3

Read/write control register that controls the State Program 2.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|---------|---------|---------|------|---------|------|------------------------|----------|-------------|
| HYST2_2 | HYST1_2 | HYST0_2 | 0 | SM2_PIN | 0 | 0 | SM2_EN | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | ĺ | ² C Address | s: 0x1Dh | |

HYST2_2, HYST1_2, HYST0_2 sets the (unsigned) hysteresis limit which is added or subtracted from the threshold value in State Program 2.

000 = 0 LSB (default)

111 = 7 LSB (maximum hysteresis)

SM2_PIN controls the routing of the State Program 2 interrupt.

SM2_PIN = 0 – State Program 2 interrupt routed to INT1

SM2_PIN = 1 – State Program 2 interrupt routed to INT2

SM2_EN enables State Program 2. Changing this bit from a 0 to a 1 initiates State Program 2. State Program 2 can control this bit according to the program code.
 SM2_EN = 0 – State Program 2 disabled. All State Program 2 related temporary memories and registers are left intact.

SM2_EN = 1 – State Program 2 enabled. Default Initial Start-task of State Program 2 is started.

/CNTL4

Read/write control register that controls several functions of the KXCNL.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|-------|------|------|---------|---------|--------------|-------------------------|-------|-------------|
| DR_EN | IEA | IEL | INT2_EN | INT1_EN | VFILT | STP | STRT | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | ² | ² C Address: | 0x1Eh | |

DR_EN sends the data ready signal (DRDY) to the INT1 pin.

 $DR_EN = 0$ Data Ready signal is <u>not</u> connected to INT1. $DR_EN = 1$ Data Ready signal is connected to INT1 and overrides any other interrupt settings.

IEA controls the polarity of interrupt signals. IEA = 0 - Interrupt signals active LOW.



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IEA = 1 – Interrupt signals active HIGH.

IEL controls the latching state of interrupt signals. IEA = 0 - Interrupt signals are latched. IEA = 1 - Interrupt signals are pulsed.

INT2_EN enables the INT2 pin.

INT2_EN = 0 – INT2 signal disabled. INT2 pin in high-Z state.
INT2_EN = 1 – INT2 signal enabled and signal is fully functional. \CNTL1, IEN must be taken into account also.

INT1_EN enables the INT1/DRDY pin.

INT1_EN = 0 – INT1/DRDY signal disabled. INT1/DRDY pin in high-Z state.
INT1_EN = 1 – INT1/DRDY signal enabled and signal is fully functional. \CNTL1, IEN or /CNTL4, DR_EN must be taken into account also.

VFILT enables or disables the Vector Filter. VFILT = 0 - Vector filter disabled.VFILT = 1 - Vector filter enabled.

STP controls the activation of self test. STP = 0 - Normal operation with no Self Test effect.STP = 1 - Positive Self Test effect.

STRT performs a Soft Reset of the KXCNL if set to a 1. Similar to POR, defaults for registers are loaded from internal memory. Once the reset is complete, this bit is set to 0.

/THRS3

Read/write register that contains the common threshold for overrun detection. This threshold is always unsigned (abs) regardless of /SETTy, ABS settings and is common to both State Programs. If any axis value exceeds /THRS3 limit (regardless /TAMxAy status), then the RESET action (/PPy=/RPy) and the RESET Initial Start task immediately occur.

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |
|---------|---------|---------|---------|---------|--------------|-------------------------|---------|-------------|--|
| THRS3_7 | THRS3_6 | THRS3_5 | THRS3_4 | THRS3_3 | THRS3_2 | THRS3_1 | THRS3_0 | Reset Value | |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 | |
| | | | | | ² | ² C Address: | 0x1Fh | | |

Offset correction

The following three registers contain up to 8-bits of offset correction for each axis. Because there are typically offset drifts after solder reflow, there is sometimes a need to zero or normalize the outputs for better application performance. These signed offset correction values are multiplied by 2 and subtracted from the outputs provided to the State Programs and to the streaming 12-bit data registers.



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/OFF_X

X-axis accelerometer offset correction

| R/W | R/W | |
|--------|--------|--------|--------|--------|--------|-------------------------|--------|-------------|
| OFF_X7 | OFF_X6 | OFF_X5 | OFF_X4 | OFF_X3 | OFF_X2 | OFF_X1 | OFF_X0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | 2 | ² C Address: | 0x20h | |

/OFF_Y

Y-axis accelerometer offset correction

| R/W | R/W | |
|--------|--------|--------|--------|--------|--------|-----------|--------|-------------|
| OFF_Y7 | OFF_Y6 | OFF_Y5 | OFF_Y4 | OFF_Y3 | OFF_Y2 | OFF_Y1 | OFF_Y0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | C Address | 0y21h | |

/OFF_Z

Z-axis accelerometer offset correction

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|--------|--------|--------|--------|--------|------------|--------|--------|-------------|
| OFF_Z7 | OFF_Z6 | OFF_Z5 | OFF_Z4 | OFF_Z3 | OFF_Z2 | OFF_Z1 | OFF_Z0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | C Address. | 0v22h | | |

Constant Shift

The following three registers contain up to 8-bits of constant shift data for each axis. The constant shift acts like a temporary offset shift and is used for the DIFF function available only inside State Program 2.

/CS_X

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X-axis accelerometer constant shift

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|-------|-------|-------|-------|-------|--------------|------------|-------|-------------|
| CS_X7 | CS_X6 | CS_X5 | CS_X4 | CS_X3 | CS_X2 | CS_X1 | CS_X0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| Ŧ | | | | | ² | C Address: | 0x24h | |



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| /CS_Y | |
|-------|--|
|-------|--|

Y-axis accelerometer constant shift

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|-------|-------|-------|-------|-------|--------------|-------------------------|-------|-------------|
| CS_Y7 | CS_Y6 | CS_Y5 | CS_Y4 | CS_Y3 | CS_Y2 | CS_Y1 | CS_Y0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | ² | ² C Address: | 0x25h | |

/CS_Z

Z-axis accelerometer constant shift

| R/W | R/W | |
|-------|-------|-------|-------|-------|-------|------------|-------|-------------|
| CS_Z7 | CS_Z6 | CS_Z5 | CS_Z4 | CS_Z3 | CS_Z2 | CS_Z1 | CS_Z0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | C Address: | 0x26h | |

Debug input

The following three registers contain 8-bits of debug input data for each axis. If /CNTL1, DEBUG == 1, data from these registers is fed to the State Programs when /OUTSx is read (as step command).

/X_DEBUG

X-axis accelerometer debug input

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|----------|----------|----------|---------|----------|----------|-------------------------|----------|-------------|
| X_DEBUG7 | X_DEBUG6 | X_DEBUG5 | _DEBUG4 | X_DEBUG3 | X_DEBUG2 | X_DEBUG1 | X_DEBUG0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | I | ² C Address: | 0x28h | |

/Y_DEBUG

Y-axis accelerometer debug input

| R/W | R/W | |
|----------|----------|----------|----------|----------|----------|-------------------------|----------|-------------|
| Y_DEBUG7 | Y_DEBUG6 | Y_DEBUG5 | Y_DEBUG4 | Y_DEBUG3 | Y_DEBUG2 | Y_DEBUG1 | Y_DEBUG0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | I | ² C Address: | 0x29h | |

/Z_DEBUG

Z-axis accelerometer debug input

| R/W | R/W | |
|----------|----------|----------|----------|----------|----------|-------------------------|----------|-------------|
| Z_DEBUG7 | Z_DEBUG6 | Z_DEBUG5 | Z_DEBUG4 | Z_DEBUG3 | Z_DEBUG2 | Z_DEBUG1 | Z_DEBUG0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | ľ | ² C Address: | 0x2Ah | |



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Vector filter coefficients

Total acceleration vector length is calculated with an approximation formula. The calculated vector length result is filtered with an adjustable band pass filter. The following four registers contain 8-bit vector filter coefficients.

/VFC_1

Vector calculation filter coefficient 1

| R/W | R/W | |
|--------|--------|--------|--------|--------|--------|------------|--------|-------------|
| VFC1_7 | VFC1_6 | VFC1_5 | VFC1_4 | VFC1_3 | VFC1_2 | VFC1_1 | VFC1_0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | C Address: | 0x2Ch | |

/VFC_2

Vector calculation filter coefficient 2

| R/W | R/W | |
|--------|--------|--------|--------|--------|--------|-----------|--------|-------------|
| VFC2_7 | VFC2_6 | VFC2_5 | VFC2_4 | VFC2_3 | VFC2_2 | VFC2_1 | VFC2_0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |
| | | | | | | C Address | 0v2Dh | |

/VFC_3

Vector calculation filter coefficient 3

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|--------|--------|--------|--------|--------|----------------|------------|--------|-------------|
| VFC3_7 | VFC3_6 | VFC3_5 | VFC3_4 | VFC3_3 | VFC3_2 | VFC3_1 | VFC3_0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | l ² | C Address: | 0x2Eh | |

/VFC_4

Vector calculation filter coefficient 4

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
|--------|--------|--------|--------|--------|--------------|-------------------------|--------|-------------|
| VFC4_7 | VFC4_6 | VFC4_5 | VFC4_4 | VFC4_3 | VFC4_2 | VFC4_1 | VFC4_0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| * | | | | | ² | ² C Address: | 0x2Fh | |



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State Program 1

The following 32 registers pertain to State Program 1. They contain the program code, timers, thresholds, masks, settings, and outputs.

| Register Name | I ² C Address | Read/Write | Name | Description |
|----------------|--------------------------|------------|-------------|--|
| /ST1_1 | 0x40 | -/VV | Step 1 | code |
| /ST2_1 | 0x41 | -/W | Step 2 | code |
| /ST3_1 | 0x42 | -/W | Step 3 | code |
| /ST4_1 | 0x43 | -/VV | Step 4 | code |
| /ST5_1 | 0x44 | -/VV | Step 5 | code |
| /ST6_1 | 0x45 | -/VV | Step 6 | code |
| /ST7_1 | 0x46 | -/W | Step 7 | code |
| /ST8_1 | 0x47 | -/W | Step 8 | code |
| /ST9_1 | 0x48 | -/W | Step 9 | code |
| /ST10_1 | 0x49 | -/W | Step 10 | code |
| /ST11_1 | 0x4A | -/W | Step 11 | code |
| /ST12_1 | 0x4B | -/W | Step 12 | code |
| /ST13_1 | 0x4C | -/W | Step 13 | code |
| /ST14_1 | 0x4D | -/W | Step 14 | code |
| /ST15_1 | 0x4E | -/W | Step 15 | code |
| /ST16_1 | 0x4F | -/W | Step 16 | code |
| /TIM4_1 | 0x50 | -/W | Timer 4 | General timer parameter, unsigned value |
| /TIM3_1 | 0x51 | -/VV | Timer 3 | General timer parameter, unsigned value |
| /TIM2 1 | 0x52 | -/W | Timer 2 LSB | General timer parameter, unsigned value |
| / 1 11/12_1 | 0x53 | -/VV | Timer 2 MSB | General limer parameter, unsigned value |
| /TIM1 1 | 0x54 | -/W | Timer 1 LSB | General timer parameter, unsigned value |
| / 1 1101 1 _ 1 | 0x55 | -/W | Timer 1 MSB | General linter parameter, unsigned value |
| /THRS2_1 | 0x56 | -/W | Threshold 2 | Signed value |
| /THRS1_1 | 0x57 | -/W | Threshold 1 | Signed value |

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/SA1

The register that controls the settings of swap axis and sign masks.

| -/W | -/W | -/W | -/W | -/W | -/W | -/W | -/W |
|------|------|------|------|------|------------------|-------------------------|-------|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | BitO |
| | | | | | l l ² | ² C Address: | 0x59h |

 P_X is axis mask x+. $P_X = 0$ x+ disabled. $P_X = 1$ x+ enabled.

 N_X is axis mask x-. $N_X = 0 x$ - disabled. $N_X = 1 x$ - enabled.

 P_Y is axis mask y+. $P_Y = 0$ y+ disabled. $P_Y = 1$ y+ enabled.

 N_Y is axis mask y-. $N_Y = 0$ y- disabled. $N_Y = 1$ y- enabled.

P_Z is axis mask z+. $P_Z = 0 z$ + disabled. $P_Z = 1 z$ + enabled.

N_Z is axis mask z-. $N_Z = 0$ z- disabled. $N_Z = 1$ z- enabled.

 P_V is axis mask v+. $P_V = 0$ v+ disabled. $P_V = 1$ v+ enabled.

 N_V is axis mask v-. $N_V = 0$ v- disabled. $N_V = 1$ v- enabled.



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/MA1

The register that controls the default settings of axis and sign masks.

| -/W | -/W | -/W | -/W | -/W | -/W | -/W | -/W | |
|------|-------------------|---|--|-------------------------------------|------|------------|-------|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V | |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| | | | | | | C Address: | 0x5Ah | |
| | P_X N_X P_Y | (is axis ma P_X = P_X = (is axis ma N_X = N_X = (is axis ma P_Y = | ask x+. 0 x+ disab 1 x+ enabl ask x 0 x- disabl 1 x- enabl ask y+. 0 y+ disab | led. led. led. ed. led. | 0 | | | 5 |
| | N_Y | P_Y = is axis ma N_Y = | i y+ enabl ask y 0 y- disabl | led. | 0 | | | |

N_Y is axis mask y-. $N_Y = 0 y$ - disabled. $N_Y = 1 y$ - enabled.

P_Z is axis mask z+. Z = 0 z + disabled.Z = 1 z + enabled.

Z is axis mask z-. $N_Z = 0 z$ - disabled. $N_Z = 1 z$ - enabled.

P_V is axis mask v+. P V = 0 v + disabled. $P_V = 1 v_+ enabled.$

N_V is axis mask v-. N V = 0 v- disabled. $N_V = 1 v$ - enabled.



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/SETT1

The register that controls the State Program 1 flow.

| -/W | -/W | -/W | -/W | -/W | -/W | -/W | -/W |
|-------|---------|------|------|------|---------|-------------------------|-------|
| P_DET | THR3_SA | ABS | 0 | 0 | THR3_MA | R_TAM | SITR |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | | ² C Address: | 0x5Bh |

P_DET is the peak detection control bit. P DET = 0 peak detection disabled.

 $P_DET = 1$ peak detection enabled in State Program 1.

THR3_SA controls the reset action when Threshold 3 is exceeded and mask is /SA1. THR3_SA = 0 no action.

THR3_SA = 1 Exceeding Threshold 3 immediately triggers Reset action if mask is /SA1 (/MASA1 == 1). Every sample and every axis is tested to determine if it exceeds Threshold 3 regardless of the /TAMxA1 value. /THRS3 (register) limit is common for both State Programs.

ABS is the peak absolute threshold enable/disable control.

ABS = 0 unsigned thresholds. Thresholds are symmetric across the zero line. ABS = 1 signed thresholds in State Program 1. Thresholds are sign dependent.

THR3_MA controls the reset action when Threshold 3 is exceeded and mask is /MA1. THR3_MA = 0 no action.

THR3_MA = 1 Exceeding Threshold 3 immediately triggers Reset action if mask is /SA1 (/MASA1 == 0). Every sample and every axis is tested to determine if it exceeds Threshold 3 regardless of the /TAMxA1 value. /THRS3 (register) limit is common for both State Programs.

R_TAM is the temporary axis mask and peak state flag release.

 $R_{TAM} = 0$ no changes for /TAMxA1.

 $R_TAM \neq 1 / TAMxA^{1}$ released to default after every valid NEXT condition.

SITR is the temporary axis mask and peak state flag release.

SITR = 0 no actions.

SITR = 1 STOP and CONT commands proceeds also output as OUTC command.



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/PR1

The register contains the program pointer (PP1) address and the reset point (RP1) address. The internal addresses for program flow management are reported in an unsigned 4b+4b value. /PR1_PP1 is the LSB part of byte (/PP1) and /PR1_RP1 is the MSB part of byte (/RP1)

| R | R | R | R | R | R | R | R | |
|-------|-------|-------|-------|-------|-------|-------------------------|-------|-------------|
| RP1_3 | RP1_2 | RP1_1 | RP1_0 | PP1_3 | PP1_2 | PP1_1 | PP1_0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | ľ | ² C Address: | 0x5Ch | |

/TC1_L

Current timer counter value (unsigned) least significant byte

| R | R | R | R | R | R | R | R | |
|-------|-------|-------|-------|-------|-------|------------------------|---------|-------------|
| TC1_7 | TC1_6 | TC1_5 | TC1_4 | TC1_3 | TC1_2 | TC1_1 | TC1_0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | | ² C Address | : 0x5Dh | |

/TC1_H

Current timer counter value (unsigned) most significant byte

| R | R | R | R | R | R | R | R | |
|--------|--------|--------|--------|--------|--------------|------------|-------|-------------|
| TC1_15 | TC1_14 | TC1_13 | TC1_12 | TC1_11 | TC1_10 | TC1_9 | TC1_8 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | ² | C Address: | 0x5Eh | |

/OUTS1

The output register containing the main set flags. Reading this register affects the interrupt release function. This register is set to default after the host reads this register.

| R | R | R | R | R | R | R | R | |
|------|------|------|------|------|--------------|-------------------------|-------|-------------|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | ² | ² C Address: | 0x5Fh | |

 P_X is axis mask x+. $P_X = 0$ x+ no show. $P_X = 1$ x+ show.

 N_X is axis mask x-. $N_X = 0$ x- no show. $N_X = 1$ x- show.

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State Program 2

The following 32 registers pertain to State Program 2. They contain the program code, timers, thresholds, masks, settings, and outputs.

| Register Name | I ² C Address | Read/Write | Name | Description |
|-----------------------|--------------------------|------------|-------------|---|
| /ST1_2 | 0x60 | -/W | Step 1 | code |
| /ST2_2 | 0x61 | -/W | Step 2 | code |
| /ST3_2 | 0x62 | -/W | Step 3 | code |
| /ST4_2 | 0x63 | -/VV | Step 4 | code |
| /ST5_2 | 0x64 | -/VV | Step 5 | code |
| /ST6_2 | 0x65 | -/VV | Step 6 | code |
| /ST7_2 | 0x66 | -/VV | Step 7 | code |
| /ST8_2 | 0x67 | -/W | Step 8 | code |
| /ST9_2 | 0x68 | -/W | Step 9 | code |
| /ST10_2 | 0x69 | -/W | Step 10 | code |
| /ST11_2 | 0x6A | -/W | Step 11 | code |
| /ST12_2 | 0x6B | -/W | Step 12 | code |
| /ST13_2 | 0x6C | -/W | Step 13 | code |
| /ST14_2 | 0x6D | -/W | Step 14 | code |
| /ST15_2 | 0x6E | -/W | Step 15 | code |
| /ST16_2 | 0x6F | -/W | Step 16 | code |
| /TIM4_2 | 0x70 | -/W | Timer 4 | General timer parameter, unsigned value |
| /TIM3_2 | 0x71 | -/VV | Timer 3 | General timer parameter, unsigned value |
| | 0x72 | -/W | Timer 2 LSB | Coneral timer parameter, unsigned value |
| /111112_2 | 0x73 | -/VV | Timer 2 MSB | General limer parameter, unsigned value |
| /TIM1_2 | 0x74 | -/W | Timer 1 LSB | General timer parameter, unsigned value |
| / I IIWI I _ Z | 0x75 | -/W | Timer 1 MSB | |
| /THRS2_2 | 0x76 | -/W | Threshold 2 | Signed value |
| /THRS1_2 | 0x77 | -/W | Threshold 1 | Signed value |

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| /DES2 | 0: | x78 | -/W | Decim | ation | Initial decimation | on counter value | |
|-----------------------|------------|-----------|---------------|------------|----------|--------------------------|------------------|--|
| /SA2 The re | gister tha | at contro | ls the settir | igs of swa | p axis a | and sign mask | (S. | |
| -/W | -/W | -/W | -/W | -/W | -/W | -/W | -/W | |
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V | |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| | | | | | | I ² C Address | : 0x79h | |
| | ΡXi | s axis ma | ask x+. | | | Ó | | |

 P_X is axis mask x+. $P_X = 0$ x+ disabled. $P_X = 1$ x+ enabled.

N_X is axis mask x-. $N_X = 0 x$ - disabled. $N_X = 1 x$ - enabled.

 P_Y is axis mask y+. $P_Y = 0$ y+ disabled. $P_Y = 1$ y+ enabled.

 N_Y is axis mask y-. $N_Y = 0$ y- disabled. $N_Y = 1$ y- enabled.

 P_Z is axis mask z+. $P_Z = 0$ z+ disabled. $P_Z = 1$ z+ enabled.

N_Z is axis mask z-. $N_Z = 0$ z- disabled. $N_Z = 1$ z- enabled.

 P_V is axis mask v+. $P_V = 0$ v+ disabled. $P_V = 1$ v+ enabled.

 N_V is axis mask v-. $N_V = 0$ v- disabled. $N_V = 1$ v- enabled.



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/MA2

The register that controls the default settings of axis and sign masks.

| -/W | -/W | -/W | -/W | -/W | -/W | -/W | -/W | |
|------|-------------------|---|--|-------------------------------------|------|------------|-------|---------------|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V | |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| | | | | | | C Address: | 0x7Ah | |
| | P_X N_X P_Y | (is axis ma P_X = P_X = (is axis ma N_X = N_X = (is axis ma P_Y = P_Y = P_Y = | ask x+. 0 x+ disab 1 x+ enabl ask x 0 x- disabl 1 x- enabl ask y+. 0 y+ disab 1 y+ enabl | led. led. led. ed. led. | 0 | | | , 7 |
| | N_Y | is axis ma N_Y = | ask y 0 y- disabl | ed. | | | | |

N_Y is axis mask y-. $N_Y = 0 y$ - disabled. $N_Y = 1 y$ - enabled.

P_Z is axis mask z+. Z = 0 z + disabled.= 1 z+ enabled.

Z is axis mask z-. $N_Z = 0 z$ - disabled. $N_Z = 1 z$ - enabled.

P_V is axis mask v+. P V = 0 v + disabled. $P_V = 1 v_+ enabled.$

N_V is axis mask v-. N V = 0 v- disabled. $N_V = 1 v$ - enabled.



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/SETT2

The register that controls the State Program 2 flow.

| -/W | -/W | -/W | -/W | -/W | -/W | -/W | -/W |
|-------|---------|------|------|------|---------|-------------------------|-------|
| P_DET | THR3_SA | ABS | RADI | D_CS | THR3_MA | R_TAM | SITR |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | | | | | ² C Address: | 0x7Bh |

P_DET is the peak detection control bit. P DET = 0 peak detection disabled.

P DET = 1 peak detection enabled in State Program 2.

THR3_SA controls the reset action when Threshold 3 is exceeded and mask is /SA2. THR3_SA = 0 no action.

THR3_SA = 1 Exceeding Threshold 3 immediately triggers Reset action if mask is /SA2 (/MASA2 == 1). Every sample and every axis is tested to determine if it exceeds Threshold 3 regardless of the /TAMxA2 value. /THRS3 (register) limit is common for both State Programs.

ABS is the peak absolute threshold enable/disable control.

ABS = 0 unsigned thresholds. Thresholds are symmetric across the zero line.

ABS = 1 signed thresholds in State Program 2. Thresholds are sign dependent.

RADI controls difference data mode. Only for State Program 2.

RADI = 0 use raw data

RADI = 1 use difference data in State Program 2.

D_CS DIFF2 or constant shift mode. Only for State Program 2.

- $D_{CS} = 0 DIFF2$
- D_CS = 1 constant shift for DIFF definition

THR3_MA controls the reset action when Threshold 3 is exceeded and mask is /MA2. THR3_MA = 0 no action.

THR3_MA = 1 Exceeding Threshold 3 immediately triggers Reset action if mask is /SA2 (/MASA2 == 0). Every sample and every axis is tested to determine if it exceeds Threshold 3 regardless of the /TAMxA2 value. /THRS3 (register) limit is common for both State Programs.

R_TAM is the temporary axis mask and peak state flag release.

 $R_TAM = 0$ no changes for /TAMxA2.

 $R_TAM = 1 / TAM x A^2$ released to default after every valid NEXT condition.

SITR is the temporary axis mask and peak state flag release.

SITR = 0 no actions.

SITR = 1 STOP and CONT commands proceeds also output as OUTC command.



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/PR2

The register contains the program pointer (PP2) address and the reset point (RP2) address. The internal addresses for program flow management are reported in an unsigned 4b+4b value. /PR2_PP2 is the LSB part of byte (/PP2) and /PR2_RP2 is the MSB part of byte (/RP2)

| R | R | R | R | R | R | R | R | |
|-------|-------|-------|-------|-------|-------|-------------------------|-------|-------------|
| RP2_3 | RP2_2 | RP2_1 | RP2_0 | PP2_3 | PP2_2 | PP2_1 | PP2_0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | | ² C Address: | 0x7Ch | |

/TC2_L

Current timer counter value (unsigned) least significant byte

| R | R | R | R | R | R | R | R | |
|-------|-------|-------|-------|-------|-------|------------------------|---------|-------------|
| TC2_7 | TC2_6 | TC2_5 | TC2_4 | TC2_3 | TC2_2 | TC2_1 | TC2_0 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | | ² C Address | : 0x7Dh | |

/TC2_H

Current timer counter value (unsigned) most significant byte

| R | R | R | R | R | R | R | R | |
|--------|--------|--------|--------|--------|--------------|-----------|-------|-------------|
| TC2_15 | TC2_14 | TC2_13 | TC2_12 | TC2_11 | TC2_10 | TC2_9 | TC2_8 | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | ² | C Address | 0x7Eh | |

/OUTS2

The output register containing the main set flags. Reading this register affects the interrupt release function. This register is set to default after the host reads this register.

| R | R | R | R | R | R | R | R | |
|------|------|------|------|------|--------------|-------------------------|-------|-------------|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V | Reset Value |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 0000000 |
| | | | | | ² | ² C Address: | 0x7Fh | |

 P_X is axis mask x+. $P_X = 0$ x+ no show. $P_X = 1$ x+ show.

 N_X is axis mask x-. $N_X = 0$ x- no show. $N_X = 1$ x- show.

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State Program OP Codes

| # | Mnemonic | Explanation | Notes |
|----|----------|---|--|
| 0h | NOP | No operation | Execution moved to next or resetconditions in state |
| 1h | TI1 | Timer 1 valid | Data samples are not evaluated |
| 2h | TI2 | Timer 2 valid | Data samples are not evaluated |
| 3h | TI3 | Timer 3 valid | Data samples are not evaluated |
| 4h | TI4 | Timer 4 valid | Data samples are not evaluated |
| 5h | GNTH1 | Any/triggered axis greater than threshold 1 | First axis triggers |
| 6h | GNTH2 | Any/triggered axis greater than threshold 2 | First axis triggers |
| 7h | LNTH1 | Any/triggered axis less than or equal to threshold 1 | First axis triggers |
| 8h | LNTH2 | Any/triggered axis less than or equal to threshold 2 | First axis triggers |
| 9h | GTTH1 | Any/triggered axis greater than threshold 1 | First axis triggers |
| Ah | LLTH2 | All axis less than or equal to threshold 2 | First masked axis triggers |
| Bh | GRTH1 | Any/triggered axis greater than to reversed threshold 1 | First axis triggers |
| Ch | LRTH1 | Any/triggered axis less than or equal to reversed threshold 1 | First axis triggers |
| Dh | GRTH2 | Any/triggered axis greater than to reversed threshold 2 | First axis triggers |
| Eh | LRTH2 | Any/triggered axis less than or equal to reversed threshold 2 | First axis triggers |
| Fh | NZERO | Any axis zero crossed | Uses previous data samples sign First axis triggers |

Table 1. Conditions

| | # | Mnemonic | Explanation | Run Scope | Notes |
|---|----|----------|--|---|---|
| 0 | 0h | STOP | Stop execution, and resets reset-point to start | Immediately | Output also if enabled |
| 1 | 1h | CONT | Continues execution from reset-point | Immediately | Output also if enabled |
| 2 | 2h | JMP | Jump address for two Next conditions - 1 st parameter is conditions - 2 nd parameter are addresses for valid conditions | Immediately for command & Sample for conditions | Special (command and conditions) |
| 3 | 3h | SRP | Set reset-point to next address / state | Immediately | |
| 4 | 4h | CRP | Clear reset-point to start position (to 1 st address) | Immediately | |
| 5 | 5h | SETP | Set parameter in register memory -1 st is address of parameter - 2 nd parameter is new parameter set to address | Immediately | Address parameter is direct absolute pointer to register memory |
| 6 | 6h | SETS1 | Set new setting to Settings 1 register - 1 st is new settings byte | Immediately | |
| 7 | 7h | STHR1 | Set new value to /THRS1_y register - 1 st is new settings byte | Immediately | |
| 8 | 8h | OUTC | Set outputs to output registers | Immediately output | |



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| # | Mnemonic | Explanation | Run Scope | Notes | | |
|-------------------|----------|--|------------------------------------|-----------------------------|--|--|
| 99h | OUTW | Set outputs to output registers and wait for latch reset from host | Immediately output and Wait (host) | Host driven event | | |
| Aah | STHR2 | Set new value to /THRS2_y register - 1 st is new settings byte | Immediately | | | |
| BBh | DEC | Decrease long counter -1 and validate counter | Immediately | | | |
| CCh | SISW | Swaps sign information to opposite in mask and trigger | Immediately | | | |
| DDh | REL | Releases temporary output information | Immediately | | | |
| Eeh | STHR3 | Set new value to /THRS3 register - 1 st is new settings byte | Immediately | | | |
| FFh | SSYNC | Set synchronization point to other State program | Immediately and Wait (sync) | Affects both State Programs | | |
| Table 2. Commands | | | | | | |

Table 2. Commands

| # | Mnemonic | Explanation | Run Scope | Notes |
|-----|----------|---|-------------|---------------------------|
| 12h | SABS0 | Set /SETTy, bit ABS = 0. Select unsigned filter | Immediately | |
| 13h | SABS1 | Set /SETTy, bit ABS = 1. Select signed filter ON | Immediately | |
| 14h | SELMA | Set /MASAy pointer to May (set MASAy = 0) | Immediately | |
| 21h | SRADI0 | Set /SETT2, bit RADI = 0. Select raw data mode | Immediately | Only for State Program 2* |
| 23h | SRADI1 | Set /SETT2, bit RADI = 1. Select difference data mode | Immediately | Only for State Program 2* |
| 24h | SELSA | Set /MASAy pointer to Say (set MASAy = 1) | Immediately | |
| 31h | SCS0 | Set /SETT2, bit $D_CS = 0$. Select DIFF data mode | Immediately | Only for State Program 2* |
| 32h | SCS1 | Set /SETT2, bit D_CS = 1. Select Constant Shift data mode | Immediately | Only for State Program 2* |
| 34h | STRAMO | Set /SETTy, bit R_TAM = 0. Temporary Axis Mask /TAMxAy is kept intact | Immediately | |
| 41h | STIM3 | Set new value to /TIM3_y register - 1 st is new settings byte | Immediately | |
| 42h | STIM4 | Set new value to /TIM4_y register - 1 st is new settings byte | Immediately | |
| 43h | SRTAM1 | Set /SETTy, bit R_TAM = 1. Temporary Axis Mask /TAMxAy is released to default after every valid condition | Immediately | |

Table 3. Commands (extended set)

*Note: 21h, 23h, 31h, and 32h are forbidden with State Program 1. When a forbidden OP code exists in State Program y, it will immediately stop/halt (F_Smy_EM = 0).

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Revision History

| REVISION | DESCRIPTION | DATE |
|-----------------------|---|---|
| 1.0 | Initial Release | 21-Aug-2012 |
| 2.0 | Updated /SETT2 register to include RADI and D_CS bits | 8-Oct-2012 |
| 3.0 | Added Floor Life Specification | 19-Nov-2013 |
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