
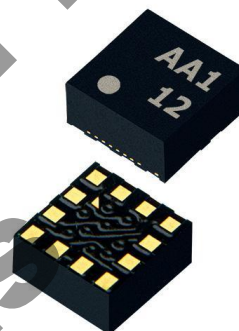


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|---|---|---|
|  | <p align="center"><b>± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications</b></p> | <p><b>PART NUMBER:</b><br/><b>KX112-1042</b><br/><b>Rev. 6.0</b><br/><b>15-Jan-2018</b></p> |
|---|---|---|


## Product Description

The KX112-1042 is a tri-axis  $\pm 2g$ ,  $\pm 4g$  or  $\pm 8g$  silicon micromachined accelerometer with integrated 2048-byte buffer, orientation, Directional-Tap™/Double-Tap™, activity detecting, and Free fall algorithms. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning, and intelligent user-programmable application algorithms. The accelerometer is delivered in a 2 x 2 x 0.6 mm LGA plastic package operating from a 1.71V – 3.6V DC supply. Voltage regulators are used to maintain constant internal operating voltages over the range of input supply voltages. This results in stable operating characteristics over the range of input supply voltages. I<sup>2</sup>C or SPI digital protocol is used to communicate with the chip to configure and check for updates to the orientation, Directional-Tap™/Double-Tap™ detection, Free fall detection, and activity monitoring algorithms.




## Features

- 2 x 2 x 0.6 mm LGA
- User-selectable g Range up to  $\pm 8g$
- User-selectable Output Data Rate up to 25600Hz
- User-selectable Low Power or High Resolution modes
- Digital High-Pass Filter Outputs
- Extra-large embedded 2048 byte FIFO/FILO buffer
- Low Power Consumption with FlexSet™ Performance Optimization
- Internal voltage regulator
- Enhanced integrated Free fall, Directional-Tap™/Double-Tap™, and Device-orientation Algorithms
- User-configurable wake-up function
- Digital I<sup>2</sup>C up to 3.4MHz and Digital SPI up to 10MHz
- Lead-free Solderability
- Excellent Temperature Performance
- High Shock Survivability
- Factory Programmed Offset and Sensitivity
- Self-test Function

|   |   |  |
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# $\pm 2g / 4g / 8g$ Tri-axis Digital Accelerometer Specifications

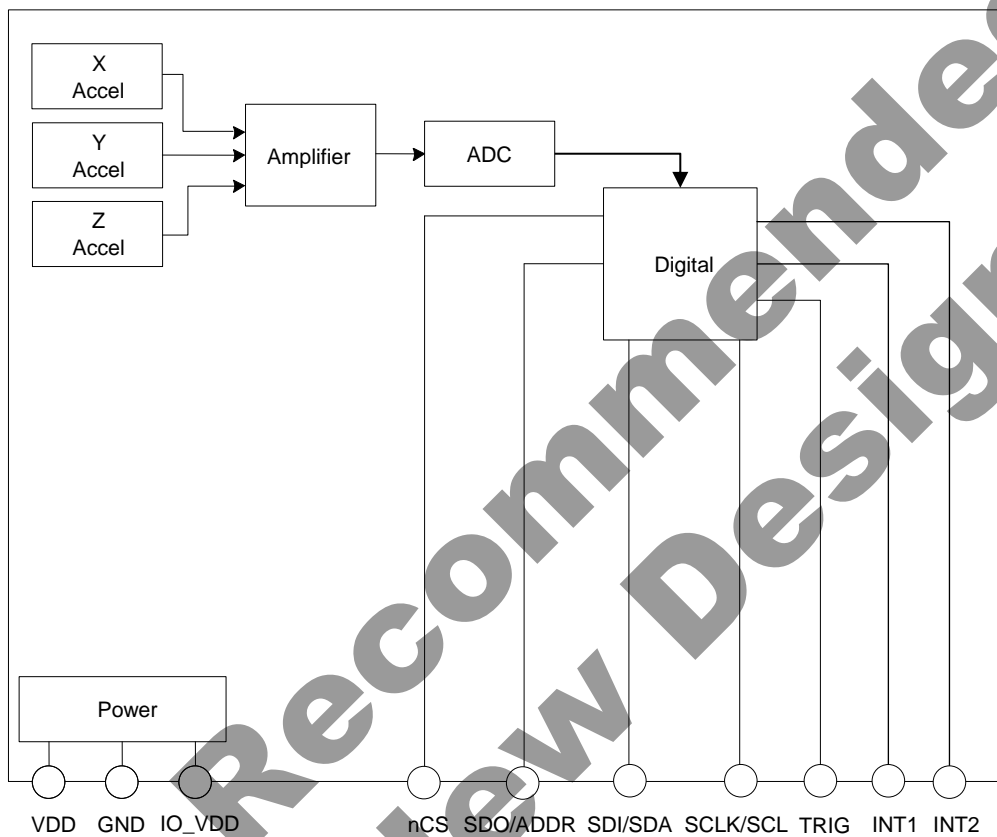
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## Functional Diagram



|   |  |   |
|---|--|---|
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|---|--|---|

## Product Specifications

### Mechanical


(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

| Parameters  |                        | Units    | Min                  | Typical               | Max   |
|---|------------------------|----------|----------------------|-----------------------|-------|
| Operating Temperature Range                                 |                        | °C       | -40                  | -                     | +85   |
| Zero-g Offset   |                        | mg       |                      | ±25                   | ±90   |
| Zero-g Offset Variation from RT over Temp.                  |                        | mg/°C    |                      | 0.2                   |       |
| Sensitivity <sup>1</sup>                                    | GSEL1=0, GSEL0=0 (±2g) | counts/g | 15401                | 16384                 | 17367 |
|   | GSEL1=0, GSEL0=1 (±4g) |          | 7700                 | 8192                  | 8684  |
|   | GSEL1=1, GSEL0=0 (±8g) |          | 3850                 | 4096                  | 4342  |
| Sensitivity (Buffer 8-bit mode) <sup>1,2</sup>              | GSEL1=0, GSEL0=0 (±2g) | counts/g | 60                   | 64                    | 68    |
|   | GSEL1=0, GSEL0=1 (±4g) |          | 30                   | 32                    | 34    |
|   | GSEL1=1, GSEL0=0 (±8g) |          | 15                   | 16                    | 17    |
| Sensitivity Variation from RT over Temp.                    |                        | %/°C     |                      | 0.01                  |       |
| Positive Self Test Output change on Activation <sup>4</sup> |                        | g        | 0.25 (xy)<br>0.2 (z) | 0.5                   | 0.75  |
| Signal Bandwidth (-3dB)                                     |                        | Hz       |                      | 3500 (xy)<br>1800 (z) |       |
| Non-Linearity   |                        | % of FS  |                      | 0.6                   |       |
| Cross Axis Sensitivity                                      |                        | %        |                      | 2                     |       |
| Noise <sup>3,5</sup>  | RMS                    | mg       |                      | 0.7                   |       |
|   | Density                | µg/√Hz   |                      | 130                   |       |

**Table 1: Mechanical Specifications**

#### Notes:

1. Resolution and acceleration ranges are user selectable via I<sup>2</sup>C or SPI
2. Sensitivity is proportional to BRES in BUF\_CNTL2
3. Noise varies with Output Data Rate (ODR), and the Average Filter Control settings and can be tested using Kionix FlexSet™ Performance Optimization Tool found at <http://www.kionix.com/flexset>
4. Requires changing of STPOL bit in INC1 register to 1 prior to performing self-test
5. Measured with ODR=50Hz, IIR\_BYPASS=0, LPRO=1 (filter corner frequency set to ODR/2)

|   |   |   |
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|---|---|---|

## Electrical

(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

| Parameters                                    |                                       | Units | Min          | Typical        | Max          |
|---|---------------------------------------|-------|--------------|----------------|--------------|
| Supply Voltage (VDD)                          | Operating                             | V     | 1.71         | 2.5            | 3.6          |
| I/O Pads Supply Voltage (IO_VDD)              |                                       | V     | 1.7          |                | 3.6          |
| Current Consumption                           | High Resolution Mode (RES = 1)        | μA    |              | 145            |              |
|   | Low Power Mode <sup>1</sup> (RES = 0) |       |              | 10             |              |
|   | Standby                               |       |              | 0.9            |              |
| Output Low Voltage (IO_VDD < 2V) <sup>2</sup> |                                       | V     | -            | -              | 0.2 * IO_VDD |
| Output Low Voltage (IO_VDD ≥ 2V) <sup>2</sup> |                                       | V     | -            | -              | 0.4          |
| Output High Voltage                           |                                       | V     | 0.8 * IO_VDD | -              | -            |
| Input Low Voltage                             |                                       | V     | -            | -              | 0.2 * IO_VDD |
| Input High Voltage                            |                                       | V     | 0.8 * IO_VDD | -              | -            |
| Start Up Time <sup>3</sup>                    |                                       | ms    | 2            |                | 1300         |
| Power Up Time <sup>4</sup>                    |                                       | ms    |              | 20             | 50           |
| I <sup>2</sup> C Communication Rate           |                                       | MHz   |              |                | 3.4          |
| I <sup>2</sup> C Slave Address (7-bit)        |                                       |       |              | 0x1E / 0x1F    |              |
| SPI Communication Rate                        |                                       | MHz   |              |                | 10           |
| Output Data Rate (ODR) <sup>5</sup>           |                                       | Hz    | 0.781        | 50             | 25600        |
| Bandwidth (-3dB) <sup>6</sup>                 |                                       | Hz    |              | ODR/9 or ODR/2 |              |

**Table 2:** Electrical Specifications

### Notes:

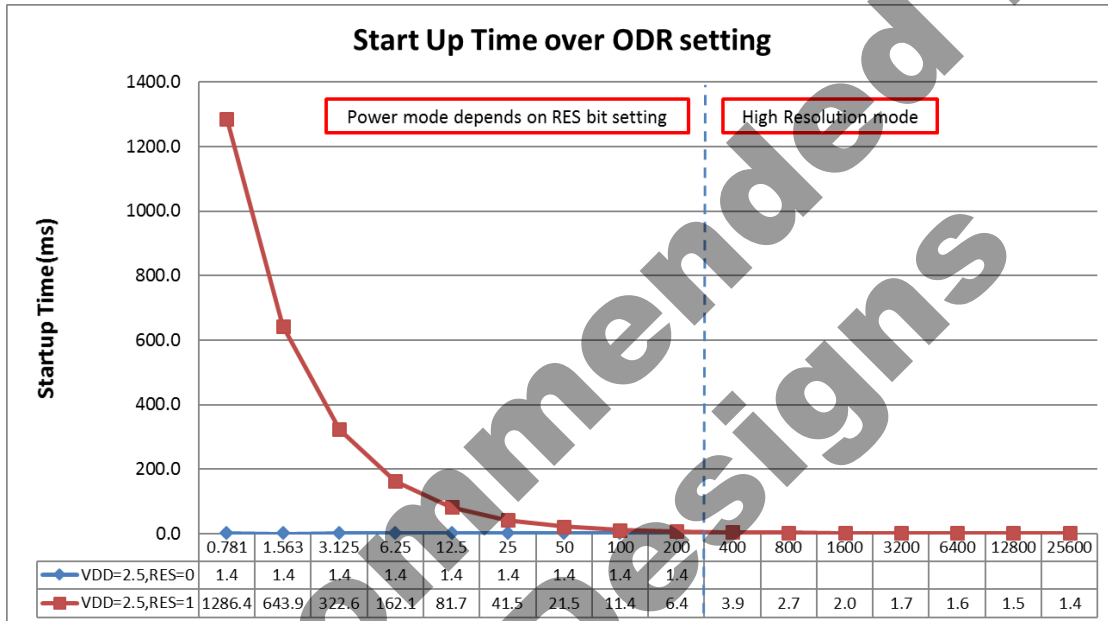
1. Current varies with Output Data Rate (ODR) as shown in Figure 2, types and number of enabled digital engines, and the Average Filter Control settings that can be tested using Kionix FlexSet™ Performance Optimization Tool found at <http://www.kionix.com/flexset>.
2. For I<sup>2</sup>C communication, this assumes a minimum 1.5kΩ pull-up resistor on SCL and SDA pins.
3. Start up time is from PC1 set to valid outputs. Time varies with Output Data Rate (ODR) and power mode setting. See Figure 1 for details.
4. Power up time is from VDD valid to device boot completion.
5. User selectable through I<sup>2</sup>C or SPI.
6. User selectable and dependent on ODR. See ODCNTL register description for details.



# ± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications

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**15-Jan-2018**

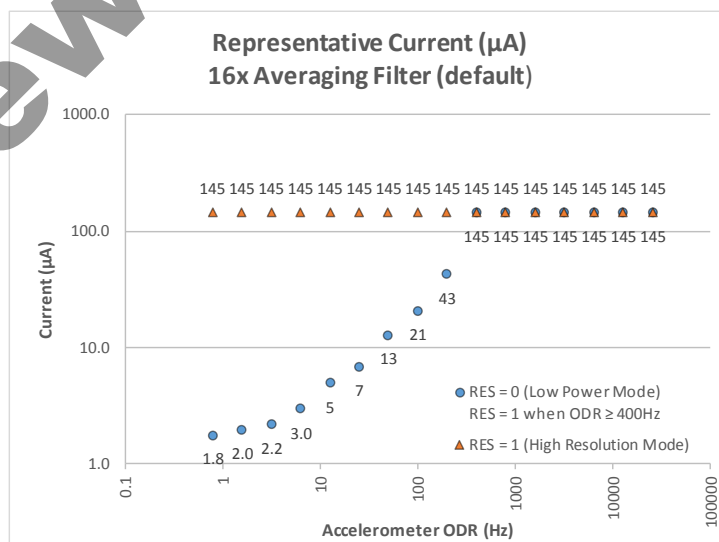
## Start Up Time Profile



**Figure 1:** Start up Time as a function of the Output Data Rate (ODR) and Power Mode Settings


## Current Profile

| Representative Current Profile (µA) |          |           |
|-------------------------------------|----------|-----------|
| ODR (Hz)                            | High Res | Low Power |
| Standby                             | 0.9      | 0.9       |
| 0.781                               | 145      | 1.8       |
| 1.563                               | 145      | 2.0       |
| 3.125                               | 145      | 2.2       |
| 6.25                                | 145      | 3.0       |
| 12.5                                | 145      | 5         |
| 25                                  | 145      | 7         |
| 50                                  | 145      | 13        |
| 100                                 | 145      | 21        |
| 200                                 | 145      | 43        |
| 400                                 | 145      | 145       |
| 800                                 | 145      | 145       |
| 1600                                | 145      | 145       |
| 3200                                | 145      | 145       |
| 6400                                | 145      | 145       |
| 12800                               | 145      | 145       |
| 25600                               | 145      | 145       |



**Figure 2:** Current as a function of the Output Data Rate (ODR) and Power Mode Settings




|   |   |  |
|---|---|--|
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### Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD**, **VDD<sub>LOW</sub>**, **T<sub>VDD</sub>** (rise time), and **T<sub>VDD\_OFF</sub>** profile of individual applications. It is recommended to minimize **VDD<sub>LOW</sub>**, and **T<sub>VDD</sub>**, and maximize **T<sub>VDD\_OFF</sub>**. It is also advised that the **VDD** ramp up time **T<sub>VDD</sub>** be monotonic. Note that the outputs will not be stable until **VDD** has reached its final value.

- ! *To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD<sub>LOW</sub>, T<sub>VDD</sub>, T<sub>VDD\_OFF</sub> and temperature as POR performance can vary depending on these parameters.*

Please refer to Technical Note [TN004 Power-On Procedure](#) for more information.

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|---|---|---|

## Environmental

| Parameters                          |                 | Units | Min  | Typical | Max                               |
|-------------------------------------|-----------------|-------|------|---------|-----------------------------------|
| Supply Voltage (VDD)                | Absolute Limits | V     | -0.5 | -       | 3.60                              |
| Operating Temperature Range         |                 | °C    | -40  | -       | 85                                |
| Storage Temperature Range           |                 | °C    | -55  | -       | 150                               |
| Mech. Shock (powered and unpowered) |                 | g     | -    | -       | 5000 for 0.5ms<br>10000 for 0.2ms |
| ESD                                 | HBM             | V     | -    | -       | 2000                              |

**Table 3:** Environmental Specifications



Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.



These products conform to RoHS Directive 2011/65/EU of the European Parliament and of the Council of the European Union that was issued June 8, 2011. Specifically, these products do not contain any non-exempted amounts of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials.

Homogenous materials are “of uniform composition throughout”. The MCV for lead, mercury, hexavalent chromium, PBB, and PBDE is 0.10%. The MCV for cadmium is 0.010%.

Applicable Exemption: 7C-I - *Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors (piezoelectronic devices) or in a glass or ceramic matrix compound.*




These products are also in conformance with REACH Regulation No 1907/2006 of the European Parliament and of the Council that was issued Dec. 30, 2011. They do not contain any Substances of Very High Concern (SVHC-174) as identified by the European Chemicals Agency as of 12 July 2017.



This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

## Soldering

Soldering recommendations are available upon request or from [www.kionix.com](http://www.kionix.com).

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## Terminology

### g

A unit of acceleration equal to the acceleration of gravity at the earth's surface. One thousandth of a g (0.0098 m/s<sup>2</sup>) is referred to as 1 milli-g (1 mg).

$$1g = 9.8 \frac{m}{s^2}$$

### Sensitivity

The sensitivity of an accelerometer is the change in output per unit of input acceleration at nominal VDD and temperature. The term is essentially the gain of the sensor expressed in counts per g (counts/g) or LSB's per g (LSB/g). Occasionally, sensitivity is expressed as a resolution, i.e. milli-g per LSB (mg/LSB) or milli-g per count (mg/count). Sensitivity for a given axis is determined by measurements of the formula:

$$Sensitivity = \frac{(Output @ +1g - Output @ -1g)}{2g}$$


The sensitivity tolerance describes the range of sensitivities that can be expected from a large population of sensors at room temperature and over life. When the temperature deviates from room temperature (25°C), the sensitivity will vary by the amount shown in Table 1.

### Zero-g offset

Zero-g offset or 0-g offset describes the actual output of the accelerometer when no acceleration is applied. Ideally, the output would always be in the middle of the dynamic range of the sensor (content of the XOUT, YOUT, ZOUT registers = 0x00, expressed as a 2's complement number). However, because of mismatches in the sensor, calibration errors, and mechanical stress, the output can deviate from 0x00. This deviation from the ideal value is called 0-g offset. The zero-g offset tolerance describes the range of 0-g offsets of a population of sensors over the operating temperature range.

### Self-test

Self-test allows a functional test of the sensor without applying a physical acceleration to it. When activated, an electrostatic force is applied to the sensor, simulating an input acceleration. The sensor outputs respond accordingly. If the output signals change within the amplitude specified in Table 1 then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

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|---|---|--|

## Functionality

### Sense element

The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. This process technology allows Kionix to create mechanical silicon structures which are essentially mass-spring systems that move in the direction of the applied acceleration. Acceleration sensing is based on the principle of a differential capacitance arising from the acceleration-induced motion. Capacitive plates on the moving mass move relative to fixed capacitive plates anchored to the substrate. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit.

### ASIC interface

A separate ASIC device packaged with the sense element provides all the signal conditioning and communication with the sensor. The complete measurement chain is composed by a low-noise capacitance to voltage amplifier which converts the differential capacitance of the MEMS sensor into an analog voltage that is sent through an analog-to-digital converter. The acceleration data may be accessed through the I<sup>2</sup>C digital communications provided by the ASIC. In addition, the ASIC contains all the logic to allow the user to choose data rates, g-ranges, filter settings, and interrupt logic. Plus, there are two programmable state machines which allow the user to create unique embedded functions based on changes in acceleration.

### Factory calibration

Kionix trims the offset and sensitivity of each accelerometer by adjusting gain (sensitivity) and 0-g offset trim codes stored in non-volatile memory (OTP). Additionally, all functional register default values are also programmed into the nonvolatile memory. Every time the device is turned on or a software reset command is issued, the trimming parameters and default register values are downloaded into the volatile registers to be used during active operation. This allows the device to function without further calibration.

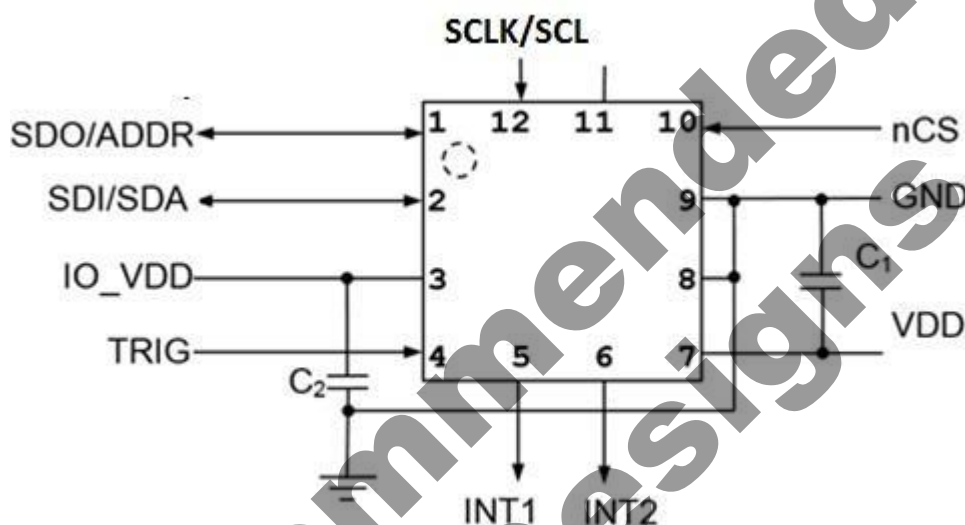


# **± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications**

**PART NUMBER:**  
**KX112-1042**  
**Rev. 6.0**  
**15-Jan-2018**

## **Application Schematic and Pin Description**

### **Application Schematic**



### **Pin Description**

| Pin | Name     | Description  |
|-----|----------|--|
| 1   | SDO/ADDR | Serial Data Out pin during 4-wire SPI communication and part of the device address during I2C communication. Do not leave floating.  |
| 2   | SDI/SDA  | SPI Data input / I2C Serial Data   |
| 3   | IO_VDD   | The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.     |
| 4   | TRIG     | Trigger pin for FIFO buffer control - Connect to GND when not using external trigger option.   |
| 5   | INT1     | Physical Interrupt 1 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used. |
| 6   | INT2     | Physical Interrupt 2 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used. |
| 7   | VDD      | The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.  |
| 8   | GND      | Ground   |
| 9   | GND      | Ground   |
| 10  | nCS      | Chip Select (active LOW) for SPI communication. Connect to IO_VDD for I2C communication. Do not leave floating.                      |
| 11  | NC       | Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating.   |
| 12  | SCLK/SCL | SPI and I2C Serial Clock   |

**Table 4: Pin Description**



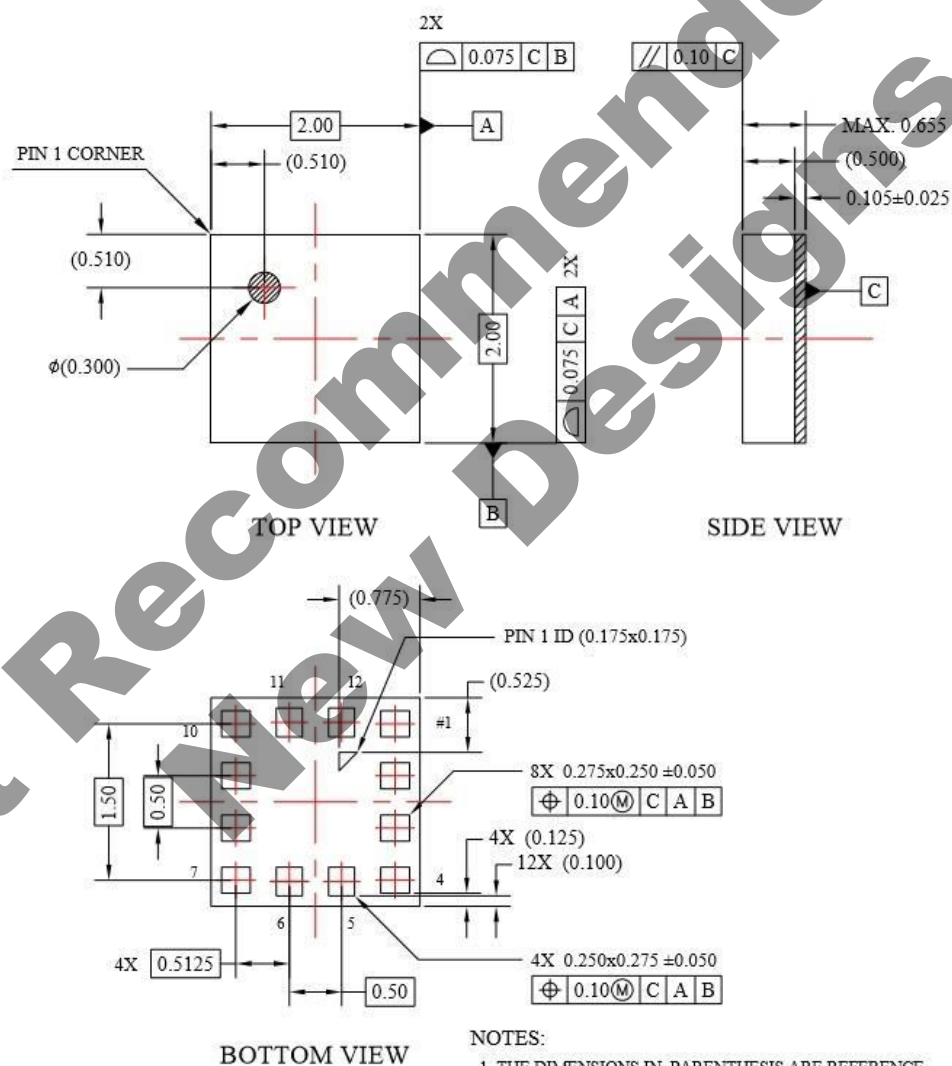
# ± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications

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## Package Dimensions and Orientation

### Dimensions

2 x 2 x 0.6 mm LGA



All dimensions and tolerances conform to ASME Y14.5M-1994



# ± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications

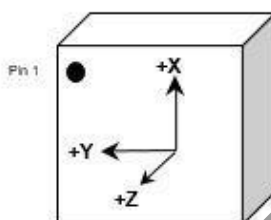
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## Orientation



When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

### **Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):**

GSEL1=0, GSEL0=0 (±2g)

| Position          | 1      |     | 2      |     | 3      |     | 4      |     | 5      |     | 6      |     |
|-------------------|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|
| Diagram           |        |     |        |     |        |     |        |     |        |     |        |     |
| Resolution (bits) | 16     | 8   | 16     | 8   | 16     | 8   | 16     | 8   | 16     | 8   | 16     | 8   |
| X (counts)        | +16384 | +64 | 0      | 0   | -16384 | -64 | 0      | 0   | 0      | 0   | 0      | 0   |
| Y (counts)        | 0      | 0   | -16384 | -64 | 0      | 0   | +16384 | +64 | 0      | 0   | 0      | 0   |
| Z (counts)        | 0      | 0   | 0      | 0   | 0      | 0   | 0      | 0   | +16384 | +64 | -16384 | -64 |
| X-Polarity        | +      |     | 0      |     | -      |     | 0      |     | 0      |     | 0      |     |
| Y-Polarity        | 0      |     | -      |     | 0      |     | +      |     | 0      |     | 0      |     |
| Z-Polarity        | 0      |     | 0      |     | 0      |     | 0      |     | +      |     | -      |     |



Earth's Surface



# **± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications**

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## **Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):**

GSEL1=0, GSEL0=1 (±4g)

| Position          | 1     |     | 2     |     | 3     |     | 4     |     | 5     |     | 6     |     |
|-------------------|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|
| Diagram           |       |     |       |     |       |     |       |     |       |     |       |     |
| Resolution (bits) | 16    | 8   | 16    | 8   | 16    | 8   | 16    | 8   | 16    | 8   | 16    | 8   |
| X (counts)        | +8192 | +32 | 0     | 0   | -8192 | -32 | 0     | 0   | 0     | 0   | 0     | 0   |
| Y (counts)        | 0     | 0   | -8192 | -32 | 0     | 0   | +8192 | +32 | 0     | 0   | 0     | 0   |
| Z (counts)        | 0     | 0   | 0     | 0   | 0     | 0   | 0     | 0   | +8192 | +32 | -8192 | -32 |
| X-Polarity        | +     |     | 0     |     | -     |     | 0     |     | 0     |     | 0     |     |
| Y-Polarity        | 0     |     | -     |     | 0     |     | +     |     | 0     |     | 0     |     |
| Z-Polarity        | 0     |     | 0     |     | 0     |     | 0     |     | +     |     | -     |     |

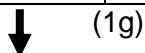


Earth's Surface

## **Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):**


GSEL1=1, GSEL0=0 (±8g)

| Position          | 1     |     | 2     |     | 3     |     | 4     |     | 5     |     | 6     |     |
|-------------------|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|
| Diagram           |       |     |       |     |       |     |       |     |       |     |       |     |
| Resolution (bits) | 16    | 8   | 16    | 8   | 16    | 8   | 16    | 8   | 16    | 8   | 16    | 8   |
| X (counts)        | +4096 | +16 | 0     | 0   | -4096 | -16 | 0     | 0   | 0     | 0   | 0     | 0   |
| Y (counts)        | 0     | 0   | -4096 | -16 | 0     | 0   | +4096 | +16 | 0     | 0   | 0     | 0   |
| Z (counts)        | 0     | 0   | 0     | 0   | 0     | 0   | 0     | 0   | +4096 | +16 | -4096 | -16 |
| X-Polarity        | +     |     | 0     |     | -     |     | 0     |     | 0     |     | 0     |     |
| Y-Polarity        | 0     |     | -     |     | 0     |     | +     |     | 0     |     | 0     |     |
| Z-Polarity        | 0     |     | 0     |     | 0     |     | 0     |     | +     |     | -     |     |



Earth's Surface



|   |   |  |
|---|---|--|
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## Digital Interface

The Kionix KX112 digital accelerometer can communicate via the I<sup>2</sup>C and SPI digital serial interface protocols. This allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 5 below will be observed throughout this document.

| Term        | Description   |
|-------------|---|
| Transmitter | The device that transmits data to the bus.  |
| Receiver    | The device that receives data from the bus.   |
| Master      | The device that initiates a transfer, generates clock signals, and terminates a transfer. |
| Slave       | The device addressed by the Master.   |

**Table 5:** Serial Interface Terminologies

## I<sup>2</sup>C Serial Interface

As previously mentioned, the KX112 accelerometer can communicate on an I<sup>2</sup>C bus. I<sup>2</sup>C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KX112 always operates as a Slave device during standard Master-Slave I<sup>2</sup>C operation.

I<sup>2</sup>C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held LOW by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I<sup>2</sup>C bus is considered free when both lines are HIGH.

The I<sup>2</sup>C interface is compliant with high-speed mode, fast mode, and standard mode I<sup>2</sup>C protocols.



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### I<sup>2</sup>C Operation

Transactions on the I<sup>2</sup>C bus begin after the Master transmits a start condition (S), which is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The KX112 Slave Address is comprised of a user programmable part, a factory programmable part, and a fixed part, which allows for connection of multiple accelerometers to the same I<sup>2</sup>C bus. The Slave Address associated with the KX112 is 00111YX, where the user programmable bit X, is determined by the assignment of ADDR pin to GND or IO\_VDD. Also, the factory programmable bit Y is set at the factory. **For KX112-1042, the factory programmable bit Y is fixed to 1** (contact your Kionix sales representative for list of available devices). Table 6 lists possible I<sup>2</sup>C addresses for KX112-1042. It is possible to have up to four accelerometers on a shared I<sup>2</sup>C bus as shown in Figure 3 (i.e. two KX112-1042 accelerometers and two additional accelerometers with the factory programmable bit Y set to 0).

| Description | Address Pad | 7-bit Address | Address | <7> | <6> | <5> | <4> | <3> | Y   | X   | <0> |
|-------------|-------------|---------------|---------|-----|-----|-----|-----|-----|-----|-----|-----|
|             |             |               |         |     |     |     |     |     | <2> | <1> |     |
| I2C Wr      | GND         | 0x1E          | 0x3C    | 0   | 0   | 1   | 1   | 1   | 1   | 0   | 0   |
| I2C Rd      | GND         | 0x1E          | 0x3D    | 0   | 0   | 1   | 1   | 1   | 1   | 0   | 1   |
| I2C Wr      | IO_VDD      | 0x1F          | 0x3E    | 0   | 0   | 1   | 1   | 1   | 1   | 1   | 0   |
| I2C Rd      | IO_VDD      | 0x1F          | 0x3F    | 0   | 0   | 1   | 1   | 1   | 1   | 1   | 1   |

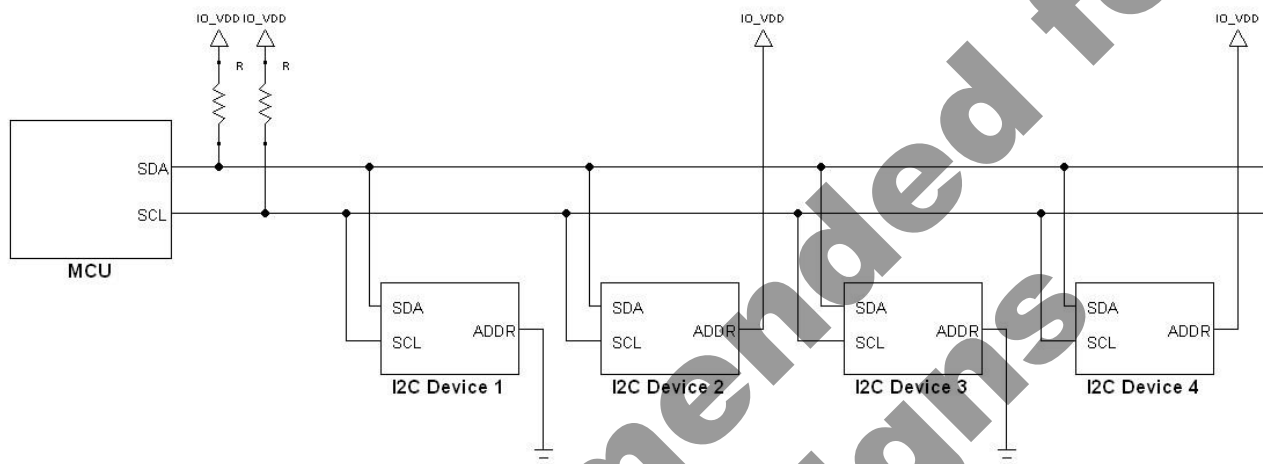
Table 6: I<sup>2</sup>C Slave Addresses for KX112-1042

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line LOW so that it remains stable LOW during the HIGH period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C bus is now free. Note that if the accelerometer is accessed through I<sup>2</sup>C protocol before the startup is finished a NACK signal is sent.



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| I <sup>2</sup> C Device | Part Number | ADDR Pin | Slave Address | Bit Y (Bit 1 in 7-bit address) |
|-------------------------|-------------|----------|---------------|--------------------------------|
| 1                       | KX112-1042  | GND      | 0x1E          | Factory Set to 1               |
| 2                       | KX112-1042  | IO_VDD   | 0x1F          | Factory Set to 1               |
| 3                       | *KXMMM      | GND      | 0x1C          | Factory Set to 0               |
| 4                       | *KXMMM      | IO_VDD   | 0x1D          | Factory Set to 0               |


\* KXMMM – contact Kionix sales representative for list of compatible devices

**Figure 3: Multiple KX112 Accelerometers on a Shared I<sup>2</sup>C Bus**

## Writing to an 8-bit Register

Upon power up, the Master must write to the KX112's control registers to set its operational mode. Therefore, when writing to a control register on the I<sup>2</sup>C bus, as shown Sequence 1, the following protocol must be observed: After a start condition, SAD+W transmission, and the KX112 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KX112 to which 8-bit register the Master will be writing the data. Since this is I<sup>2</sup>C mode, the MSB of the RA command should always be zero (0). The KX112 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KX112 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KX112 is now stored in the appropriate register. The KX112 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2.

**\*\*Note\*\*** If a STOP condition is sent on the least significant bit of write data or the following master acknowledge cycle, the last write operation is not guaranteed and it may alter the content of the affected registers.

|   |   |   |
|---|---|---|
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### Reading from an 8-bit Register

When reading data from a KX112 8-bit register on the I<sup>2</sup>C bus, as shown in Sequence 3, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KX112 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KX112 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KX112 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KX112 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4. Reading data from a buffer read register is a special case because if register address (RA) is set to buffer read register (BUF\_READ) in Sequence 4, the register auto-increment feature is automatically disabled. Instead, the Read Pointer will increment to the next data in the buffer, thus allowing reading multiple bytes of data from the buffer using a single SAD+R command.

**\*\*Note\*\*** Accelerometer's output data should be read in a single transaction using the auto-increment feature to prevent output data from being updated prior to intended completion of the read transaction.



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## Data Transfer Sequences

The following information illustrates the variety of data transfers that can occur on the I<sup>2</sup>C bus and how the Master and Slave interact during these transfers. Table 7 defines the I<sup>2</sup>C terms used during the data transfers.

| Term | Definition                |
|------|---------------------------|
| S    | Start Condition           |
| Sr   | Repeated Start Condition  |
| SAD  | Slave Address             |
| W    | Write Bit                 |
| R    | Read Bit                  |
| ACK  | Acknowledge               |
| NACK | Not Acknowledge           |
| RA   | Register Address          |
| Data | Transmitted/Received Data |
| P    | Stop Condition            |

Table 7: I<sup>2</sup>C Terms

**Sequence 1:** The Master is writing one byte to the Slave

|        |   |         |     |    |     |      |     |   |
|--------|---|---------|-----|----|-----|------|-----|---|
| Master | S | SAD + W |     | RA |     | DATA |     | P |
| Slave  |   |         | ACK |    | ACK |      | ACK |   |

**Sequence 2:** The Master is writing multiple bytes to the Slave


|        |   |         |     |    |     |      |     |      |     |   |
|--------|---|---------|-----|----|-----|------|-----|------|-----|---|
| Master | S | SAD + W |     | RA |     | DATA |     | DATA |     | P |
| Slave  |   |         | ACK |    | ACK |      | ACK |      | ACK |   |

**Sequence 3:** The Master is receiving one byte of data from the Slave

|        |   |         |     |    |     |    |         |     |      |      |   |
|--------|---|---------|-----|----|-----|----|---------|-----|------|------|---|
| Master | S | SAD + W |     | RA |     | Sr | SAD + R |     |      | NACK | P |
| Slave  |   |         | ACK |    | ACK |    |         | ACK | DATA |      |   |

**Sequence 4:** The Master is receiving multiple bytes of data from the Slave

|        |   |         |     |    |     |    |         |     |      |     |      |      |   |
|--------|---|---------|-----|----|-----|----|---------|-----|------|-----|------|------|---|
| Master | S | SAD + W |     | RA |     | Sr | SAD + R |     |      | ACK |      | NACK | P |
| Slave  |   |         | ACK |    | ACK |    |         | ACK | DATA |     | DATA |      |   |

|   |   |  |
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## HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

### Sequence 5: HS-mode data transfer of the Master writing multiple bytes to the Slave

| Speed  | FS-mode |        |      | HS-mode |         |     |    |     |      |     |   | FS-mode |
|--------|---------|--------|------|---------|---------|-----|----|-----|------|-----|---|---------|
| Master | S       | M-code | NACK | Sr      | SAD + W |     | RA |     | DATA |     | P |         |
| Slave  |         |        |      |         |         | ACK |    | ACK |      | ACK |   |         |

n bytes + ack.

### Sequence 6: HS-mode data transfer of the Master receiving multiple bytes of data from the Slave

| Speed  | FS-mode |        |      | HS-mode |         |     |    |     |
|--------|---------|--------|------|---------|---------|-----|----|-----|
| Master | S       | M-code | NACK | Sr      | SAD + W |     | RA |     |
| Slave  |         |        |      |         |         | ACK |    | ACK |

| Speed  | HS-mode |         |     |      |     |      |      |   | FS-mode |
|--------|---------|---------|-----|------|-----|------|------|---|---------|
| Master | Sr      | SAD + R |     |      |     |      | NACK | P |         |
| Slave  |         |         | ACK | DATA | ACK | DATA |      |   |         |

(n-1) bytes + ack.



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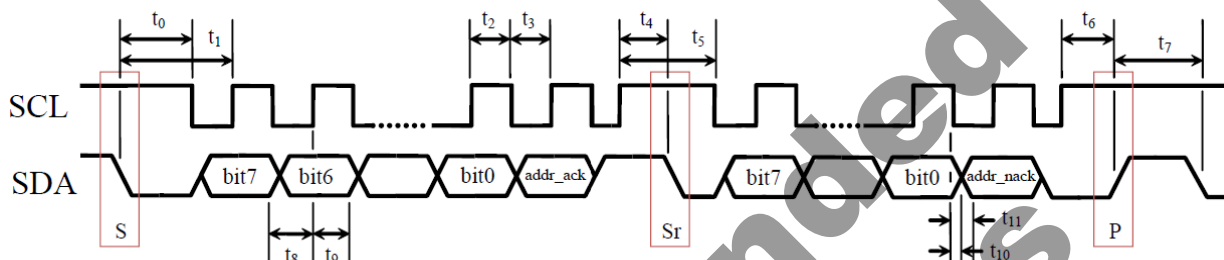
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## **I<sup>2</sup>C Timing Diagram**



| Number          | Description  | MIN | MAX | Units |
|-----------------|--|-----|-----|-------|
| t <sub>0</sub>  | SDA LOW to SCL LOW transition (Start event)                  | 50  | -   | ns    |
| t <sub>1</sub>  | SDA LOW to first SCL rising edge                             | 100 | -   | ns    |
| t <sub>2</sub>  | SCL pulse width: HIGH  | 100 | -   | ns    |
| t <sub>3</sub>  | SCL pulse width: LOW   | 100 | -   | ns    |
| t <sub>4</sub>  | SCL HIGH before SDA falling edge (Start Repeated)            | 50  | -   | ns    |
| t <sub>5</sub>  | SCL pulse width: HIGH during a S/Sr/P event                  | 100 | -   | ns    |
| t <sub>6</sub>  | SCL HIGH before SDA rising edge (Stop)                       | 50  | -   | ns    |
| t <sub>7</sub>  | SDA pulse width: HIGH  | 25  | -   | ns    |
| t <sub>8</sub>  | SDA valid to SCL rising edge                                 | 50  | -   | ns    |
| t <sub>9</sub>  | SCL rising edge to SDA invalid                               | 50  | -   | ns    |
| t <sub>10</sub> | SCL falling edge to SDA valid (when slave is transmitting)   | -   | 100 | ns    |
| t <sub>11</sub> | SCL falling edge to SDA invalid (when slave is transmitting) | 0   | -   | ns    |
| Note            | Recommended I <sup>2</sup> C CLK                             | 2.5 | -   | μs    |

**Table 8: I<sup>2</sup>C Timing (Fast Mode)**

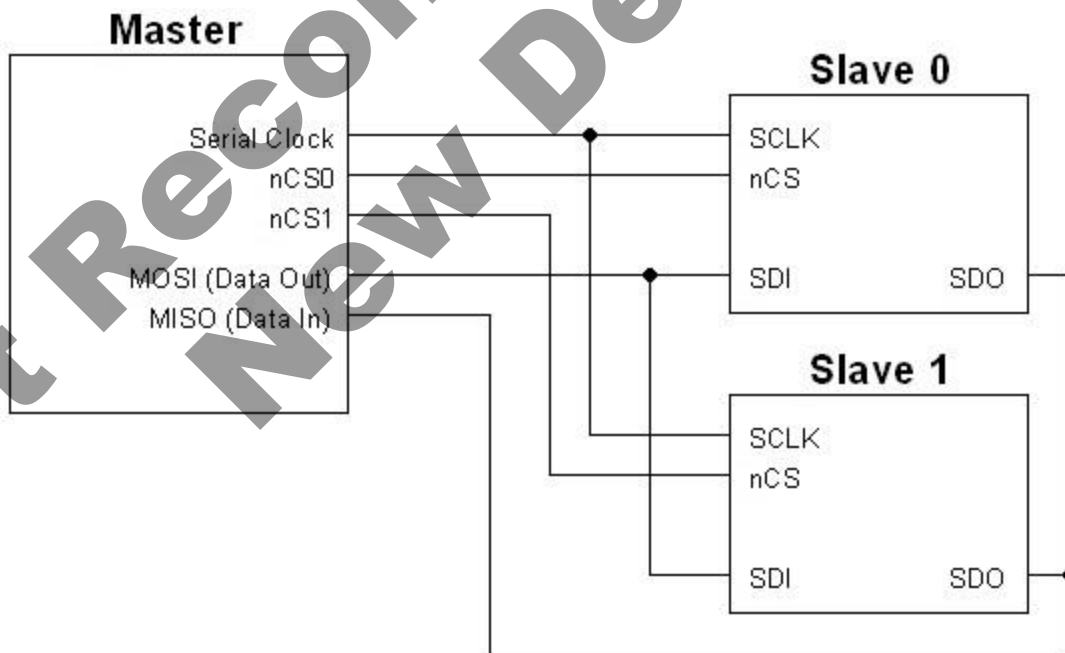
|   |   |  |
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## SPI Communications

### 4-Wire SPI Interface

The KX112 also utilizes an integrated 4-Wire Serial Peripheral Interface (SPI) for digital communication. The SPI interface is primarily used for synchronous serial communication between one Master device and one or more Slave devices. The Master, typically a micro controller, provides the SPI clock signal (SCLK) and determines the state of Chip Select (nCS). The KX112 always operates as a Slave device during standard Master-Slave SPI operation.

4-wire SPI is a synchronous serial interface that uses two control and two data lines. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDI or MOSI) and the Data Input (SDO or MISO) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes LOW at the start of transmission and goes back HIGH at the end. The Slave Data Output (SDO) line, remains in a high-impedance (hi-z) state when the device is not selected, so it does not interfere with any active devices. This allows multiple Slave devices to share a master SPI port as shown in Figure 4 below.



**Figure 4: 4-wire SPI Connections**





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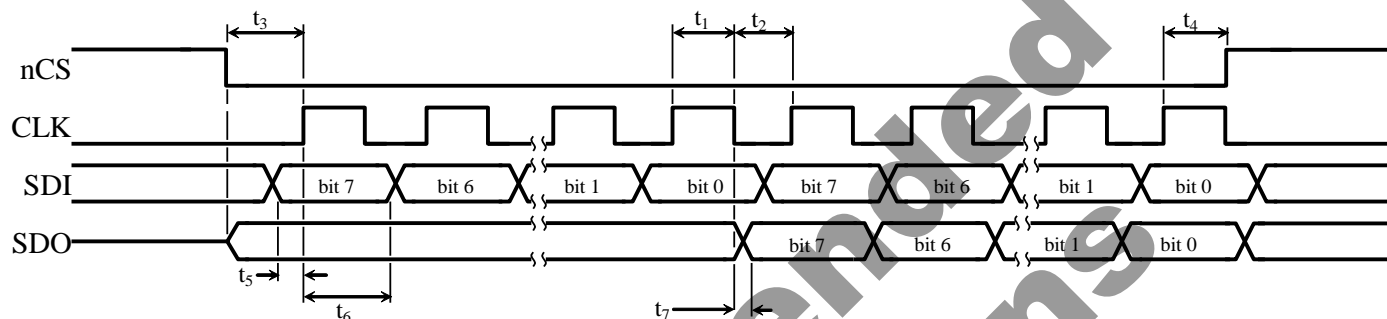
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## **4-Wire SPI Timing Diagram**



| Number         | Description                             | MIN | MAX | Units |
|----------------|---|-----|-----|-------|
| t <sub>1</sub> | CLK pulse width: HIGH                   | 40  |     | ns    |
| t <sub>2</sub> | CLK pulse width: LOW                    | 40  |     | ns    |
| t <sub>3</sub> | nCS LOW to first CLK rising edge        | 20  |     | ns    |
| t <sub>4</sub> | nCS LOW after the final CLK rising edge | 30  |     | ns    |
| t <sub>5</sub> | SDI valid to CLK rising edge            | 10  |     | ns    |
| t <sub>6</sub> | CLK rising edge to SDI invalid          | 10  |     | ns    |
| t <sub>7</sub> | CLK falling edge to SDO valid           |     | 35  | ns    |

**Table 9: 4-Wire SPI Timing**

## **Notes**

1. t<sub>7</sub> is only present during reads.
2. Timings are for VDD of 1.8V to 3.6V with 1kΩ pull-up resistor and maximum 20pF load capacitor on SDO.



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### 4-Wire Read and Write Registers

The registers embedded in the KX112 accelerometer have 8-bit addresses. Upon power up, the Master must write to the accelerometer's control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate "0" when writing to the register and "1" when reading from the register. This operation occurs over 16 clock cycles. All commands are sent MSB first. The host must return nCS HIGH for at least one clock cycle before the next data request. However, when data is being read from a buffer read register (BUF\_READ), the nCS signal can remain LOW until the buffer is read. Figure 5 below shows the timing diagram for carrying out an 8-bit register write operation.

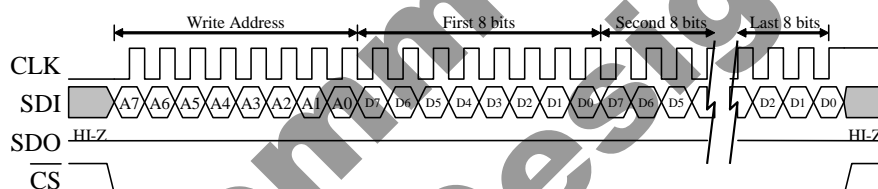


Figure 5: Timing Diagram for 8-Bit Register Write Operation

In order to read an 8-bit register, an 8-bit register address must be written to the accelerometer to initiate the read. The MSB of this register address byte will indicate "0" when writing to the register and "1" when reading from the register. Upon receiving the address, the accelerometer returns the 8-bit data stored in the addressed register. This operation also occurs over 16 clock cycles. All returned data is sent MSB first, and the host must return nCS HIGH for at least one clock cycle before the next data request. Figure 6 shows the timing diagram for an 8-bit register read operation.

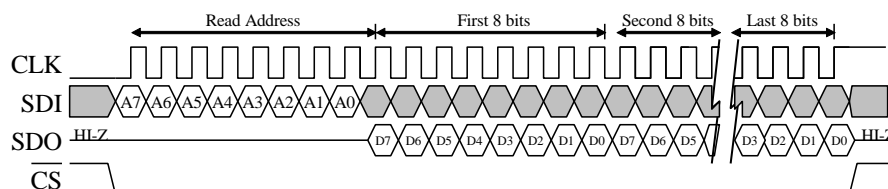
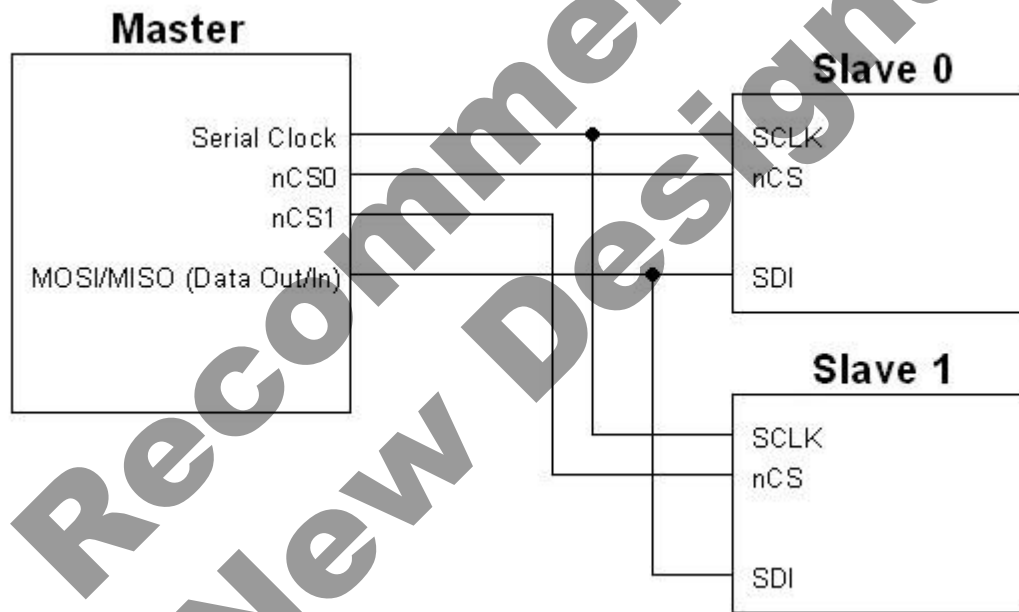


Figure 6: Timing Diagram for 8-Bit Register Read Operation

|   |   |  |
|---|---|--|
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|---|---|--|

### 3-Wire SPI Interface

The KX112 also utilizes an integrated 3-Wire Serial Peripheral Interface (SPI) for digital communication. 3-wire SPI is a synchronous serial interface that uses two control lines and one data line. With respect to the Master, the Serial Clock output (SCLK), the Data Output/Input (SDI) are shared among the Slave devices. The Master generates an independent Chip Select ( $nCS$ ) for each Slave device that goes LOW at the start of transmission and goes back HIGH at the end. This allows multiple Slave devices to share a master SPI port as shown in Figure 7 below.



**Figure 7: 3-wire SPI Connections**



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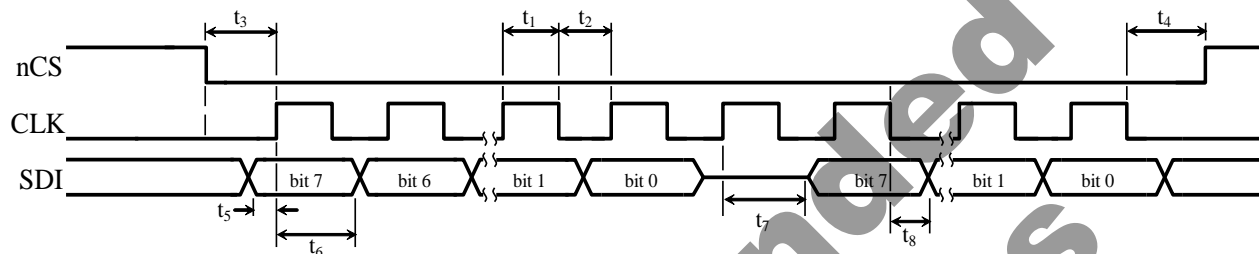
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## **3-Wire SPI Timing Diagram**



| Number         | Description   | MIN | MAX | Units |
|----------------|---|-----|-----|-------|
| t <sub>1</sub> | CLK pulse width: HIGH   | 40  | -   | ns    |
| t <sub>2</sub> | CLK pulse width: LOW  | 40  | -   | ns    |
| t <sub>3</sub> | nCS LOW to first CLK rising edge                              | 20  | -   | ns    |
| t <sub>4</sub> | nCS LOW after the final CLK falling edge                      | 20  | -   | ns    |
| t <sub>5</sub> | SDI valid to CLK rising edge                                  | 10  | -   | ns    |
| t <sub>6</sub> | CLK rising edge to SDI input invalid                          | 10  | -   | ns    |
| t <sub>7</sub> | CLK extra clock cycle rising edge to SDI output becomes valid | -   | -   | ns    |
| t <sub>8</sub> | CLK falling edge to SDI output becomes valid                  | -   | 35  | ns    |

**Table 10: 3-Wire SPI Timing**

## **Notes**

1. t<sub>7</sub> and t<sub>8</sub> are only present during reads.
2. Timings are for VDD of 1.8V to 3.6V with 1kΩ pull-up resistor and maximum 20pF load capacitor on SDI.
3. The SDO/ADDR pin is configured in a high-impedance input-state, and must be externally tied to GND or IO\_VDD



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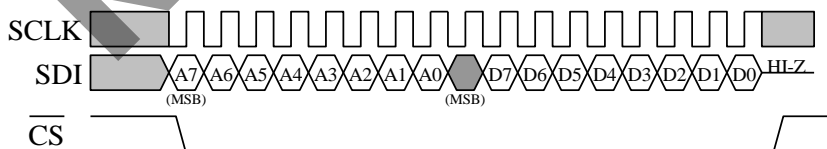
## **3-Wire Read and Write Registers**

The registers embedded in the KX112 accelerometer have 8-bit addresses. Upon power up, the Master must write to the accelerometer's control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate "0" when writing to the register and "1" when reading from the register. A read operation occurs over 17 clock cycles and a write operation occurs over 16 clock cycles. All commands are sent MSB first. The host must return nCS HIGH for at least one clock cycle before the next data request. However, when data is being read from a buffer read register (BUF\_READ), the nCS signal can remain LOW until the buffer is read. Figure 8 below shows the timing diagram for carrying out an 8-bit register write operation.



**Figure 8: Timing Diagram for 8-Bit Register Write Operation**

In order to read an 8-bit register, an 8-bit register address must be written to the accelerometer to initiate the read. The MSB of this register address byte will indicate "0" when writing to the register and "1" when reading from the register. Upon receiving the address, the accelerometer returns the 8-bit data stored in the addressed register. For 3-wire read operations, one extra clock cycle between the address byte and the data output byte is required. Therefore, this operation occurs over 17 clock cycles. All returned data is sent MSB first, and the host must return nCS HIGH for at least one clock cycle before the next data request. Figure 9 shows the timing diagram for an 8-bit register read operation.



**Figure 9: Timing Diagram for 8-Bit Register Read Operation**



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## Embedded Registers


The KX112 has 57 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and describes bit functions of each register. Table 11 below provides a listing of the accessible 8-bit registers and their addresses.

| Address | Register Name   | R/W | Address | Register Name   | R/W |
|---------|-----------------|-----|---------|-----------------|-----|
| 0x00    | XHPL            | R   | 0x21    | INC6*           | R/W |
| 0x01    | XHPH            | R   | 0x22    | TILT_TIMER*     | R/W |
| 0x02    | YHPL            | R   | 0x23    | WUFC*           | R/W |
| 0x03    | YHPH            | R   | 0x24    | TDTRC*          | R/W |
| 0x04    | ZHPL            | R   | 0x25    | TDTC*           | R/W |
| 0x05    | ZHPH            | R   | 0x26    | TTH*            | R/W |
| 0x06    | XOUTL           | R   | 0x27    | TTL*            | R/W |
| 0x07    | XOUTH           | R   | 0x28    | FTD*            | R/W |
| 0x08    | YOUTL           | R   | 0x29    | STD*            | R/W |
| 0x09    | YOUTH           | R   | 0x2A    | TLT*            | R/W |
| 0x0A    | ZOUTL           | R   | 0x2B    | TWS*            | R/W |
| 0x0B    | ZOUTH           | R   | 0x2C    | FFTH*           | R/W |
| 0x0C    | COTR            | R   | 0x2D    | FFC*            | R/W |
| 0x0D    | Kionix Reserved |     | 0x2E    | FFCNTL*         | R/W |
| 0x0E    | Kionix Reserved |     | 0x2F    | Kionix Reserved |     |
| 0x0F    | WHO_AM_I        | R   | 0x30    | ATH*            | R/W |
| 0x10    | TSCP            | R   | 0x31    | Kionix Reserved |     |
| 0x11    | TSPP            | R   | 0x32    | TILT_ANGLE_LL*  | R/W |
| 0x12    | INS1            | R   | 0x33    | TILT_ANGLE_HL*  | R/W |
| 0x13    | INS2            | R   | 0x34    | HYST_SET*       | R/W |
| 0x14    | INS3            | R   | 0x35    | LP_CNTL*        | R/W |
| 0x15    | STAT            | R   | 0x36    | Kionix Reserved |     |
| 0x16    | Kionix Reserved |     | 0x37    | Kionix Reserved |     |
| 0x17    | INT_REL         | R   | 0x38    | Kionix Reserved |     |
| 0x18    | CNTL1*          | R/W | 0x39    | Kionix Reserved |     |
| 0x19    | CNTL2*          | R/W | 0x3A    | BUF_CNTL1*      | R/W |
| 0x1A    | CNTL3*          | R/W | 0x3B    | BUF_CNTL2*      | R/W |
| 0x1B    | ODCNTL*         | R/W | 0x3C    | BUF_STATUS_1    | R   |
| 0x1C    | INC1*           | R/W | 0x3D    | BUF_STATUS_2    | R   |
| 0x1D    | INC2*           | R/W | 0x3E    | BUF_CLEAR       | W   |
| 0x1E    | INC3*           | R/W | 0x3F    | BUF_READ        | R   |
| 0x1F    | INC4*           | R/W | 0x60    | SELF_TEST       | W   |
| 0x20    | INC5*           | R/W |         |                 |     |

\* Note:

- When changing the contents of these registers, the PC1 bit in CNTL1 register must first be set to "0".
- Reserved registers should not be written.

Table 11: Register Map

|   |   |   |
|---|---|---|
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## Register Descriptions

### Accelerometer Outputs

These registers contain up to 16-bits of valid acceleration data for each axis. However, the user may choose to read only the 8 MSB thus reading an effective 8-bit resolution. When BRES = 0 in BUF\_CNTL2 register, the 8 MSB is the only data recorded in the buffer. The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per Table 12 below. The register acceleration output binary data is represented in 2's complement format. For example, if N = 16 bits, then the Counts range is from -32768 to 32767, and if N = 8 bits, then the Counts range is from -128 to 127.

| 16-bit Register Data (2's complement) | Equivalent Counts in decimal | Range = ±2g | Range = ±4g | Range = ±8g |
|---------------------------------------|------------------------------|-------------|-------------|-------------|
| 0111 1111 1111 1111                   | 32767                        | +1.99994g   | +3.99988g   | +7.99976g   |
| 0111 1111 1111 1110                   | 32766                        | +1.99988g   | +3.99976g   | +7.99951g   |
| ...                                   | ...                          | ...         | ...         | ...         |
| 0000 0000 0000 0001                   | 1                            | +0.00006g   | +0.00012g   | +0.00024g   |
| 0000 0000 0000 0000                   | 0                            | 0.00000g    | 0.00000g    | 0.00000g    |
| 1111 1111 1111 1111                   | -1                           | -0.00006g   | -0.00012g   | -0.00024g   |
| ...                                   | ...                          | ...         | ...         | ...         |
| 1000 0000 0000 0001                   | -32767                       | -1.99994g   | -3.99988g   | -7.99976g   |
| 1000 0000 0000 0000                   | -32768                       | -2.00000g   | -4.00000g   | -8.00000g   |

| 8-bit Register Data (2's complement) | Equivalent Counts in decimal | Range = ±2g | Range = ±4g | Range = ±8g |
|--------------------------------------|------------------------------|-------------|-------------|-------------|
| 0111 1111                            | 127                          | +1.98438g   | +3.96875g   | +7.93750g   |
| 0111 1110                            | 126                          | +1.96875g   | +3.93750g   | +7.87500g   |
| ...                                  | ...                          | ...         | ...         | ...         |
| 0000 0001                            | 1                            | +0.01563g   | +0.03125g   | +0.06250g   |
| 0000 0000                            | 0                            | 0.0000g     | 0.0000g     | 0.0000g     |
| 1111 1111                            | -1                           | -0.01563g   | -0.03125g   | -0.06250g   |
| ...                                  | ...                          | ...         | ...         | ...         |
| 1000 0001                            | -127                         | -1.98438g   | -3.96875g   | -7.93750g   |
| 1000 0000                            | -128                         | -2.00000g   | -4.00000g   | -8.00000g   |

**Table 12: Acceleration (g) Calculation**



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## XHP\_L

X-axis high-pass filter accelerometer output least significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3 register. Data is only available when wake-up engine is enabled (WUFE = 1 in CNTL1 register)

|               |       |       |       |       |       |       |       |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R             | R     | R     | R     | R     | R     | R     | R     |
| XHPD7         | XHPD6 | XHPD5 | XHPD4 | XHPD3 | XHPD2 | XHPD1 | XHPD0 |
| Bit7          | Bit6  | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  |
| Address: 0x00 |       |       |       |       |       |       |       |

## XHP\_H

X-axis high-pass filter accelerometer output most significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3 register. Data is only available when wake-up engine is enabled (WUFE = 1 in CNTL1 register)

|               |        |        |        |        |        |       |       |
|---------------|--------|--------|--------|--------|--------|-------|-------|
| R             | R      | R      | R      | R      | R      | R     | R     |
| XHPD15        | XHPD14 | XHPD13 | XHPD12 | XHPD11 | XHPD10 | XHPD9 | XHPD8 |
| Bit7          | Bit6   | Bit5   | Bit4   | Bit3   | Bit2   | Bit1  | Bit0  |
| Address: 0x01 |        |        |        |        |        |       |       |

## YHP\_L

Y-axis high-pass filter accelerometer output least significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3 register. Data is only available when wake-up engine is enabled (WUFE = 1 in CNTL1 register)

|               |       |       |       |       |       |       |       |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R             | R     | R     | R     | R     | R     | R     | R     |
| YHPD7         | YHPD6 | YHPD5 | YHPD4 | YHPD3 | YHPD2 | YHPD1 | YHPD0 |
| Bit7          | Bit6  | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  |
| Address: 0x02 |       |       |       |       |       |       |       |

## YHP\_H

Y-axis high-pass filter accelerometer output most significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3 register. Data is only available when wake-up engine is enabled (WUFE = 1 in CNTL1 register)

|               |        |        |        |        |        |       |       |
|---------------|--------|--------|--------|--------|--------|-------|-------|
| R             | R      | R      | R      | R      | R      | R     | R     |
| YHPD15        | YHPD14 | YHPD13 | YHPD12 | YHPD11 | YHPD10 | YHPD9 | YHPD8 |
| Bit7          | Bit6   | Bit5   | Bit4   | Bit3   | Bit2   | Bit1  | Bit0  |
| Address: 0x03 |        |        |        |        |        |       |       |





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## **ZHP\_L**

Z-axis high-pass filter accelerometer output least significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3 register. Data is only available when wake-up engine is enabled (WUFE = 1 in CNTL1 register)

|               |       |       |       |       |       |       |       |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R             | R     | R     | R     | R     | R     | R     | R     |
| ZHPD7         | ZHPD6 | ZHPD5 | ZHPD4 | ZHPD3 | ZHPD2 | ZHPD1 | ZHPD0 |
| Bit7          | Bit6  | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  |
| Address: 0x04 |       |       |       |       |       |       |       |

## **ZHP\_H**

Z-axis high-pass filter accelerometer output most significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3 register. Data is only available when wake-up engine is enabled (WUFE = 1 in CNTL1 register)

|               |        |        |        |        |        |       |       |
|---------------|--------|--------|--------|--------|--------|-------|-------|
| R             | R      | R      | R      | R      | R      | R     | R     |
| ZHPD15        | ZHPD14 | ZHPD13 | ZHPD12 | ZHPD11 | ZHPD10 | ZHPD9 | ZHPD8 |
| Bit7          | Bit6   | Bit5   | Bit4   | Bit3   | Bit2   | Bit1  | Bit0  |
| Address: 0x05 |        |        |        |        |        |       |       |

## **XOUT\_L**

X-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

|               |        |        |        |        |        |        |        |
|---------------|--------|--------|--------|--------|--------|--------|--------|
| R             | R      | R      | R      | R      | R      | R      | R      |
| XOUTD7        | XOUTD6 | XOUTD5 | XOUTD4 | XOUTD3 | XOUTD2 | XOUTD1 | XOUTD0 |
| Bit7          | Bit6   | Bit5   | Bit4   | Bit3   | Bit2   | Bit1   | Bit0   |
| Address: 0x06 |        |        |        |        |        |        |        |

## **XOUT\_H**

X-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

|               |         |         |         |         |         |        |        |
|---------------|---------|---------|---------|---------|---------|--------|--------|
| R             | R       | R       | R       | R       | R       | R      | R      |
| XOUTD15       | XOUTD14 | XOUTD13 | XOUTD12 | XOUTD11 | XOUTD10 | XOUTD9 | XOUTD8 |
| Bit7          | Bit6    | Bit5    | Bit4    | Bit3    | Bit2    | Bit1   | Bit0   |
| Address: 0x07 |         |         |         |         |         |        |        |



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## **YOUT\_L**

Y-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

|               |        |        |        |        |        |        |        |
|---------------|--------|--------|--------|--------|--------|--------|--------|
| R             | R      | R      | R      | R      | R      | R      | R      |
| YOUTD7        | YOUTD6 | YOUTD5 | YOUTD4 | YOUTD3 | YOUTD2 | YOUTD1 | YOUTD0 |
| Bit7          | Bit6   | Bit5   | Bit4   | Bit3   | Bit2   | Bit1   | Bit0   |
| Address: 0x08 |        |        |        |        |        |        |        |

## **YOUT\_H**

Y-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

|               |         |         |         |         |         |        |        |
|---------------|---------|---------|---------|---------|---------|--------|--------|
| R             | R       | R       | R       | R       | R       | R      | R      |
| YOUTD15       | YOUTD14 | YOUTD13 | YOUTD12 | YOUTD11 | YOUTD10 | YOUTD9 | YOUTD8 |
| Bit7          | Bit6    | Bit5    | Bit4    | Bit3    | Bit2    | Bit1   | Bit0   |
| Address: 0x09 |         |         |         |         |         |        |        |

## **ZOUT\_L**

Z-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

|               |        |        |        |        |        |        |        |
|---------------|--------|--------|--------|--------|--------|--------|--------|
| R             | R      | R      | R      | R      | R      | R      | R      |
| ZOUTD7        | ZOUTD6 | ZOUTD5 | ZOUTD4 | ZOUTD3 | ZOUTD2 | ZOUTD1 | ZOUTD0 |
| Bit7          | Bit6   | Bit5   | Bit4   | Bit3   | Bit2   | Bit1   | Bit0   |
| Address: 0x0A |        |        |        |        |        |        |        |

## **ZOUT\_H**

Z-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA bits in ODCNTL register.

|               |         |         |         |         |         |        |        |
|---------------|---------|---------|---------|---------|---------|--------|--------|
| R             | R       | R       | R       | R       | R       | R      | R      |
| ZOUTD15       | ZOUTD14 | ZOUTD13 | ZOUTD12 | ZOUTD11 | ZOUTD10 | ZOUTD9 | ZOUTD8 |
| Bit7          | Bit6    | Bit5    | Bit4    | Bit3    | Bit2    | Bit1   | Bit0   |
| Address: 0x0B |         |         |         |         |         |        |        |



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## **COTR**

The Command Test Response (COTR) register is used to verify proper integrated circuit functionality. The value of this register will change from a default value of 0x55 to 0xAA when COTC bit in CNTL2 register is set. After reading 0xAA from this register, the byte value returns to the default value of 0x55 and COTC bit in CNTL2 register is cleared.

|               |        |        |        |        |        |        |        |             |
|---------------|--------|--------|--------|--------|--------|--------|--------|-------------|
| R             | R      | R      | R      | R      | R      | R      | R      |             |
| DCSTR7        | DCSTR6 | DCSTR5 | DCSTR4 | DCSTR3 | DCSTR2 | DCSTR1 | DCSTR0 | Reset Value |
| Bit7          | Bit6   | Bit5   | Bit4   | Bit3   | Bit2   | Bit1   | Bit0   | 01010101    |
| Address: 0x0C |        |        |        |        |        |        |        |             |

## **WHO\_AM\_I**

This register is used for supplier recognition, as it is factory written to a known byte value. The default value is 0x22.

|               |      |      |      |      |      |      |      |             |
|---------------|------|------|------|------|------|------|------|-------------|
| R             | R    | R    | R    | R    | R    | R    | R    |             |
| WIA7          | WIA6 | WIA5 | WIA4 | WIA3 | WIA2 | WIA1 | WIA0 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00100010    |
| Address: 0x0F |      |      |      |      |      |      |      |             |



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## **Tilt Position Registers**

These two registers report previous and current position data that is updated at the user-defined ODR frequency OTP<1:0> in CNTL3 register. Data protected during register read. Table 13 describes the reported position for each bit value.

### **TSCP**

The Tilt Status Current Position (TSCP) register reports the current tilt position.

|               |      |      |      |      |      |      |      |             |
|---------------|------|------|------|------|------|------|------|-------------|
| R             | R    | R    | R    | R    | R    | R    | R    |             |
| 0             | 0    | LE   | RI   | DO   | UP   | FD   | FU   | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00100000    |
| Address: 0x10 |      |      |      |      |      |      |      |             |

### **TSPP**

The Tilt Status Previous Position (TSPP) register reports previous tilt position.

|               |      |      |      |      |      |      |      |             |
|---------------|------|------|------|------|------|------|------|-------------|
| R             | R    | R    | R    | R    | R    | R    | R    |             |
| 0             | 0    | LE   | RI   | DO   | UP   | FD   | FU   | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00100000    |
| Address: 0x11 |      |      |      |      |      |      |      |             |

| Bit | Description          |
|-----|----------------------|
| LE  | Left State (X-)      |
| RI  | Right State (X+)     |
| DO  | Down State (Y-)      |
| UP  | Up State (Y+)        |
| FD  | Face-Down State (Z-) |
| FU  | Face-Up State (Z+)   |

**Table 13: Tilt Position**



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## Interrupt Source Registers

These three registers report interrupt state changes. This data is updated when a new interrupt event occurs and each application's result is latched until the interrupt release register is read.

### INS1

The Interrupt Source 1 (INS1) register indicates the triggering axis when a Tap/Double-Tap™ interrupt occurs. Data is updated at the ODR settings determined by OTDT<2:0> bits in CNTL3 register.

|               |      |      |      |      |      |      |      |
|---------------|------|------|------|------|------|------|------|
| R             | R    | R    | R    | R    | R    | R    | R    |
| 0             | 0    | TLE  | TRI  | TDO  | TUP  | TFD  | TFU  |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| Address: 0x12 |      |      |      |      |      |      |      |

| Bit | Description              |
|-----|--------------------------|
| TLE | X Negative (X-) Reported |
| TRI | X Positive (X+) Reported |
| TDO | Y Negative (Y-) Reported |
| TUP | Y Positive (Y+) Reported |
| TFD | Z Negative (Z-) Reported |
| TFU | Z Positive (Z+) Reported |

**Table 14:** Directional-Tap™ Reporting

### INS2

The Interrupt Source 2 (INS2) register reports which function caused an interrupt.

|               |      |      |      |       |       |      |      |
|---------------|------|------|------|-------|-------|------|------|
| R             | R    | R    | R    | R     | R     | R    | R    |
| FFS           | BFI  | WMI  | DRDY | TDTS1 | TDTS0 | WUFS | TPS  |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3  | Bit2  | Bit1 | Bit0 |
| Address: 0x13 |      |      |      |       |       |      |      |

**FFS** – Free fall. This bit is cleared when the interrupt latch release register (INT\_REL) is read.

FFS = 0 – No Free fall

FFS = 1 – Free fall has activated the interrupt

**BFI** – Buffer Full Interrupt. Automatically cleared when at least one sample is read from the buffer or following the write to BUF\_CLEAR register.

BFI = 0 – Buffer is not full

BFI = 1 – Buffer is full



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**WMI** – The Watermark Interrupt bit is set to 1 when FIFO has filled up to the value stored in the SMP\_TH <9:0> bits. This bit is automatically cleared when FIFO is read and the SMP\_LEV<10:0> returns to a value below the value stored in the SMP\_TH <9:0> bits, or following the write to BUF\_CLEAR register.

WMI = 0 – Buffer watermark has not been exceeded

WMI = 1 – Buffer watermark has been exceeded

**DRDY** – The Data Ready bit indicates that new acceleration data (0x06 to 0x0B) is available. This bit is cleared when acceleration data is read or the interrupt release register INT\_REL is read.

DRDY = 0 – new acceleration data not available

DRDY = 1 – new acceleration data available

**TDTS1, TDTS0** – The Tap/Double-Tap™ Status bits indicate whether a tap event has occurred and what kind. The status bits are cleared when interrupt release register INT\_REL is read.

| TDTS1 | TDTS0 | Event      |
|-------|-------|------------|
| 0     | 0     | No Tap     |
| 0     | 1     | Single Tap |
| 1     | 0     | Double-Tap |
| 1     | 1     | undefined  |

**WUFS** – The Wake-Up Function Status bit is cleared when the interrupt release register INT\_REL is read.

WUFS = 0 – No motion

WUFS = 1 – Motion has activated the interrupt

**TPS** – The Tilt Position Status bit is cleared when the interrupt release register INT\_REL is read.

TPS = 0 – Position has not changed

TPS = 1 – Position has changed



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## INS3

The Interrupt Source 3 (INS3) register reports the axis and direction of detected motion.

|               |      |      |      |      |      |      |      |
|---------------|------|------|------|------|------|------|------|
| R             | R    | R    | R    | R    | R    | R    | R    |
| 0             | 0    | XNWU | XPWU | YNWU | YPWU | ZNWU | ZPWU |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| Address: 0x14 |      |      |      |      |      |      |      |

| Bit  | Description              |
|------|--------------------------|
| XNWU | X Negative (X-) Reported |
| XPWU | X Positive (X+) Reported |
| YNWU | Y Negative (Y-) Reported |
| YPWU | Y Positive (Y+) Reported |
| ZNWU | Z Negative (Z-) Reported |
| ZPWU | Z Positive (Z+) Reported |

Table 15: Motion Detection Reporting

## STATUS\_REG

The Status Register reports the status of whether the interrupt is present.

|               |      |      |      |      |      |      |      |
|---------------|------|------|------|------|------|------|------|
| R             | R    | R    | R    | R    | R    | R    | R    |
| 0             | 0    | 0    | INT  | 0    | 0    | 0    | 0    |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| Address: 0x15 |      |      |      |      |      |      |      |

**INT** – The INT bit reports the combined (OR) interrupt information of all features. If BFI and WMI bits in INS2 register are 0, the INT bit is set to 0 when INT\_REL register is read. If WMI or BFI bit in INS2 register is 1, INT bit remains at 1 until these bits are cleared by FIFO/FILO buffer read.

INT = 0 – no interrupt event

INT = 1 – interrupt event has occurred



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## INT\_REL

Interrupt Release (INT\_REL) register: Latched interrupt source information reported in INS1, INS2, and INS3 registers is cleared and physical interrupt latched pin is changed to its inactive state when this register is read. However, WMI and BFI bits in INS2 register are not cleared by this command. Furthermore, INT bit in STATUS\_REG will not be cleared by reading this register if WMI or BFI bits in INS2 register are set to 1. Read value is dummy.

|               |      |      |      |      |      |      |      |
|---------------|------|------|------|------|------|------|------|
| R             | R    | R    | R    | R    | R    | R    | R    |
| X             | X    | X    | X    | X    | X    | X    | X    |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| Address: 0x17 |      |      |      |      |      |      |      |

## CNTL1

The Control 1 (CNTL1) register controls the main feature set of the accelerometer.

|               |      |       |       |       |      |      |      |             |
|---------------|------|-------|-------|-------|------|------|------|-------------|
| R/W           | R/W  | R/W   | R/W   | R/W   | R/W  | R/W  | R/W  |             |
| PC1           | RES  | DRDYE | GSEL1 | GSEL0 | TDTE | WUFE | TPE  | Reset Value |
| Bit7          | Bit6 | Bit5  | Bit4  | Bit3  | Bit2 | Bit1 | Bit0 | 00000000    |
| Address: 0x18 |      |       |       |       |      |      |      |             |

**PC1** – The PC1 bit controls the operating mode of the KX112. Note, when configuration changes need to be made, please allow 2/ODR (sec) delay time after setting PC1=0 (i.e. transitioning from operating mode to standby mode)

PC1 = 0 – Standby mode

PC1 = 1 – operating mode (Low Power or High Resolution)

**RES** – The RES bit determines the performance mode of the KX112. The noise varies with ODR, RES and different LP\_CNTL settings possibly reducing the effective resolution. Note that to change the value of this bit, the PC1 bit must first be set to “0”.

RES = 0 – Low Power mode (higher noise, lower current, 16-bit output data)

RES = 1 – High Resolution mode (lower noise, higher current, 16-bit output data)

**DRDYE** – The Data Ready Enable bit enables the reporting of the availability of new acceleration data as an interrupt. Note that to change the value of this bit, the PC1 bit must first be set to “0”.

DRDYE = 0 – availability of new acceleration data is not reflected as an interrupt

DRDYE = 1 – availability of new acceleration data is reflected as an interrupt





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**GSEL1, GSEL0** – The G-Select bits allow to select the acceleration range of the accelerometer outputs per Table 16. Note that to change the value of this bit, the PC1 bit must first be set to “0”.

| GSEL1 | GSEL0 | Range |
|-------|-------|-------|
| 0     | 0     | ±2g   |
| 0     | 1     | ±4g   |
| 1     | 0     | ±8g   |

**Table 16:** Selected Acceleration Range

**TDTE** – The Tap/Double-Tap™ Enable bit enables the Directional-Tap™ function that will detect single and double tap events. Note that to change the value of this bit, the PC1 bit must first be set to “0”.

TDTE = 0 – Tap/Double-Tap™ disabled

TDTE = 1 – Tap/Double-Tap™ enabled

**WUFE** – The Wake-up Function Enable bit enables the Wake-Up (motion detect) function. Note that to change the value of this bit, the PC1 bit must first be set to “0”.

WUFE = 0 – Wake-Up function disabled

WUFE = 1 – Wake-Up function enabled

**TPE** – The Tilt Position Enable bit enables the Tilt Position function that will detect changes in device orientation. Note that to change the value of this bit, the PC1 bit must first be set to “0”.

TPE = 0 – Tilt Position function disabled

TPE = 1 – Tilt Position function enabled



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## CNTL2

The Control 2 (CNTL2) register provides additional feature set control. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| SRST          | COTC | LEM  | RIM  | DOM  | UPM  | FDM  | FUM  | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00111111    |
| Address: 0x19 |      |      |      |      |      |      |      |             |

**SRST** – The Software Reset bit initiates software reset, which performs the RAM reboot routine. This bit will remain 1 until the RAM reboot routine is finished. Please refer to Technical Note [TN004 Power-On Procedure](#) for more information on software reset.

SRST = 0 – no action

SRST = 1 – start RAM reboot routine

**COTC** – The Command Test Control bit is used to verify proper ASIC functionality.

COTC = 0 – no action

COTC = 1 – sets COTR register to 0xAA. When COTR register is then read, sets COTC bit to 0 and sets COTR register to 0x55.

**LEM, RIM, DOM, UPM, FDM, FUM** – these bits control the tilt axis mask. Per Table 17, if a direction's bit is set to one (1), tilt in that direction will generate an interrupt. If it is set to zero (0), tilt in that direction will not generate an interrupt.

| Bit | Description                 |
|-----|-----------------------------|
| LEM | Left state enable (X-)      |
| RIM | Right state enable (X+)     |
| DOM | Down state enable (Y-)      |
| UPM | Up state enable (Y+)        |
| FDM | Face-Down state enable (Z-) |
| FUM | Face-Up state enable (Z+)   |

**Table 17: Tilt Direction Axis Mask**



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## **CNTL3**

The Control 3 (CNTL3) register sets the output data rates for Tilt, Directional-Tap™, and the Motion Wake-Up digital engines. The output data rate set in this register and the averaging filter control settings set in LP\_CNTL register, will influence overall performance of the digital engines and the power consumption of the accelerometer. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W  | R/W  | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | Reset Value |
|------|------|-------|-------|-------|-------|-------|-------|-------------|
| OTP1 | OTP0 | OTDT2 | OTDT1 | OTDT0 | OWUF2 | OWUF1 | OWUF0 | 10011000    |
| Bit7 | Bit6 | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  |             |

Address: 0x1A

**OTP1, OTP0** – The ODR Tilt bits set the output data rate for the Tilt Position function per Table 18. The default Tilt Position ODR is 12.5Hz.

| OTP1 | OTP0 | Output Data Rate |
|------|------|------------------|
| 0    | 0    | 1.563Hz          |
| 0    | 1    | 6.25Hz           |
| 1    | 0    | 12.5Hz           |
| 1    | 1    | 50Hz             |

**Table 18:** Tilt Position Function Output Data Rate

**OTDT2, OTDT1, OTDT0** – The ODR Tap/Double-Tap™ bits set the output data rate for the Directional-Tap™ function per Table 19. The default Directional-Tap™ ODR is 400Hz.

| OTDT2 | OTDT1 | OTDT0 | Output Data Rate |
|-------|-------|-------|------------------|
| 0     | 0     | 0     | 50Hz             |
| 0     | 0     | 1     | 100Hz            |
| 0     | 1     | 0     | 200Hz            |
| 0     | 1     | 1     | 400Hz            |
| 1     | 0     | 0     | 12.5Hz           |
| 1     | 0     | 1     | 25Hz             |
| 1     | 1     | 0     | 800Hz            |
| 1     | 1     | 1     | 1600Hz           |

**Table 19:** Directional-Tap™ Function Output Data Rate



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**OWUF2, OWUF1, OWUF0** – The ODR Wake-Up Function bits set the output data rate for the general motion detection function and the high-pass filtered outputs per Table 20. The default Motion Wake-Up ODR is 0.781Hz.

| OWUF2 | OWUF1 | OWUF0 | Output Data Rate |
|-------|-------|-------|------------------|
| 0     | 0     | 0     | 0.781Hz          |
| 0     | 0     | 1     | 1.563Hz          |
| 0     | 1     | 0     | 3.125Hz          |
| 0     | 1     | 1     | 6.250Hz          |
| 1     | 0     | 0     | 12.5Hz           |
| 1     | 0     | 1     | 25Hz             |
| 1     | 1     | 0     | 50Hz             |
| 1     | 1     | 1     | 100Hz            |

**Table 20:** Motion Wake-Up Function Output Data Rate

|   |   |  |
|---|---|--|
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|---|---|--|

## ODCNTL

The ODR Control (ODCNTL) register is responsible for configuring Output Data Rate (ODR) and low-pass filter settings. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W      | R/W      | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|----------|----------|------|------|------|------|-------------|
| IIR_BYPASS    | LPRO | RESERVED | RESERVED | OSA3 | OSA2 | OSA1 | OSA0 | Reset Value |
| Bit7          | Bit6 | Bit5     | Bit4     | Bit3 | Bit2 | Bit1 | Bit0 | 00000010    |
| Address: 0x1B |      |          |          |      |      |      |      |             |

### **IIR\_BYPASS** filter bypass mode

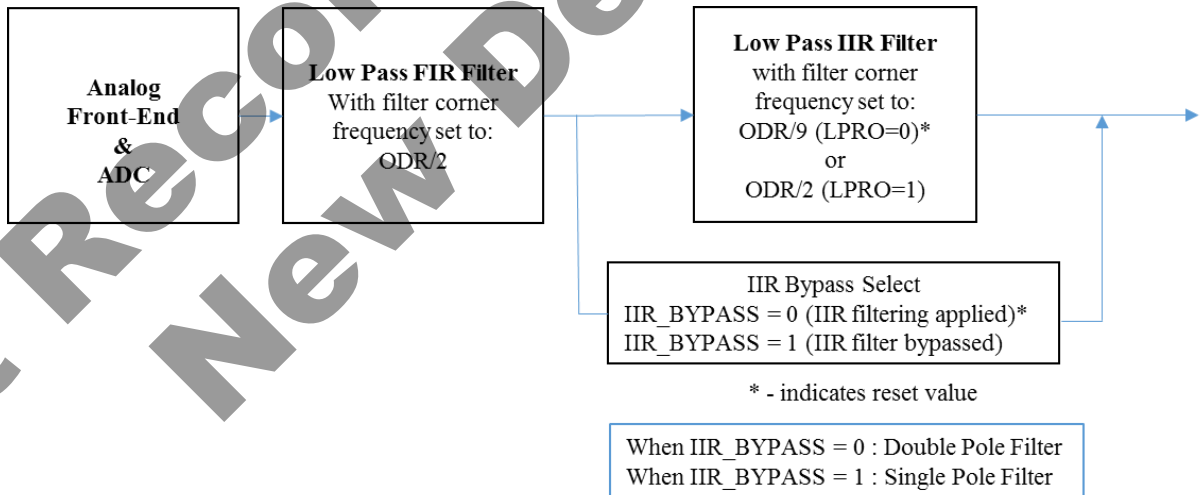
*IIR\_BYPASS = 0 – filtering applied (default)*

*IIR\_BYPASS = 1 – filter bypassed. This setting may reduce the resolution of the output data.*

### **LPRO** low-pass filter roll off control

*LPRO = 0 – filter corner frequency set to ODR/9 (default)*

*LPRO = 1 – filter corner frequency set to ODR/2*



**Figure 10: Low-Pass Filter Design and Control Circuitry**



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**OSA3, OSA2, OSA1, OSA0** – The OSA <3:0> bits set the acceleration output data rate (ODR). The default ODR is 50Hz.

| OSA3 | OSA2 | OSA1 | OSA0 | Output Data Rate |
|------|------|------|------|------------------|
| 0    | 0    | 0    | 0    | 12.5Hz*          |
| 0    | 0    | 0    | 1    | 25Hz*            |
| 0    | 0    | 1    | 0    | 50Hz*            |
| 0    | 0    | 1    | 1    | 100Hz*           |
| 0    | 1    | 0    | 0    | 200Hz*           |
| 0    | 1    | 0    | 1    | 400Hz**          |
| 0    | 1    | 1    | 0    | 800Hz            |
| 0    | 1    | 1    | 1    | 1600Hz           |
| 1    | 0    | 0    | 0    | 0.781Hz*         |
| 1    | 0    | 0    | 1    | 1.563Hz*         |
| 1    | 0    | 1    | 0    | 3.125Hz*         |
| 1    | 0    | 1    | 1    | 6.25Hz*          |
| 1    | 1    | 0    | 0    | 3200Hz           |
| 1    | 1    | 0    | 1    | 6400Hz           |
| 1    | 1    | 1    | 0    | 12800Hz          |
| 1    | 1    | 1    | 1    | 25600Hz          |

**Table 21:** Accelerometer Output Data Rates (ODR)

\* *Low Power* mode available, all other data rates will default to *High Resolution* mode

\*\* 400Hz *High Resolution* mode only (will not output in *Low Power* mode)



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### INC1

The Interrupt Control 1 (INC1) register controls the settings for the physical interrupt pin INT1, the Self-test function, and 3-wire SPI interface. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W     | R/W  | R/W  | R/W  | R/W      | R/W   | R/W   |             |
|---------------|---------|------|------|------|----------|-------|-------|-------------|
| PWSEL11       | PWSEL10 | IEN1 | IEA1 | IEL1 | Reserved | STPOL | SPI3E | Reset Value |
| Bit7          | Bit6    | Bit5 | Bit4 | Bit3 | Bit2     | Bit1  | Bit0  | 00010000    |
| Address: 0x1C |         |      |      |      |          |       |       |             |

**PWSEL1<1:0>** – Pulse interrupt 1 width configuration

00 = 50  $\mu$ sec (10  $\mu$ sec if OSA > 1600Hz)

01 = 1 \* OSA period

10 = 2 \* OSA periods

11 = 4 \* OSA periods

When PWSEL1 > 0, interrupt source auto-clearing (ACLR1=1) should be set to keep consistency between the internal status and the physical interrupt.

**IEN1** enables/disables the physical interrupt pin INT1

IEN1 = 0 – physical interrupt pin is disabled

IEN1 = 1 – physical interrupt pin is enabled

**IEA1** sets the polarity of the physical interrupt pin INT1

IEA1 = 0 – polarity of the physical interrupt pin is active LOW

IEA1 = 1 – polarity of the physical interrupt pin is active HIGH

**IEL1** sets the response of the physical interrupt pin INT1

IEL1 = 0 – the physical interrupt pin latches until it is cleared by reading INT\_REL.  
(excludes buffer full interrupt (BFI) and watermark interrupt (WMI)).

IEL1 = 1 – the physical interrupt pin will transmit one pulse configurable by PWSEL1

**STPOL** sets the polarity of Self-test

STPOL = 0 – Negative

STPOL = 1 – Positive

**SPI3E** sets the 3-wire SPI interface (set to 0 when I<sup>2</sup>C communication is used)

SPI3E = 0 – disabled

SPI3E = 1 – enabled



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### INC2

The Interrupt Control 2 (INC2) register controls which axis and direction of detected motion can cause an interrupt. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |             |
|---------------|------|-------|-------|-------|-------|-------|-------|-------------|
| 0             | AOI  | XNWUE | XPWUE | YNWUE | YPWUE | ZNWUE | ZPWUE | Reset Value |
| Bit7          | Bit6 | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  | 00111111    |
| Address: 0x1D |      |       |       |       |       |       |       |             |

**AOI** – AND-OR configuration on motion detection

0 – OR combination between selected directions

1 – AND combination between selected axes

Ex. If all directions are enabled,

Active state in OR configuration = (XN || XP || YN || YP || ZN || ZP)

Active state in AND configuration = (XN || XP) && (YN || YP) && (ZN || ZP)

**XNWU** – x negative (x-): 0 = disabled, 1 = enabled

**XPWU** – x positive (x+): 0 = disabled, 1 = enabled

**YNWU** – y negative (y-): 0 = disabled, 1 = enabled

**YPWU** – y positive (y+): 0 = disabled, 1 = enabled

**ZNWU** – z negative (z-): 0 = disabled, 1 = enabled

**ZPWU** – z positive (z+): 0 = disabled, 1 = enabled

### INC3

The Interrupt Control 3 (INC3) register controls which axis and direction of Tap/Double-Tap™ can cause an interrupt. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| 0             | 0    | TLEM | TRIM | TDOM | TUPM | TFDM | TFUM | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00111111    |
| Address: 0x1E |      |      |      |      |      |      |      |             |

**TLEM** – Tilt left state mask: 0 = disabled, 1 = enabled

**TRIM** – Tilt right state mask: 0 = disabled, 1 = enabled


**TDOM** – Tilt down state mask: 0 = disabled, 1 = enabled

**TUPM** – Tilt up state mask: 0 = disabled, 1 = enabled

**TFDM** – Tilt face-down state mask: 0 = disabled, 1 = enabled

**TFUM** – Tilt face-up state mask: 0 = disabled, 1 = enabled



|   |   |  |
|---|---|--|
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|---|---|--|

#### INC4

The Interrupt Control 4 (INC4) register controls routing of an interrupt reporting to physical interrupt pin INT1. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".

| R/W           | R/W  | R/W  | R/W    | R/W      | R/W   | R/W  | R/W  |             |
|---------------|------|------|--------|----------|-------|------|------|-------------|
| FFI1          | BFI1 | WMI1 | DRDYI1 | Reserved | TDTI1 | WUF1 | TPI1 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4   | Bit3     | Bit2  | Bit1 | Bit0 | 00000000    |
| Address: 0x1F |      |      |        |          |       |      |      |             |

**FFI1** – Free fall interrupt reported on physical interrupt INT1

**BFI1** – Buffer full interrupt reported on physical interrupt pin INT1

**WMI1** – Watermark interrupt reported on physical interrupt pin INT1

**DRDYI1** – Data ready interrupt reported on physical interrupt pin INT1

**TDTI1** – Tap/Double-Tap™ interrupt reported on physical interrupt pin INT1

**WUF1** – Wake-Up (motion detect) interrupt reported on physical interrupt pin INT1

**TPI1** – Tilt position interrupt reported on physical interrupt pin INT1

#### INC5

The Interrupt Control 5 (INC5) register controls the settings for the physical interrupt pin INT2. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".

| R/W           | R/W     | R/W  | R/W  | R/W  | R/W      | R/W   | R/W   |             |
|---------------|---------|------|------|------|----------|-------|-------|-------------|
| PWSEL21       | PWSEL20 | IEN2 | IEA2 | IEL2 | Reserved | ACLR2 | ACLR1 | Reset Value |
| Bit7          | Bit6    | Bit5 | Bit4 | Bit3 | Bit2     | Bit1  | Bit0  | 00010000    |
| Address: 0x20 |         |      |      |      |          |       |       |             |

**PWSEL2<1:0>** – Pulse interrupt 2 width configuration

00 = 50μsec (10μsec if OSA > 1600Hz)

01 = 1 \* OSA period

10 = 2 \* OSA periods

11 = 4 \* OSA periods

When PWSEL2 > 0, Interrupt source auto-clearing (ACLR2=1) is strongly recommended to keep consistency between the internal status and the physical interrupt.

**IEN2** enables/disables the physical interrupt pin INT2

IEN2 = 0 – physical interrupt pin is disabled

IEN2 = 1 – physical interrupt pin is enabled



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**IEA2** sets the polarity of the physical interrupt pin INT2

IEA2 = 0 – polarity of the physical interrupt pin is active LOW

IEA2 = 1 – polarity of the physical interrupt pin is active HIGH

**IEL2** sets the response of the physical interrupt pin INT2

IEL2 = 0 – the physical interrupt pin latches until it is cleared by reading INT\_REL.  
(excludes buffer full interrupt (BFI) and watermark interrupt (WMI)).

IEL2 = 1 – the physical interrupt pin will transmit one pulse configurable by PWSEL2

**ACLR2** – Latched interrupt source information(INS1-INS3) is cleared and physical interrupt-1 latched pin is changed to its inactive state at pulse interrupt-2 trailing edge. Note:  
WMI and BFI are not auto-cleared by a pulse interrupt trailing edge.

ACLR2 = 0 – disable

ACLR2 = 1 – enable

**ACLR1** – Latched interrupt source information(INS1-INS3) is cleared and physical interrupt-2 latched pin is changed to its inactive state at pulse interrupt-1 trailing edge. Note:  
WMI and BFI are not auto-cleared by a pulse interrupt trailing edge.

ACLR1 = 0 – disable

ACLR1 = 1 – enable

Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).

### INC6

The Interrupt Control 6 (INC6) register controls routing of interrupt reporting to physical interrupt pin INT2. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W  | R/W    | R/W      | R/W   | R/W   | R/W  |             |
|---------------|------|------|--------|----------|-------|-------|------|-------------|
| FFI2          | BFI2 | WMI2 | DRDYI2 | Reserved | TDTI2 | WUFI2 | TPI2 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4   | Bit3     | Bit2  | Bit1  | Bit0 | 00000000    |
| Address: 0x21 |      |      |        |          |       |       |      |             |

**FFI2** – Free fall interrupt reported on physical interrupt INT2

**BFI2** – Buffer full interrupt reported on physical interrupt pin INT2


**WMI2** – Watermark interrupt reported on physical interrupt pin INT2

**DRDYI2** – Data ready interrupt reported on physical interrupt pin INT2

**TDTI2** – Tap/Double-Tap™ interrupt reported on physical interrupt pin INT2

**WUFI2** – Wake-Up (motion detect) interrupt reported on physical interrupt pin INT2

**TPI2** – Tilt position interrupt reported on physical interrupt pin INT2

|   |   |  |
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*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

#### TILT\_TIMER

This register is the initial count register for the tilt position state timer (0 to 255 counts). Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 18. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| TSC7          | TSC6 | TSC5 | TSC4 | TSC3 | TSC2 | TSC1 | TSC0 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000    |
| Address: 0x22 |      |      |      |      |      |      |      |             |

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

#### WUFC

The Wake-Up Function Counter (WUFC) is the initial count register for the motion detection timer (0 to 255 counts). Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 20. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |             |
|---------------|-------|-------|-------|-------|-------|-------|-------|-------------|
| WUFC7         | WUFC6 | WUFC5 | WUFC4 | WUFC3 | WUFC2 | WUFC1 | WUFC0 | Reset Value |
| Bit7          | Bit6  | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  | 00000000    |
| Address: 0x23 |       |       |       |       |       |       |       |             |

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*



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## TDTRC

The Tap/Double-Tap™ Report Control (TDTRC) register is responsible for enabling/disabling reporting of Tap/Double-Tap™ events. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| 0             | 0    | 0    | 0    | 0    | 0    | DTRE | STRE | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000011    |
| Address: 0x24 |      |      |      |      |      |      |      |             |

**DTRE** – enables/disables the double tap interrupt

DTRE = 0 – do not update/trigger interrupts on Double-Tap™ events

DTRE = 1 – update interrupts on Double-Tap™ events

**STRE** – enables/disables single tap interrupt

STRE = 0 – do not update/trigger interrupts on single tap events

STRE = 1 – update interrupts on single tap events

## TDTC

The Tap/Double-Tap™ Counter (TDTC) register contains counter information for the detection of a double tap event. When the Directional-Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional-Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional-Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional-Tap™ ODR is user-defined per Table 19. The TDTC counts starts at the beginning of the first tap and it represents the minimum time separation between the first tap and the second tap in a double tap event. More specifically, the second tap event must end outside of the TDTC. The Kionix recommended default value is 0.3 seconds (0x78). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |             |
|---------------|-------|-------|-------|-------|-------|-------|-------|-------------|
| TDTC7         | TDTC6 | TDTC5 | TDTC4 | TDTC3 | TDTC2 | TDTC1 | TDTC0 | Reset Value |
| Bit7          | Bit6  | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  | 01111000    |
| Address: 0x25 |       |       |       |       |       |       |       |             |

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*



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## TTH

The Tap Threshold High (TTH) register represents the 8-bit jerk high threshold to determine if a tap is detected. The value is compared against the upper 8 bits of the 4g output value (independent of the actual g-range setting of the device). Though this is an 8-bit register, the register value is internally multiplied by two to set the high threshold. This multiplication results in a range of 0 to 510 with a resolution of two counts. The Performance Index (PI) is the jerk signal that is expected to be less than this threshold, but greater than the TTL threshold during single and double tap events. Equation 1 shows how to calculate the Performance Index. The Kionix recommended default value is 203 (0xCB). See *AN049 Getting Started* for recommended settings ([LINK](#)). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0"

$$X' = X \text{ (current)} - X \text{ (previous)}$$

$$Y' = Y \text{ (current)} - Y \text{ (previous)}$$

$$Z' = Z \text{ (current)} - Z \text{ (previous)}$$

$$PI = |X'| + |Y'| + |Z'|$$

Equation 1: Performance Index

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| TTH7          | TTH6 | TTH5 | TTH4 | TTH3 | TTH2 | TTH1 | TTH0 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 11001011    |
| Address: 0x26 |      |      |      |      |      |      |      |             |

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

## TTL

The Tap Threshold Low (TTL) register represents the 8-bit (0-255) jerk low threshold to determine if a tap is detected. The value is compared against the upper 8 bits of the 4g output value (independent of the actual g-range setting of the device). The Performance Index (PI) is the jerk signal that is expected to be greater than this threshold and less than the TTH threshold during single and double tap events. The Kionix recommended default value is 26 (0x1A). See *AN049 Getting Started* for recommended settings ([LINK](#)). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0"

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| TTL7          | TTL6 | TTL5 | TTL4 | TTL3 | TTL2 | TTL1 | TTL0 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00011010    |
| Address: 0x27 |      |      |      |      |      |      |      |             |



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*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

## FTD

This register contains counter information for the detection of any tap event. When the Directional-Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional-Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional-Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional-Tap™ ODR is user-defined per Table 19. To ensure that only tap events are detected, these time limits are used. A tap event must be above the performance index threshold for at least the low limit (FTDL0 – FTDL2) and no more than the high limit (FTDH0 – FTDH4). The Kionix recommended default value for the high limit is 0.05 seconds and for the low limit is 0.005 seconds (0xA2). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |             |
|---------------|-------|-------|-------|-------|-------|-------|-------|-------------|
| FTDH4         | FTDH3 | FTDH2 | FTDH1 | FTDH0 | FTDL2 | FTDL1 | FTDL0 | Reset Value |
| Bit7          | Bit6  | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  | 10100010    |
| Address: 0x28 |       |       |       |       |       |       |       |             |


*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

## STD

This register contains counter information for the detection of a double tap event. When the Directional-Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional-Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional-Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional-Tap™ ODR is user-defined per Table 19. To ensure that only tap events are detected, this time limit is used. This register sets the total amount of time that the two taps in a double tap event can be above the PI threshold (TTL). The Kionix recommended default value for STD is 0.09 seconds (0x24). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| STD7          | STD6 | STD5 | STD4 | STD3 | STD2 | STD1 | STD0 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00100100    |
| Address: 0x29 |      |      |      |      |      |      |      |             |



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*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

## TLT

This register contains counter information for the detection of a tap event. When the Directional-Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional-Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional-Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional-Tap™ ODR is user-defined per Table 19. To ensure that only tap events are detected, this time limit is used. This register sets the total amount of time that the tap algorithm will count samples that are above the PI threshold (TTL) during a potential tap event. It is used during both single and double tap events. However, reporting of single taps on the physical interrupt pin INT1 or INT2 will occur at the end of the TWS. The Kionix recommended default value for TLT is 0.1 seconds (0x28). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| TLT7          | TLT6 | TLT5 | TLT4 | TLT3 | TLT2 | TLT1 | TLT0 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00101000    |
| Address: 0x2A |      |      |      |      |      |      |      |             |

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

## TWS

This register contains counter information for the detection of single and double taps. When the Directional-Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional-Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional-Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional-Tap™ ODR is user-defined per Table 19. It defines the time window for the entire tap event, single or double, to occur. Reporting of single taps on the physical interrupt pin INT1 or INT2 will occur at the end of this tap window. The Kionix recommended default value for TWS is 0.4 seconds (0xA0). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| TWS7          | TWS6 | TWS5 | TWS4 | TWS3 | TWS2 | TWS1 | TWS0 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 10100000    |
| Address: 0x2B |      |      |      |      |      |      |      |             |



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*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

### FFTH

The Free Fall Threshold (FFTH) register contains the threshold of the Free fall detection. This value is compared to the top 8 bits of the accelerometer 8g output value (independent of the actual g-range setting of the device). See *AN049 Getting Started* for recommended settings ([LINK](#)). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".

| R/W           | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |             |
|---------------|-------|-------|-------|-------|-------|-------|-------|-------------|
| FFTH7         | FFTH6 | FFTH5 | FFTH4 | FFTH3 | FFTH2 | FFTH1 | FFTH0 | Reset Value |
| Bit7          | Bit6  | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  | 00000000    |
| Address: 0x2C |       |       |       |       |       |       |       |             |

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

### FFC

The Free Fall Counter (FFC) register contains the counter setting of the Free fall detection. Every count is calculated as 1/ODR delay period where ODR is a Free fall ODR set by OFFI<2:0> bits in FFCNTL register. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| FFC7          | FFC6 | FFC5 | FFC4 | FFC3 | FFC2 | FFC1 | FFC0 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000    |
| Address: 0x2D |      |      |      |      |      |      |      |             |

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

### FFCNTL

The Free Fall Control (FFCNTL) register contains the control setting of the Free fall detection. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".

| R/W           | R/W    | R/W  | R/W  | R/W  | R/W   | R/W   | R/W   |             |
|---------------|--------|------|------|------|-------|-------|-------|-------------|
| FFIE          | ULMODE | 0    | 0    | DCRM | OFFI2 | OFFI1 | OFFI0 | Reset Value |
| Bit7          | Bit6   | Bit5 | Bit4 | Bit3 | Bit2  | Bit1  | Bit0  | 00000000    |
| Address: 0x2E |        |      |      |      |       |       |       |             |





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**FFIE** – Free fall engine enable

FFIE = 0 – Free fall engine disabled

FFIE = 1 – Free fall engine enabled

**ULMODE** – Free fall interrupt latch/un-latch control

ULMODE = 0 – latched

ULMODE = 1 – unlatched

**DCRM** – Debounce methodology control

DCRM = 0 – count up/down

DCRM = 1 – count up/reset

**OFFI<2:0>** – Output Data Rate at which the Free fall engine performs its function.

The default Free fall ODR is 12.5Hz.

| OFFI | Output Data Rate (Hz) |
|------|-----------------------|
| 000  | 12.5                  |
| 001  | 25                    |
| 010  | 50                    |
| 011  | 100                   |
| 100  | 200                   |
| 101  | 400                   |
| 110  | 800                   |
| 111  | 1600                  |


**Table 22:** Free Fall Detection Output Data Rate

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

## ATH

The Activity Threshold (ATH) register sets the threshold for wake-up (motion detect) interrupt is set. This value is compared to the top 8 bits of the accelerometer 8g output value (independent of the actual g-range setting of the device). The KX112 will ship from the factory with this value set to correspond to a change in acceleration of 0.5g. See *AN049 Getting Started* for recommended settings ([LINK](#)). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| ATH7          | ATH6 | ATH5 | ATH4 | ATH3 | ATH2 | ATH1 | ATH0 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00001000    |
| Address: 0x30 |      |      |      |      |      |      |      |             |

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*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

#### TILT\_ANGLE\_LL

Tilt Angle Low Limit: This register sets the low-level threshold for tilt angle detection. The low-level threshold value is compared against the upper 8 bits of the 4g output value (independent of the actual g-range setting of the device). The default tilt angle low level threshold is set to 22° from the horizontal. Note that the minimum suggested tilt angle is 10°. See *AN049 Getting Started* for recommended settings ([LINK](#)). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| TA7           | TA6  | TA5  | TA4  | TA3  | TA2  | TA1  | TA0  | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00001100    |
| Address: 0x32 |      |      |      |      |      |      |      |             |

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

#### TILT\_ANGLE\_HL

Tilt Angle High Limit: This register sets the high-level threshold for tilt angle detection. The high-level threshold is used by an internal algorithm to eliminate dynamic g-variations caused by the device movement. Instead, only static g-variation (gravity) caused by the actual tilt changes are used. The high-level threshold value is compared against the upper 8 bits of the 4g output value (independent of the actual g-range setting of the device). The default tilt angle high level threshold is set to just above 1g plus some margin of error to account for external factors (e.g. device mounting). See *AN049 Getting Started* for recommended settings ([LINK](#)). Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

| R/W           | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |             |
|---------------|------|------|------|------|------|------|------|-------------|
| HL7           | HL6  | HL5  | HL4  | HL3  | HL2  | HL1  | HL0  | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00101010    |
| Address: 0x33 |      |      |      |      |      |      |      |             |

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

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## HYST\_SET

This register sets the Hysteresis that is placed in between the Screen Rotation states. The KX112 ships from the factory with HYST\_SET set to  $\pm 15^\circ$  of hysteresis. Note that when writing a new value to this register the current values of RES0 and RES1 must be preserved. These values are set at the factory and must not change. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".

| R/W           | R/W      | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |             |
|---------------|----------|-------|-------|-------|-------|-------|-------|-------------|
| Reserved      | Reserved | HYST5 | HYST4 | HYST3 | HYST2 | HYST1 | HYST0 | Reset Value |
| Bit7          | Bit6     | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  | 00010100    |
| Address: 0x34 |          |       |       |       |       |       |       |             |

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*


## LP\_CNTL

The Averaging Filter Control setting can be used in the optimization of current and noise performance of the accelerometer and can be tested using [Kionix FlexSet™ Performance Optimization Tool](#). More specifically, this setting determines the number of internal acceleration samples to be averaged in Low Power mode. Also, it determines the number of internal acceleration samples to be averaged for digital engines operation (Directional-Tap™, Tilt, Wake-Up, Free fall) both in *High Resolution* and *Low Power* modes. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".

| R/W           | R/W  | R/W  | R/W  | R/W      | R/W      | R/W      | R/W      |             |
|---------------|------|------|------|----------|----------|----------|----------|-------------|
| Reserved      | AVC2 | AVC1 | AVC0 | Reserved | Reserved | Reserved | Reserved | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3     | Bit2     | Bit1     | Bit0     | 01001011    |
| Address: 0x35 |      |      |      |          |          |          |          |             |

**AVC<2:0>** – Averaging Filter Control. The default setting is 16 samples and was found to work for most case.

000 = No Averaging  
 001 = 2 Samples Averaged  
 010 = 4 Samples Averaged  
 011 = 8 Samples Averaged  
 100 = 16 Samples Averaged (default)  
 101 = 32 Samples Averaged  
 110 = 64 Samples Averaged  
 111 = 128 Samples Averaged

|   |   |  |
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*Note: New data is blocked from being written to the sample buffer when this register is read from using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

#### BUF\_CNTL1

The Buffer Control 1 (BUF\_CNTL1) register controls the buffer sample threshold. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to "0".


| R/W           | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     |             |
|---------------|---------|---------|---------|---------|---------|---------|---------|-------------|
| SMP_TH7       | SMP_TH6 | SMP_TH5 | SMP_TH4 | SMP_TH3 | SMP_TH2 | SMP_TH1 | SMP_TH0 | Reset Value |
| Bit7          | Bit6    | Bit5    | Bit4    | Bit3    | Bit2    | Bit1    | Bit0    | 00000000    |
| Address: 0x3A |         |         |         |         |         |         |         |             |

**SMP\_TH [9:0] Sample Threshold** determines the number of samples that will trigger a watermark interrupt or will be saved prior to a trigger event. When BUF\_RES=1, the maximum number of samples is 340; when BUF\_RES=0, the maximum number of samples is 681.

| Buffer Model | Sample Function  |
|--------------|--|
| Bypass       | None   |
| FIFO         | Specifies how many buffer samples are needed to trigger a watermark interrupt.         |
| Stream       | Specifies how many buffer samples are needed to trigger a watermark interrupt.         |
| Trigger      | Specifies how many buffer samples before the trigger event are retained in the buffer. |
| FILO         | Specifies how many buffer samples are needed to trigger a watermark interrupt.         |

**Table 23:** Sample Threshold Operation by Buffer Mode

*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

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## BUF\_CNTL2

The Buffer Control 2 (BUF\_CNTL2) register controls sample buffer operation. Note that to properly change the value of this register, the PC1 bit in CNTL1 register must first be set to “0”.

|               |      |      |      |         |         |        |        |             |
|---------------|------|------|------|---------|---------|--------|--------|-------------|
| R/W           | R/W  | R/W  | R/W  | R/W     | R/W     | R/W    | R/W    |             |
| BUFE          | BRES | BFIE | 0    | SMP_TH9 | SMP_TH8 | BUF_M1 | BUF_M0 | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3    | Bit2    | Bit1   | Bit0   | 00000000    |
| Address: 0x3B |      |      |      |         |         |        |        |             |

**BUFE** controls activation of the sample buffer.

*BUFE = 0 – sample buffer inactive*

*BUFE = 1 – sample buffer active*

*Note: Disabling the sample buffer (BUFE = 0) will clear the buffer. The buffer will also be cleared (1) following write to BUF\_CLEAR register and/or (2) after setting PC1 bit in CNTL1 register to 0 (standby mode).*

**BRES** determines the resolution of the acceleration data samples collected by the sample buffer.

*BRES = 0 – 8-bit samples are accumulated in the buffer*

*BRES = 1 – 16-bit samples are accumulated in the buffer*

**BFIE** buffer full interrupt enable bit

*BFIE = 0 – buffer full interrupt disabled*

*BFIE = 1 – buffer full interrupt updated in INS2*

**BUF\_M1, BUF\_M0** selects the operating mode of the sample buffer per Table 24.

| BUF_M1 | BUF_M0 | Mode    | Description   |
|--------|--------|---------|---|
| 0      | 0      | FIFO    | The buffer collects 681 sets of 8-bit low resolution values or 340 sets of 16-bit high resolution values and then stops collecting data, collecting new data only when the buffer is not full.  |
| 0      | 1      | Stream  | The buffer holds the last 681 sets of 8-bit low resolution values or 340 sets of 16-bit high resolution values. Once the buffer is full, the oldest data is discarded to make room for newer data.  |
| 1      | 0      | Trigger | When a trigger event occurs, the buffer holds the last data set of SMP_TH[9:0] samples before the trigger event and then continues to collect data until full. New data is collected only when the buffer is not full.  |
| 1      | 1      | FILO    | The buffer holds the last 681 sets of 8-bit low resolution values or 340 sets of 16-bit high resolution values. Once the buffer is full, the oldest data is discarded to make room for newer data. Reading from the buffer in this mode will return the most recent data first. |

**Table 24:** Selected Buffer Mode



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*Note: New data is blocked from being written to the sample buffer when this register is read from / written to using SPI interface only. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready).*

## BUF\_STATUS\_1

Buffer Status 1: This register reports the status of the sample buffer.

|               |          |          |          |          |          |          |          |
|---------------|----------|----------|----------|----------|----------|----------|----------|
| R             | R        | R        | R        | R        | R        | R        | R        |
| SMP_LEV7      | SMP_LEV6 | SMP_LEV5 | SMP_LEV4 | SMP_LEV3 | SMP_LEV2 | SMP_LEV1 | SMP_LEV0 |
| Bit7          | Bit6     | Bit5     | Bit4     | Bit3     | Bit2     | Bit1     | Bit0     |
| Address: 0x3C |          |          |          |          |          |          |          |

**SMP\_LEV [10:0] Sample Level:** reports the number of data bytes that have been stored in the sample buffer. When BRES=1, this count will increase by 6 for each 3-axis sample in the buffer. When BRES=0, the count will increase by 3 for each 3-axis sample. If this register reads 0, no data has been stored in the buffer.

*Note: New data is blocked from being written to the sample buffer when this register is read using I<sup>2</sup>C/SPI interface. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready) or perform a burst read from 0x3B to 0x3C.*

## BUF\_STATUS\_2

Buffer Status 2: This register reports the status of the sample buffer trigger function.

|               |      |      |      |      |           |          |          |
|---------------|------|------|------|------|-----------|----------|----------|
| R             | R    | R    | R    | R    | R         | R        | R        |
| BUF_TRIG      | 0    | 0    | 0    | 0    | SMP_LEV10 | SMP_LEV9 | SMP_LEV8 |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2      | Bit1     | Bit0     |
| Address: 0x3D |      |      |      |      |           |          |          |

**BUF\_TRIG** reports the status of the buffer's trigger function if this mode has been selected. When using trigger mode, a buffer read should only be performed after a trigger event. This bit is cleared after writing to BUF\_CLEAR register. This will prevent Buffer Full interrupt from firing while TRIG pin remains de-asserted.

*Note: New data is blocked from being written to the sample buffer when this register is read from using I<sup>2</sup>C/SPI interface. To prevent this, complete the serial communication transacting before the next ODR update (synchronous with Data Ready) or perform a burst read from 0x3B to 0x3D.*



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### BUF\_CLEAR

Buffer Clear: When any data is written to this register, the entire sample buffer is cleared. This causes the sample level bits SMP\_LEV [10:0] to be cleared in BUF\_STATUS\_1 and BUF\_STATUS\_2 registers. In addition, if the sample buffer is set to Trigger mode, the BUF\_TRIG bit in BUF\_STATUS\_2 is cleared too. Finally, the BFI and WMI bits in INS2 will be cleared and physical interrupt latched pin will be changed to its inactive state.

|               |      |      |      |      |      |      |      |
|---------------|------|------|------|------|------|------|------|
| W             | W    | W    | W    | W    | W    | W    | W    |
| X             | X    | X    | X    | X    | X    | X    | X    |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| Address: 0x3E |      |      |      |      |      |      |      |

### BUF\_READ

Buffer Read: Buffer output register

|               |      |      |      |      |      |      |      |
|---------------|------|------|------|------|------|------|------|
| R             | R    | R    | R    | R    | R    | R    | R    |
| X             | X    | X    | X    | X    | X    | X    | X    |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| Address: 0x3F |      |      |      |      |      |      |      |

*Note: New data is not being written to the buffer during the buffer read operation. Thus, care must be taken when reading from the buffer. If data loss is not desired, the buffer read operation should be completed within ODR clock cycle.*


### SELF\_TEST

Self-Test: When 0xCA value is written to this register, the MEMS self-test function is enabled. Electrostatic-actuation of the accelerometer, results in a DC shift of the X, Y and Z axis outputs. Writing 0x00 to this register will return the accelerometer to normal operation.

**\*\*Note**, this is a write-only register. Read back value from this register will always be 0x00.

|               |      |      |      |      |      |      |      |             |
|---------------|------|------|------|------|------|------|------|-------------|
| W             | W    | W    | W    | W    | W    | W    | W    |             |
| 0             | 0    | 0    | 0    | 0    | 0    | 0    | 0    | Reset Value |
| Bit7          | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000    |
| Address: 0x60 |      |      |      |      |      |      |      |             |



|   |   |   |
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## Embedded Applications

### Orientation Detection Feature

The orientation detection feature of the KX112 will report changes in face up, face down,  $\pm$  vertical and  $\pm$  horizontal orientation. This intelligent embedded algorithm considers very important factors that provide accurate orientation detection from low cost tri-axis accelerometers. Factors such as: hysteresis, device orientation angle, and delay time are described below as these techniques are utilized inside the KX112.

#### Hysteresis

A 45° tilt angle threshold seems like a good choice because it is halfway between 0° and 90°. However, a problem arises when the user holds the device near 45°. Slight vibrations, noise and inherent sensor error will cause the acceleration to go above and below the threshold rapidly and randomly, so the screen will quickly flip back and forth between the 0° and the 90° orientations. This problem is avoided in the KX112 by choosing a 30° threshold angle. With a 30° threshold, the screen will not rotate from 0° to 90° until the device is tilted to 60° (30° from 90°). To rotate back to 0°, the user must tilt back to 30°, thus avoiding the screen flipping problem. This example essentially applies  $\pm 15^\circ$  of hysteresis in between the four screen rotation states. Table 25 shows the acceleration limits implemented for  $\phi_T = 30^\circ$ .

| Orientation | X Acceleration (g) | Y Acceleration (g) |
|-------------|--------------------|--------------------|
| 0°/360°     | $-0.5 < a_x < 0.5$ | $a_y > 0.866$      |
| 90°         | $a_x > 0.866$      | $-0.5 < a_y < 0.5$ |
| 180°        | $-0.5 < a_x < 0.5$ | $a_y < -0.866$     |
| 270°        | $a_x < -0.866$     | $-0.5 < a_y < 0.5$ |

**Table 25:** Acceleration at the four orientations with  $\pm 15^\circ$  of hysteresis

The KX112 allows the user to change the amount of hysteresis in between the four screen rotation states. By simply writing to the HYST\_SET register, the user can adjust the amount of hysteresis up to  $\pm 45^\circ$ . The plot in Figure 11 shows the typical amount of hysteresis applied for a given digital count value of HYST\_SET.





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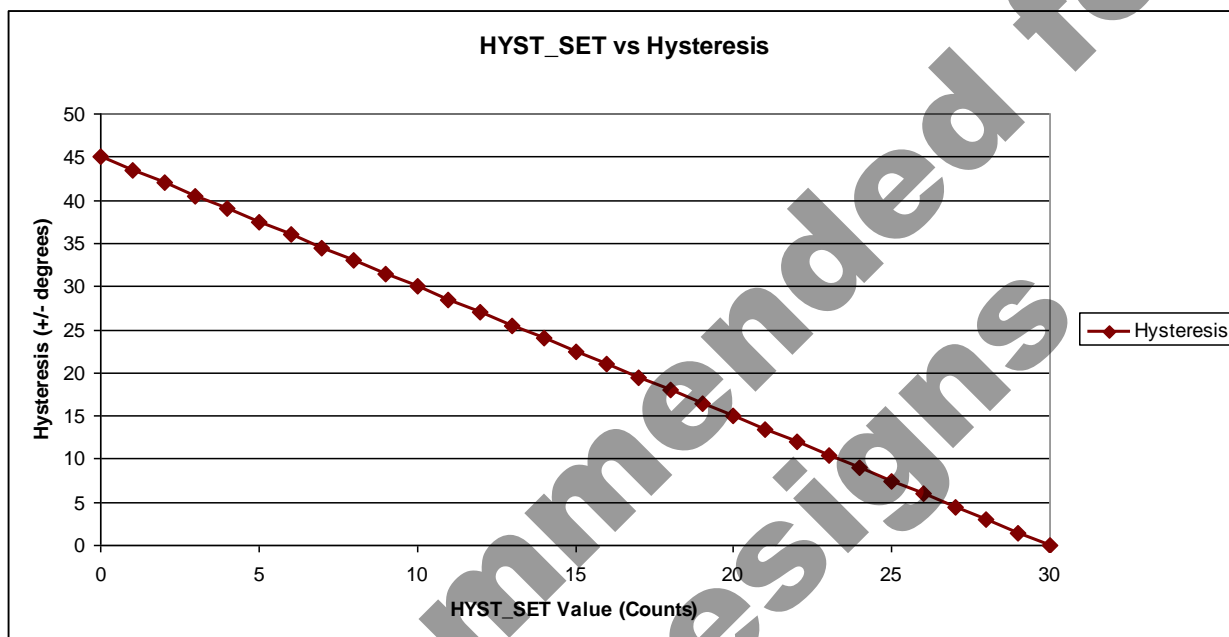


Figure 11: HYST\_SET vs Hysteresis

### Device Orientation Angle (aka Tilt Angle)

To ensure that horizontal and vertical device orientation changes are detected, even when it isn't in the ideal vertical orientation – where the angle  $\theta$  in Figure 12 is  $90^\circ$ , the KX112 considers device orientation angle in its algorithm.

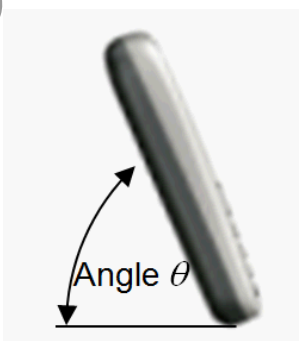


Figure 12: Device Orientation Angle

As the angle in Figure 12 is decreased, the maximum gravitational acceleration on the X-axis or Y-axis will also decrease. Therefore, when the angle becomes small enough, the user will not be able to make



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the screen orientation change. When the device orientation angle approaches 0° (device is flat on a desk or table),  $a_x = a_y = 0g$ ,  $a_z = +1g$ , and there is no way to determine which way the screen should be oriented, the internal algorithm determines that the device is in either the face-up or face-down orientation, depending on the sign of the z-axis. The KX112 will only change the screen orientation when the orientation angle is above the factory-defaulted/user-defined threshold set in the TILT\_ANGLE\_LL register. Equation 2 can be used to determine what value to write to the TILT\_ANGLE\_LL register to set the device orientation angle. The value for TILT\_ANGLE\_HL is preset at the factory but can be adjusted in special cases (e.g. to reduce the effect of transient g-variation such as when device is being moved rather than just being rotated).

$$\text{TILT\_ANGLE\_LL (counts)} = \sin \theta * (32 \text{ (counts/g)})$$


**Equation 2:** Tilt Angle Threshold

### Tilt Timer

The 8-bit register, TILT\_TIMER can be used to qualify changes in orientation. The KX112 does this by incrementing a counter with a size that is specified by the value in TILT\_TIMER for each set of acceleration samples to verify that a change to a new orientation state is maintained. A user defined Tilt Position output data rate (ODR) as set by OTP<1:0> bits in CNTL3 register, determines the time period for each sample. Equation 3 shows how to calculate the TILT\_TIMER register value for a desired delay time.

$$\text{TILT\_TIMER (counts)} = \text{Delay Time (sec)} \times \text{Tilt Position ODR (Hz)}$$

**Equation 3:** Tilt Position Delay Time

|   |   |   |
|---|---|---|
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## Motion Interrupt Feature Description

The Motion interrupt feature of the KX112 reports qualified changes in the high-pass filtered acceleration based on the wake-up Activity Threshold (ATH). If the high-pass filtered acceleration on any axis is greater than the user-defined wake-up activity threshold (ATH), the device has transitioned from an inactive state to an active state. Equation 4 shows how to calculate the ATH register value for a desired wake-up threshold. The wake-up engine function is independent of the user selected g-range and resolution.

$$\text{ATH (counts)} = \text{Wake-Up Threshold (g)} \times 16 \text{ (counts/g)}$$

### Equation 4: Wake-Up Threshold

An 8-bit raw unsigned value represents a counter that permits the user to qualify each active/inactive state change. Note that each Wake-Up Function Counter (WUFC) count value qualifies 1 (one) user-defined Wake-up Function ODR period as set by OWUF<2:0> bits in CNTL3 register. Equation 5 shows how to calculate the WUFC register value for a desired wake-up delay time.

$$\text{WUFC (counts)} = \text{Wake-Up Delay Time (sec)} \times \text{Wake-up Function ODR (Hz)}$$

### Equation 5: Wake-Up Delay Time

The latched motion interrupt response algorithm works as following: while the part is in inactive state, the algorithm evaluates differential measurement between each new acceleration data point with the preceding one and evaluates it against the Activity Threshold (ATH). When the differential measurement is greater than ATH, the wake-up function counter (WUFC) starts the count. Differential measurements are now calculated based on the difference between the current acceleration and the acceleration when the counter started. The part will report that motion has occurred at the end of the count assuming each differential measurement has remained above the threshold. If at any moment during the count the differential measurement falls below the threshold, the counter will stop the count and the part will remain in inactive state.

To illustrate how the algorithm works, consider the Figure 13 below that shows the latched response of the motion detection algorithm with the Wake-up Function Counter (WUFC) set to 10 counts. Note how the difference between the acceleration sample marked in red and the one marked in green resulted in a differential measurement represented with orange bar being above the Activity Threshold (ATH). At this point, the Wake-up Function Counter (WUFC) begins to count number of counts stored in WUFC register and the wake-up algorithm will evaluate the difference between each new acceleration measurement and the measurement marked in green that will remain a reference measurement for the duration of the counter count. At the end of the count, assuming all differential measurements were larger than Activity Threshold (ATH), as is the case in the example showed in Figure 13 a motion event will be reported.



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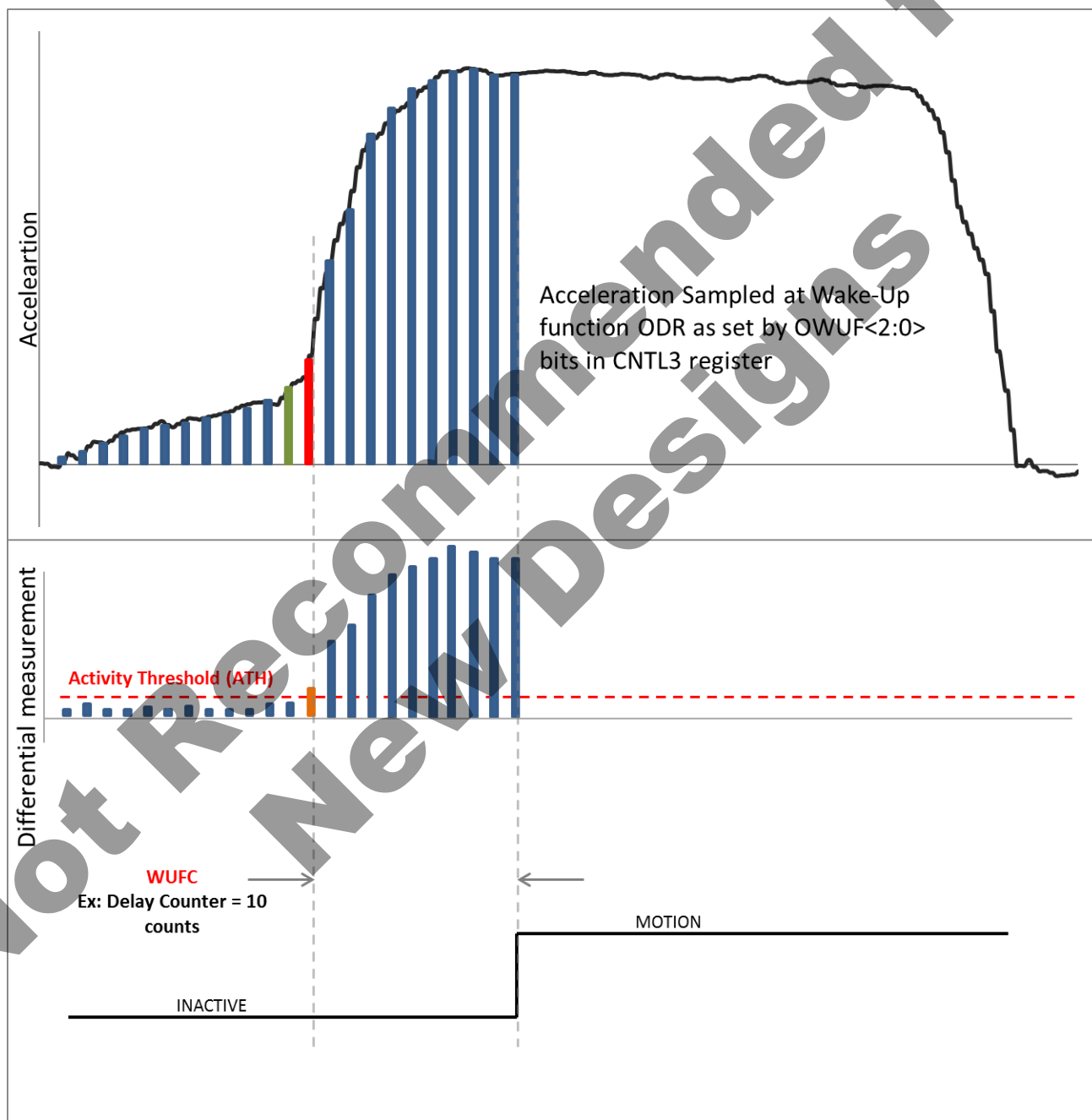


Figure 13: Latched Motion Interrupt Response



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### Directional-Tap Detection Feature Description

The Directional-Tap™ Detection feature of the KX112 recognizes single and double tap inputs and reports the acceleration axis and direction that each tap occurred. Eight performance parameters, as well as a user-selectable ODR are used to configure the KX112 for a desired tap detection response.

### Performance Index

The Directional-Tap™ detection algorithm uses low and high thresholds to help determine when a tap event has occurred. A tap event is detected when the previously described jerk summation exceeds the low *threshold (TTL)* for more than the tap detection low limit, but less than the tap detection high limit as contained in FTD. Samples that exceed the high limit (TTH) will be ignored. Figure 14 shows an example of a single tap event meeting the performance index criteria.

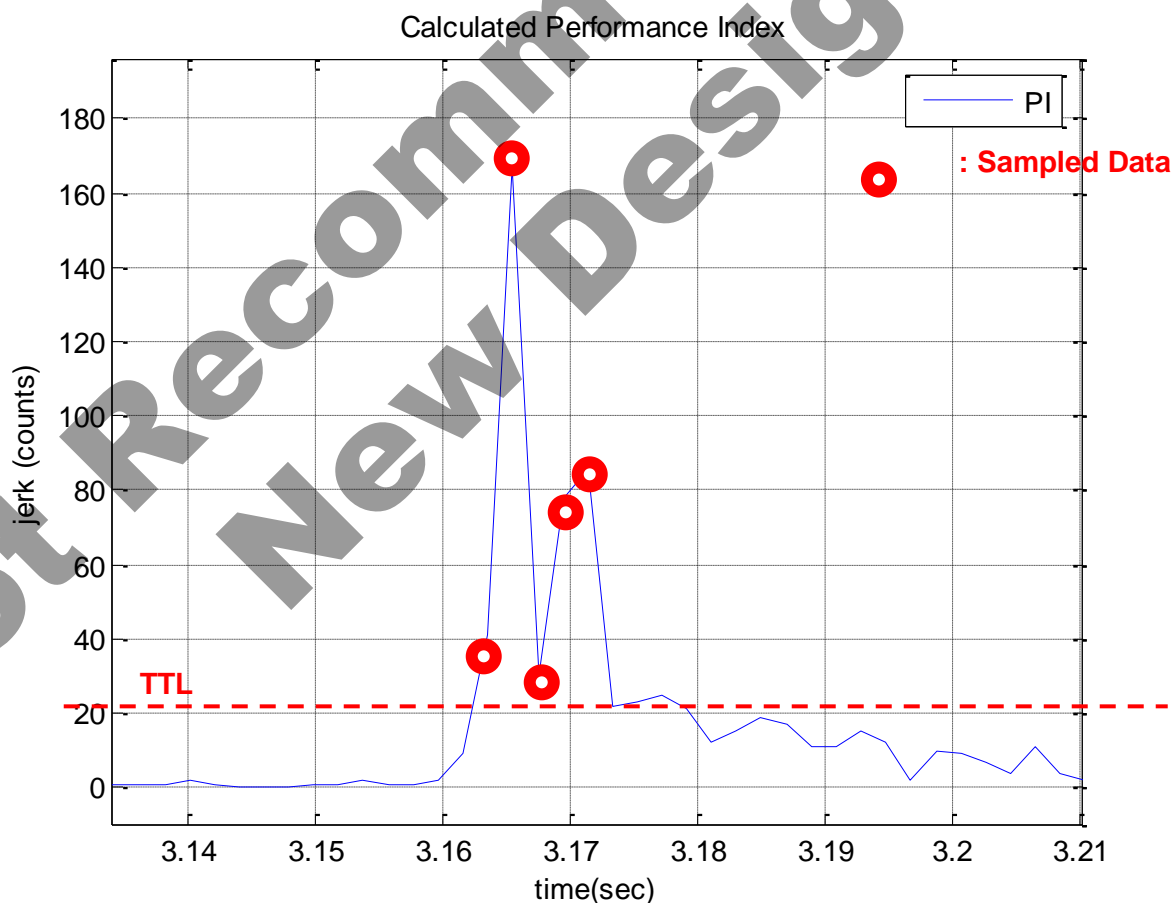


Figure 14: Jerk Summation vs Threshold



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## Single Tap Detection

The latency timer (TLT) sets the time period that a tap event will only be characterized as a single tap. A second tap must occur outside of the latency timer. If a second tap occurs inside the latency time, it will be ignored as it occurred too quickly. The single tap will be reported at the end of the TWS. Figure 15 shows a single tap event meeting the PI, latency and window requirements.

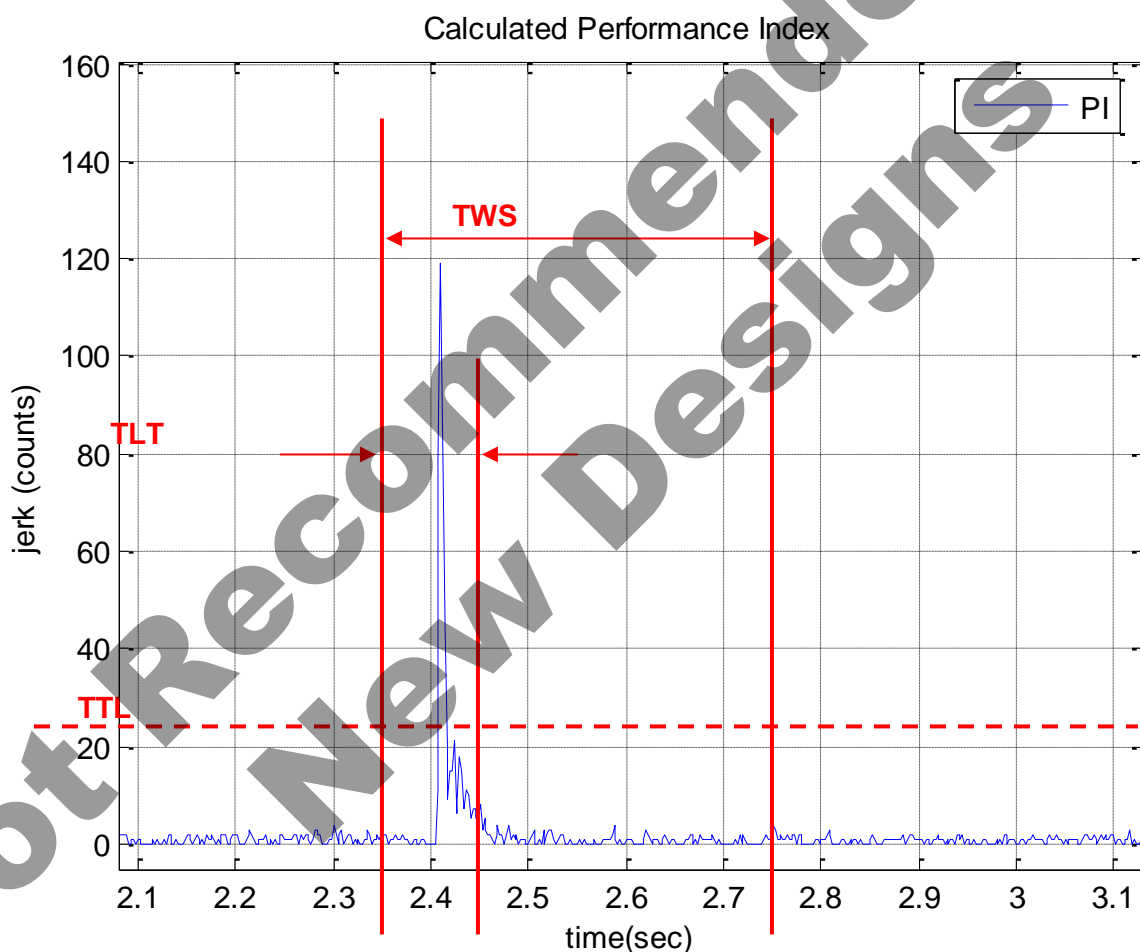


Figure 15: Single Directional-Tap™ Timing



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### Double-Tap Detection

An event can be characterized as a double tap if the second tap crosses the performance index (TTL) inside the TWS period and ends outside the TDTC. This means that the TDTC determines the minimum time separation that must exist between the two taps of a double tap event. Similar to the single tap, the first tap event must exceed the performance index for the time limit contained in FTD. Also, the duration when the first and second events combined exceed the performance index should not exceed STD. The double tap will be reported at the end of the second TLT. Figure 16 shows a double tap event meeting the PI, latency and window requirements.

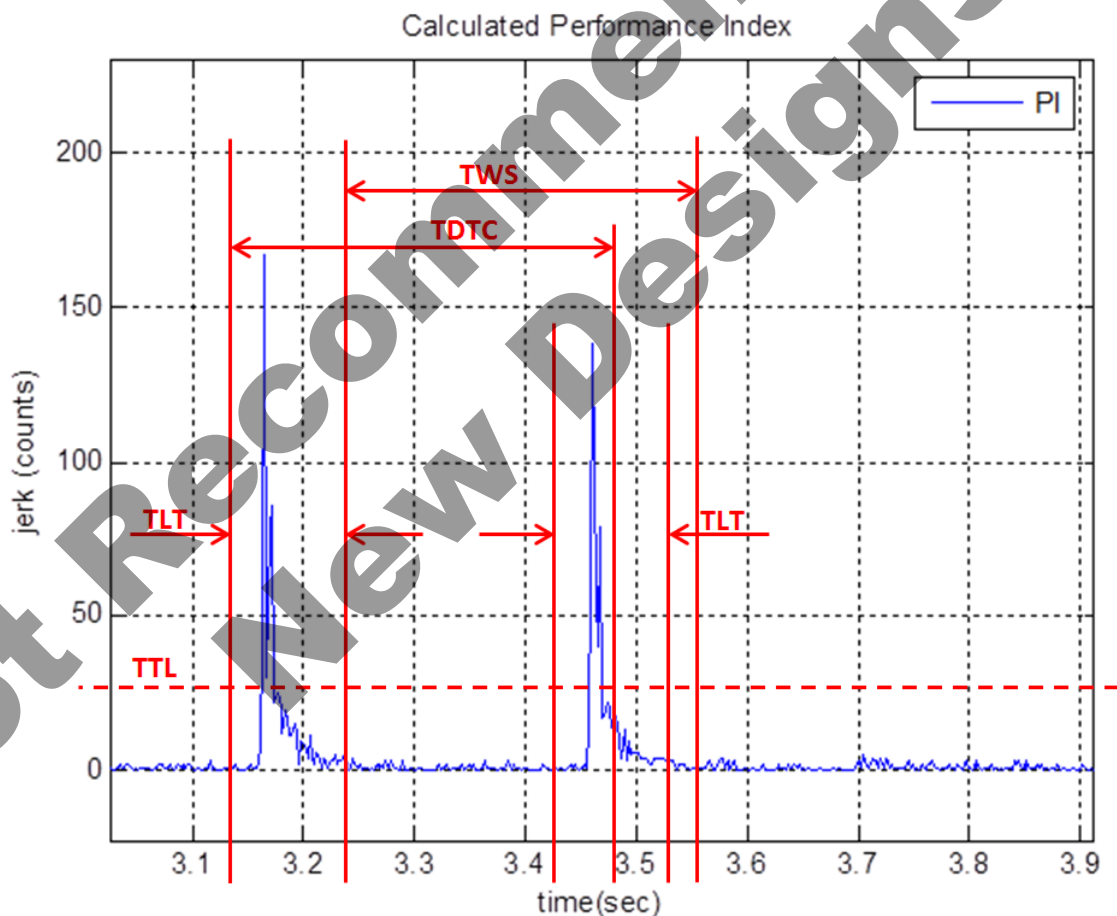



Figure 16: Double-Tap™ Timing

|   |   |   |
|---|---|---|
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## Free fall Detect

The KX112 features a Free fall interrupt that sends a flag through the INT1 or the INT2 output pins when the accelerometer senses a Free fall event. The interrupt event is also reflected on the INT (bit 4) of the STATUS\_REG and FFS (bit 7) of the INS2 registers. A Free fall event is evident when all three accelerometer axes simultaneously fall below a certain acceleration threshold for a set amount of time. The KX112 gives the user the option to define the acceleration threshold value through the FFTH 8-bit register where 256 counts cover the g range of the accelerometer. This value is compared to the top 8 bits of the accelerometer 8g output value (independent of the actual g-range setting of the device). Equation 6 shows how to calculate the FFTH register value for a desired Free fall threshold. The threshold of 0.5g is a good starting point.

$$\text{FFTH (counts)} = \text{Free fall Threshold (g)} \times 16 \text{ (counts/g)}$$

### Equation 6: Free fall Threshold

Through the Free Fall Counter (FFC), the user can set the amount of time all three accelerometer axes must simultaneously remain below the FFTH acceleration threshold before the Free fall interrupt flag is sent through the INT1 or the INT2 output pins. This delay/debounce time is defined by the available 0 to 255 counts, which represent accelerometer samples taken at the Free fall ODR defined by OFFI<2:0> bits in the FFCNTL register. Every count is calculated as 1/ODR delay period. Equation 7 shows how to calculate the FFC register value for a desired Free fall delay. The delay of 0.32 sec is a good starting point.

$$\text{FFC (counts)} = \text{Free fall delay (sec)} \times \text{Free fall ODR (Hz)}$$

### Equation 7: Free fall Threshold

When the Free fall interrupt is enabled the part must not be in a physical state that would trigger the Free fall interrupt or the delay will not be correct for the present Free fall.





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### Typical Freefall Interrupt Example (nonLatching)

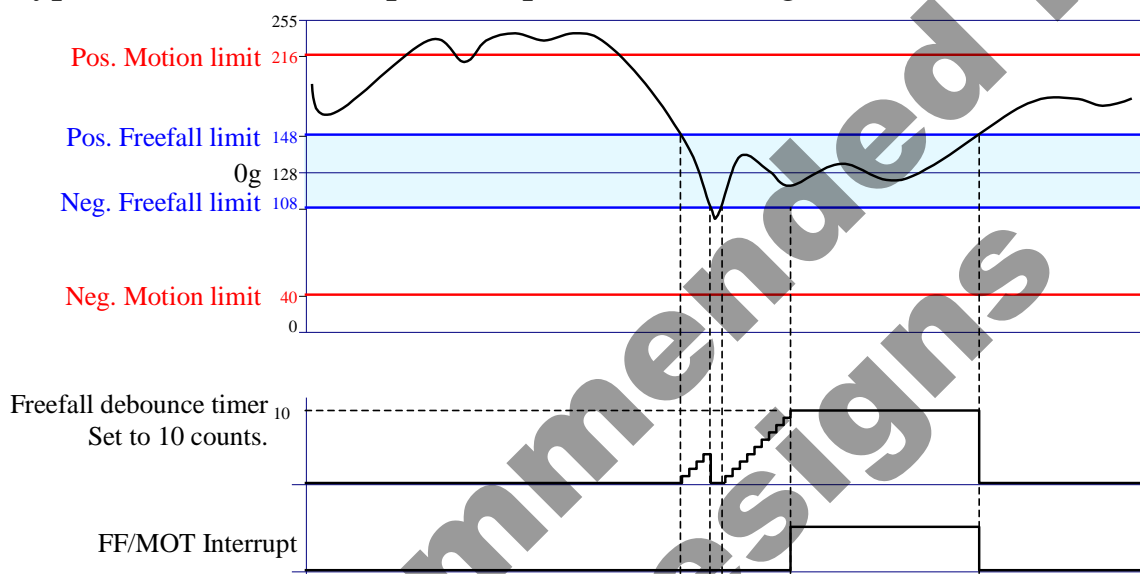


Figure 17: Typical Free Fall Interrupt Example (FFCNTL ULMODE = 1)

### Typical Freefall Interrupt Example (Latching)

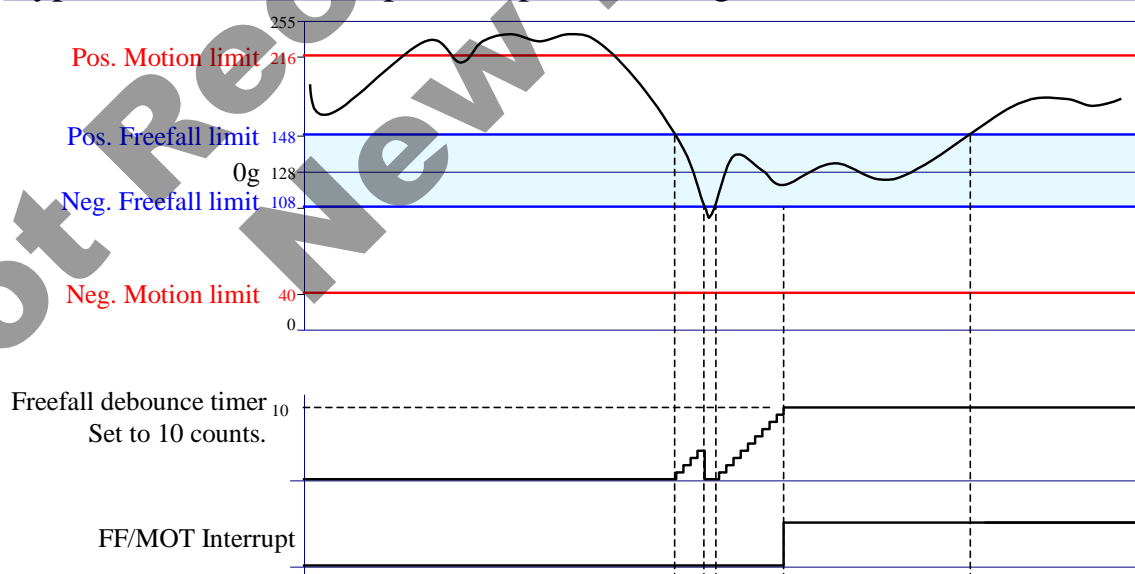



Figure 18: Typical Free Fall Interrupt Example (FFCNTL ULMODE = 0)

|   |   |   |
|---|---|---|
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## Sample Buffer Feature Description

The sample buffer feature of the KX112 accumulates and outputs acceleration data based on how it is configured. There are 4 buffer modes available, and samples can be accumulated at either low (8-bit) or high (16-bit) resolution. Acceleration data is collected at the ODR specified by OSA[3:0] in the ODCNTL register. Each buffer mode accumulates data, reports data, and interacts with status indicators in a slightly different way.

### FIFO Mode

#### Data Accumulation

Sample collection stops when the buffer is full.

#### Data Reporting

Data is reported with the oldest byte of the oldest sample first (X\_L or X based on resolution).

#### Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 8).

BUF\_RES=0:

$$\text{SMPX} = \text{SMP\_LEV}[10:0] / 3 - \text{SMP\_TH}[9:0]$$

BUF\_RES=1:

$$\text{SMPX} = \text{SMP\_LEV}[10:0] / 6 - \text{SMP\_TH}[9:0]$$

**Equation 8:** Samples Above Sample Threshold

### Stream Mode

#### Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

#### Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

#### Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 8).

|   |   |  |
|---|---|--|
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## Trigger Mode

### Data Accumulation

When a physical interrupt is caused by one of the digital engines or when a logic high signal occurs on the TRIG pin, the trigger event is asserted and SMP\_TH[9:0] samples prior to the event are retained. Sample collection continues until the buffer is full.

### Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

### Status Indicators

When a physical interrupt occurs and there are at least SMP\_TH[9:0] samples in the buffer, BUF\_TRIG in BUF\_STATUS\_2 is asserted.

## FILO Mode

### Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

### Data Reporting

Data is reported with the newest byte of the newest sample first (Z\_H or Z based on resolution).

### Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 8).

## Buffer Operation

The following diagrams illustrate the operation of the buffer conceptually. Actual physical implementation has been abstracted to offer a simplified explanation of how the different buffer modes operate. Figure 19 represents a high-resolution 3-axis sample within the buffer. Figure 20 – Figure 28 represent a 10-sample version of the buffer (for simplicity), with Sample Threshold set to 8.

Regardless of the selected mode, the buffer fills sequentially, one byte at a time. Figure 19 shows one 6-byte data sample. Note the location of the FILO read pointer versus that of the FIFO read pointer.



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| Index | Byte |                       |
|-------|------|-----------------------|
| 0     | X_L  | ←-- FIFO read pointer |
| 1     | X_H  |                       |
| 2     | Y_L  |                       |
| 3     | Y_H  |                       |
| 4     | Z_L  |                       |
| 5     | Z_H  | ←-- FILO read pointer |
| 6     |      |                       |

buffer write pointer --→

**Figure 19: One Buffer Sample**

Regardless of the selected mode, the buffer fills sequentially, one sample at a time. Note in Figure 20 the location of the FILO read pointer versus that of the FIFO read pointer. The buffer write pointer shows where the next sample will be written to the buffer.

| Index | Sample |                     |
|-------|--------|---------------------|
| 0     | Data0  | ← FIFO read pointer |
| 1     | Data1  |                     |
| 2     | Data2  | ← FILO read pointer |
| 3     |        |                     |
| 4     |        |                     |
| 5     |        |                     |
| 6     |        |                     |
| 7     |        | ← Sample Threshold  |
| 8     |        |                     |
| 9     |        |                     |

buffer write pointer →

**Figure 20: Buffer Filling**



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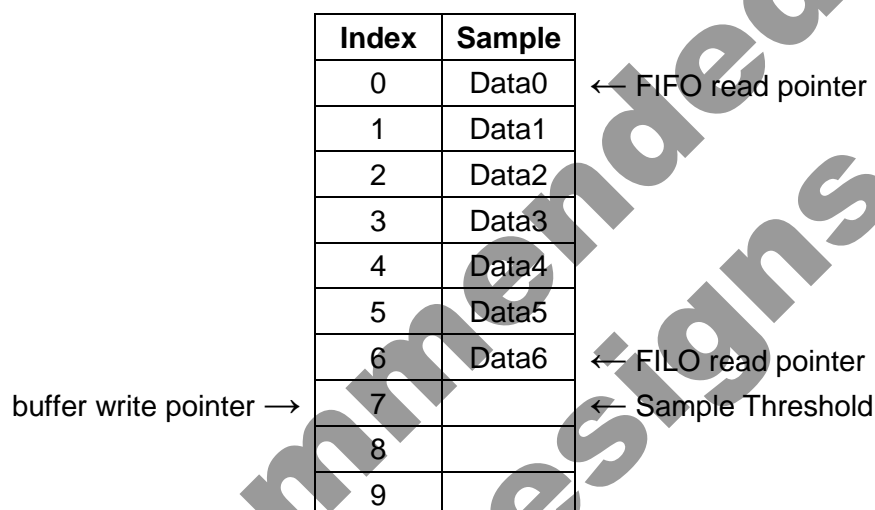
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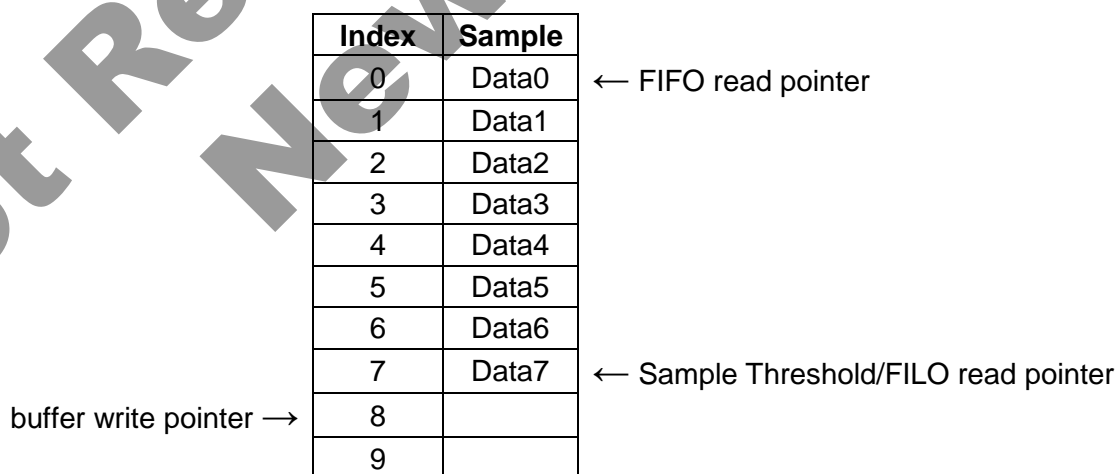
**15-Jan-2018**

The buffer continues to fill sequentially until the Sample Threshold is reached. Note in Figure 21 the location of the FILO read pointer versus that of the FIFO read pointer.



**Figure 21: Buffer Approaching Sample Threshold**

In FIFO, Stream, and FILO modes, a watermark interrupt is issued when the number of samples in the buffer reaches the Sample Threshold. In trigger mode, this is the point where the oldest data in the buffer is discarded to make room for newer data.



**Figure 22: Buffer at Sample Threshold**



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In trigger mode, data is accumulated in the buffer sequentially until the Sample Threshold is reached. Once the Sample Threshold is reached, the oldest samples are discarded when new samples are collected. Note in Figure 23 how Data0 was thrown out to make room for Data8.

| Index | Sample |                        |
|-------|--------|------------------------|
| 0     | Data1  | ← Trigger read pointer |
| 1     | Data2  |                        |
| 2     | Data3  |                        |
| 3     | Data4  |                        |
| 4     | Data5  |                        |
| 5     | Data6  |                        |
| 6     | Data7  |                        |
| 7     | Data8  | ← Sample Threshold     |
| 8     |        |                        |
| 9     |        |                        |

Trigger write pointer →

**Figure 23:** Additional Data Prior to Trigger Event

After a trigger event occurs, the buffer no longer discards the oldest samples, and instead begins accumulating samples sequentially until full. The buffer then stops collecting samples, as seen in Figure 24. This results in the buffer holding SMP\_TH[9:0] samples prior to the trigger event, and SMPX samples after the trigger event.

| Index | Sample |                        |
|-------|--------|------------------------|
| 0     | Data1  | ← Trigger read pointer |
| 1     | Data2  |                        |
| 2     | Data3  |                        |
| 3     | Data4  |                        |
| 4     | Data5  |                        |
| 5     | Data6  |                        |
| 6     | Data7  |                        |
| 7     | Data8  | ← Sample Threshold     |
| 8     | Data9  |                        |
| 9     | Data10 |                        |

**Figure 24:** Additional Data after Trigger Event



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In FIFO, Stream, FILO, and Trigger (after a trigger event has occurred) modes, the buffer continues filling sequentially after the Sample Threshold is reached. Sample accumulation after the buffer is full depends on the selected operation mode. FIFO and Trigger modes stop accumulating samples when the buffer is full, and Stream and FILO modes begin discarding the oldest data when new samples are accumulated.

| Index | Sample |                     |
|-------|--------|---------------------|
| 0     | Data0  | ← FIFO read pointer |
| 1     | Data1  |                     |
| 2     | Data2  |                     |
| 3     | Data3  |                     |
| 4     | Data4  |                     |
| 5     | Data5  |                     |
| 6     | Data6  |                     |
| 7     | Data7  | ← Sample Threshold  |
| 8     | Data8  |                     |
| 9     | Data9  | ← FILO read pointer |

Figure 25: Buffer Full

After the buffer has been filled in FILO or Stream mode, the oldest samples are discarded when new samples are collected. Note in Figure 26 how Data0 was thrown out to make room for Data10.

| Index | Sample |                     |
|-------|--------|---------------------|
| 0     | Data1  | ← FIFO read pointer |
| 1     | Data2  |                     |
| 2     | Data3  |                     |
| 3     | Data4  |                     |
| 4     | Data5  |                     |
| 5     | Data6  |                     |
| 6     | Data7  |                     |
| 7     | Data8  | ← Sample Threshold  |
| 8     | Data9  |                     |
| 9     | Data10 | ← FILO read pointer |

Figure 26: Buffer Full – Additional Sample Accumulation in Stream or FILO Mode



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In FIFO, Stream, or Trigger mode, reading one sample from the buffer will remove the oldest sample and effectively shift the entire buffer contents up, as seen in Figure 27.

| Index | Sample |                     |
|-------|--------|---------------------|
| 0     | Data1  | ← FIFO read pointer |
| 1     | Data2  |                     |
| 2     | Data3  |                     |
| 3     | Data4  |                     |
| 4     | Data5  |                     |
| 5     | Data6  |                     |
| 6     | Data7  |                     |
| 7     | Data8  | ← Sample Threshold  |
| 8     | Data9  | ← FILO read pointer |
| 9     |        |                     |

buffer write pointer →

Figure 27: FIFO Read from Full Buffer


In FILO mode, reading one sample from the buffer will remove the newest sample and leave the older samples untouched, as seen in Figure 28.

| Index | Sample |                     |
|-------|--------|---------------------|
| 0     | Data0  | ← FIFO read pointer |
| 1     | Data1  |                     |
| 2     | Data2  |                     |
| 3     | Data3  |                     |
| 4     | Data4  |                     |
| 5     | Data5  |                     |
| 6     | Data6  |                     |
| 7     | Data7  | ← Sample Threshold  |
| 8     | Data8  | ← FILO read pointer |
| 9     |        |                     |

buffer write pointer →


Figure 28: FILO Read from Full Buffer



|   |   |   |
|---|---|---|
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## Revision History

| Revision | Description   | Date        |
|----------|---|-------------|
| 1.0      | Initial Release   | 27-Feb-2015 |
| 2.0      | POR, Double Tap, Standby requirement to change digital engine registers.<br>Updated Motion Interrupt Feature Description.<br>Updated reference in Buffer Operation section.<br>Updated Table 13: Acceleration (g) Calculation table values.   | 01-Apr-2015 |
| 3.0      | Updated Power-On Procedure section.<br>Note was added to check relevant Technical Note for information related to Power-On Procedure.<br>Tables numbering has been updated to reflect the change.<br>Removed negative self test requirement.  | 15-May-2015 |
| 4.0      | Updated I2C Writing/Reading to/from KX112 section.<br>Updated I2C Timing Diagram.<br>Update title for Power-On Procedure Technical Note.<br>Updated Wake-up Threshold Equation.<br>Updated Product Features.  | 16-Jun-2015 |
| 5.0      | Updated product photo, functional diagram.<br>Revised I2C section to include support for alternative I2C address.<br>Updated 3-Wire Read and Write Registers section.<br>Revised RoHS/REECH compliance Changed SELF_TEST register description to W from R/W and added a note.<br>Clarified pin description in Table 4.<br>Fixed SMP to SMP_TH in BUF_CNTL1, BUF_CNTL2, in Table 24.<br>Indicated TRIG pin as a possible source to assert the trigger event in Tiger Mode.<br>Added Product Notice.  | 18-Jan-2016 |
| 6.0      | Updated Functional Diagram.<br>Updated Noise in Mechanical Spec table.<br>Updated IO_VDD max parameter in Electrical Spec table.<br>Removed input pull down current information in Electrical Spec table.<br>Updated Bandwidth (-3dB) setting in Electrical Spec table and corresponding note under the table.<br>Added supported I2C addresses to Electrical Spec table.<br>Updated Start Up Time and Current Profile figures.<br>Updated 3-Wire Read and Write Registers section.<br>Revised RoHS/REACH compliance section.<br>Revised Pin Description table.<br>Removed Test Specifications (Min/Max values are already reflected in Mechanical Spec table). | 15-Jan-2018 |

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|  |  |  |
|--|--|--|
|  | <p>Revised Package Outline Drawing.<br/> Updated 3-wire and 4-wire connection diagrams.<br/> Corrected R/W Status in Register Map.<br/> Revised Sample Buffer, Motion Interrupt, Free fall Detect, Device Orientation engine descriptions.<br/> Updated SPI3E, PC1, RES, IIR_BYPASS, SMP_TH, BUFE, BFI, WMI, IEL1, IEL2, TDTS, SRST, BUF_TRIG bit descriptions.<br/> Revised INT1, INT2 pin descriptions.<br/> Revised CNTL3, LP_CNTL, SELF-TEST, INT_REL, FFC, FFCNTL, BUF_READ, BUF_CLEAR register descriptions.</p> |  |
|--|--|--|

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|-----------|-----------|------------|-----------|
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