

## N-Channel Enhancement Mode Power MOSFET

### Description

The RM100N60DF uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

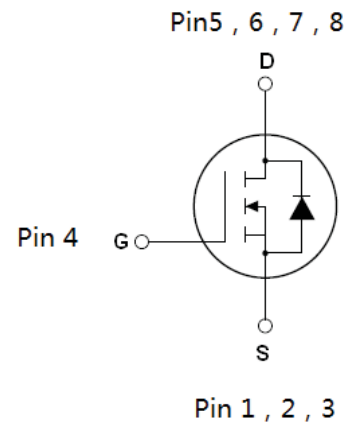
### General Feature

- $V_{DS} = 65V, I_D = 95A$   
 $R_{DS(ON)} < 4.6m\Omega @ V_{GS}=10V$  (Typ:3.8m $\Omega$ )  
 $R_{DS(ON)} < 7m\Omega @ V_{GS}=4.5V$  (Typ:5.6m $\Omega$ )
- Special process technology for high ESD capability
- High density cell design for ultra low  $R_{dson}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

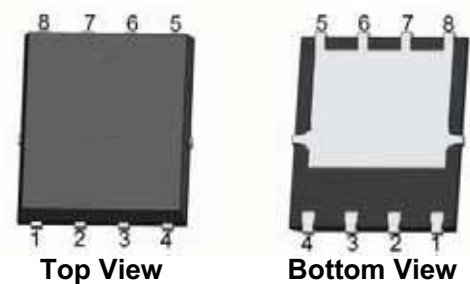
### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply
- Halogen-free

**100% UIS TESTED!**  
**100%  $\Delta V_{ds}$  TESTED!**



**Schematic diagram**



**Top View**

**Bottom View**

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AN60	RM100N60DF	DFN5X6-8L	-	-	-

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25^\circ C$	95	A
		$T_C=100^\circ C$	60	
		$T_C=25^\circ C$	45	
Continuous Drain Current (Package Limited)				
Drain to Source Voltage	$V_{DS}$	-	65	V
Gate to Source Voltage	$V_{GS}$	-	$\pm 20$	V
Pulsed Drain Current	$I_{DM}$	-	340	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.1mH, T_C=25^\circ C$	31	mJ
Power Dissipation	$P_D$	$T_C=25^\circ C$	74	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 150	$^\circ C$

## Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	°C/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.7	°C/W

## Electrical Characteristics ( $T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	65	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.6	2.4	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS}=0V, V_{DS}=60V, T_J=25^{\circ}\text{C}$	-	-	1	$\mu A$
		$V_{GS}=0V, V_{DS}=60V, T_J=100^{\circ}\text{C}$	-	-	100	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	3.8	4.6	m $\Omega$
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=10A$	-	5.6	7	m $\Omega$
Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=20A$	-	60	-	S
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}$ Open, $f=1\text{MHz}$	-	1.3	-	$\Omega$

## Dynamic Characteristics

Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=30V, f=1\text{MHz}$	-	1978	-	pF
Output Capacitance	$C_{oss}$		-	870	-	
Reverse Transfer Capacitance	$C_{rss}$		-	56	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=30V, I_D=20A, V_{GS}=10V$	-	41	-	nC
Total Gate Charge	$Q_g(4.5V)$		-	25	-	
Gate to Source Charge	$Q_{gs}$		-	5	-	
Gate to Drain (Miller) Charge	$Q_{gd}$		-	11	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=20A, V_{GS}=10V, R_G=10\Omega,$	-	10	-	ns
Rise time	$t_r$		-	8	-	
Turn off Delay Time	$t_{d(off)}$		-	34	-	
Fall Time	$t_f$		-	10	-	

## Reverse Diode Characteristics

Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_F=30A$	-	0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_R=30V, I_F=20A, dI_F/dt=400A/\mu s$	-	30	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	68	-	nC

## RATING AND CHARACTERISTICS CURVES (RM100N60DF)

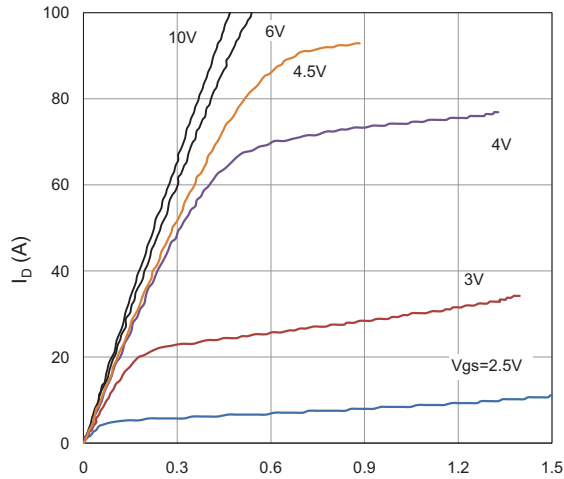


Fig 1. Typical Output Characteristics

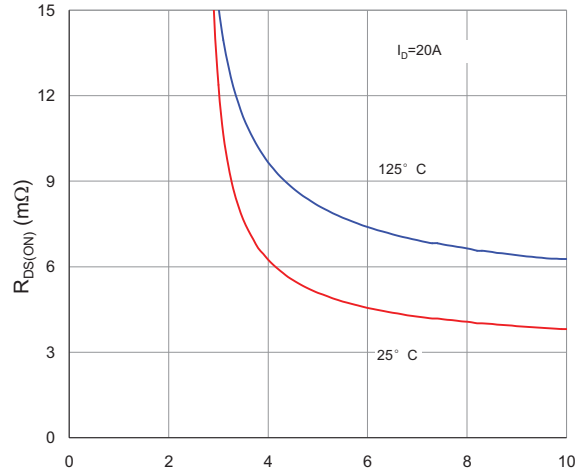


Figure 2. On-Resistance vs. Gate-Source Voltage

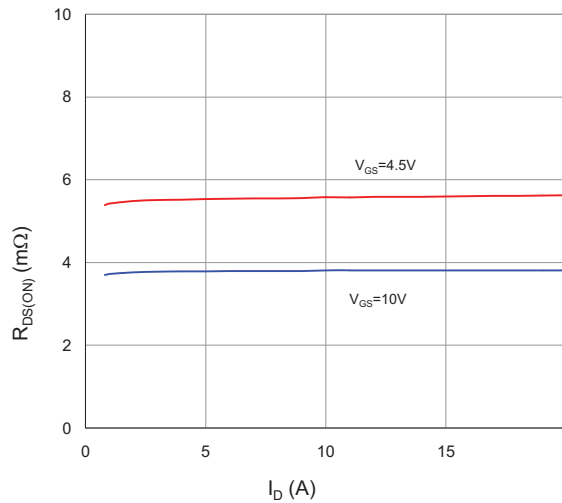


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

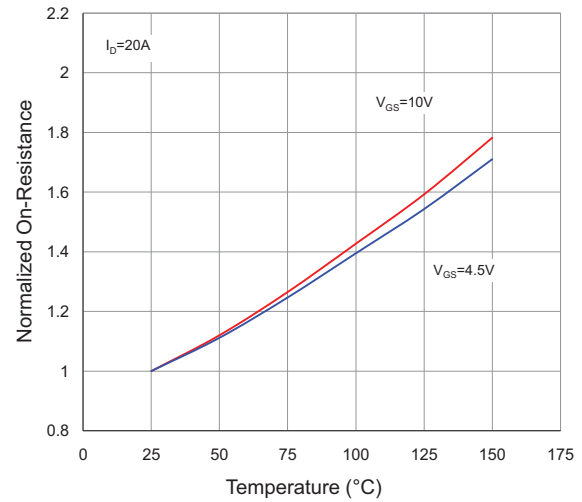


Figure 4. Normalized On-Resistance vs. Junction Temperature

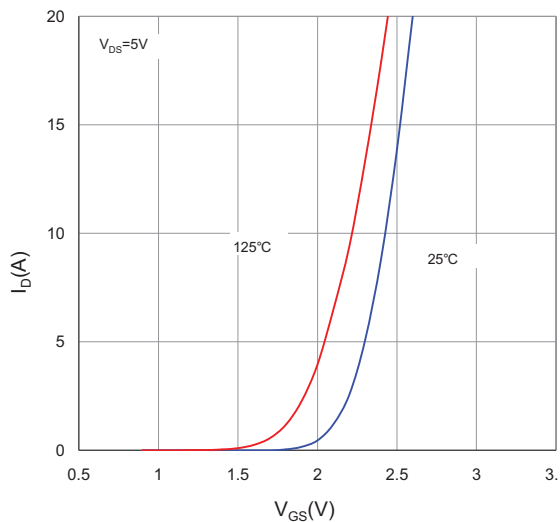


Figure 5. Typical Transfer Characteristics

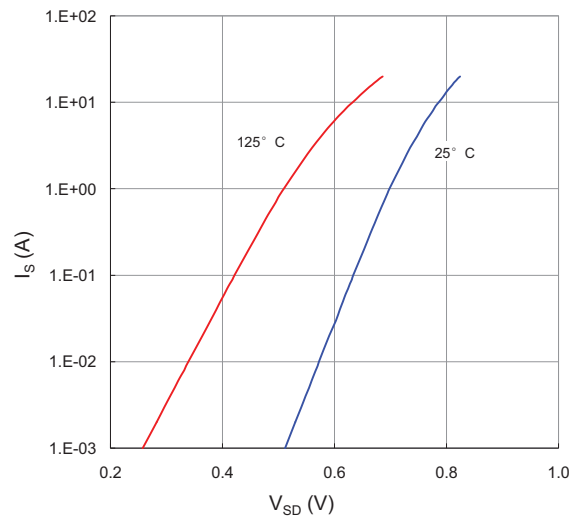


Figure 6. Typical Source-Drain Diode Forward Voltage

## RATING AND CHARACTERISTICS CURVES (RM100N60DF)

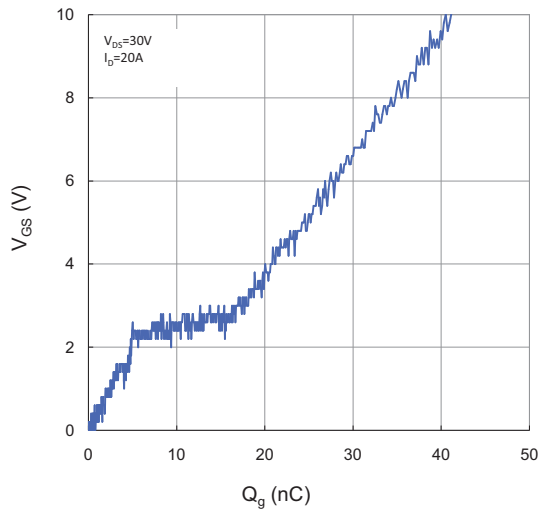


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

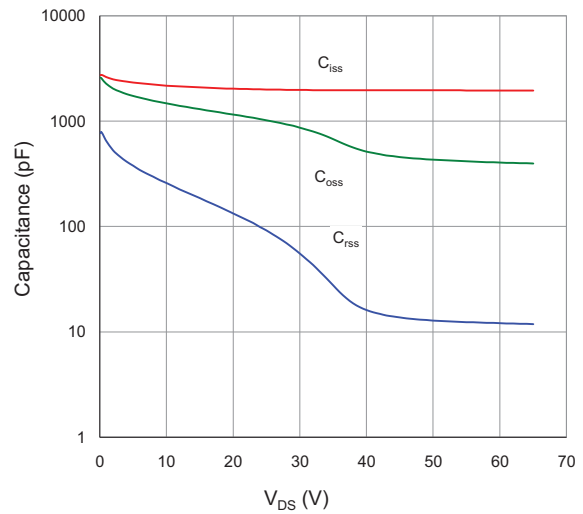


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

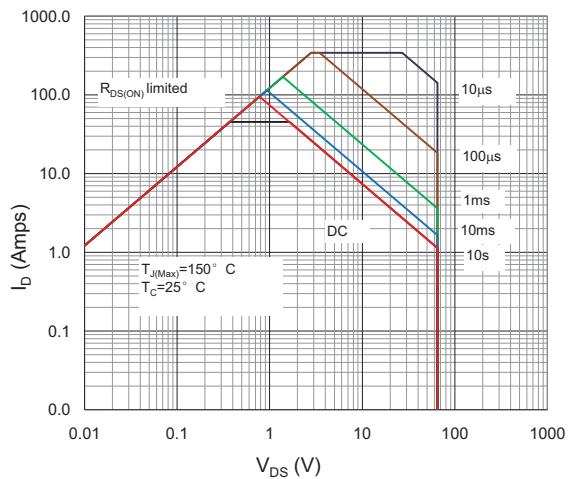


Figure 9. Maximum Safe Operating Area

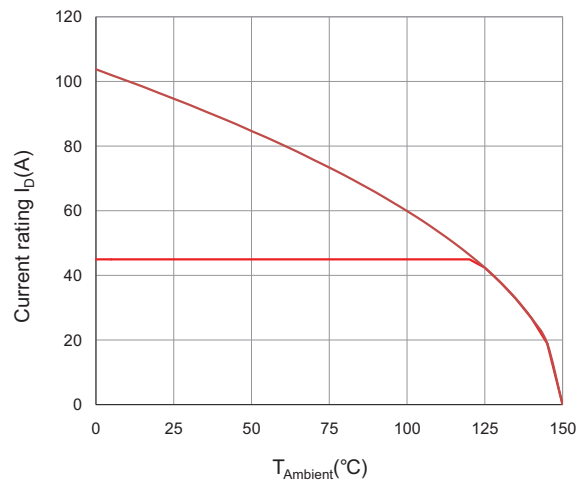


Figure 10. Maximum Drain Current vs. Case Temperature

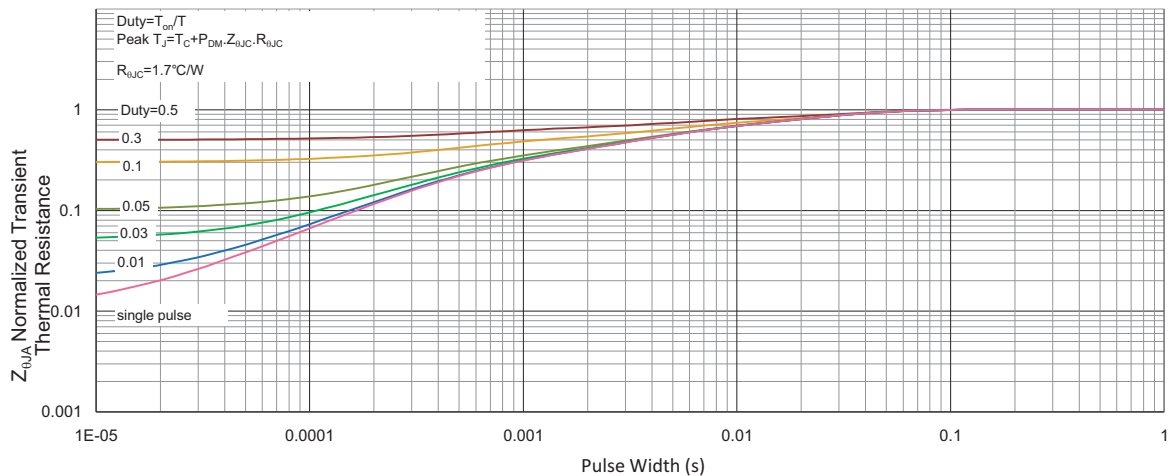
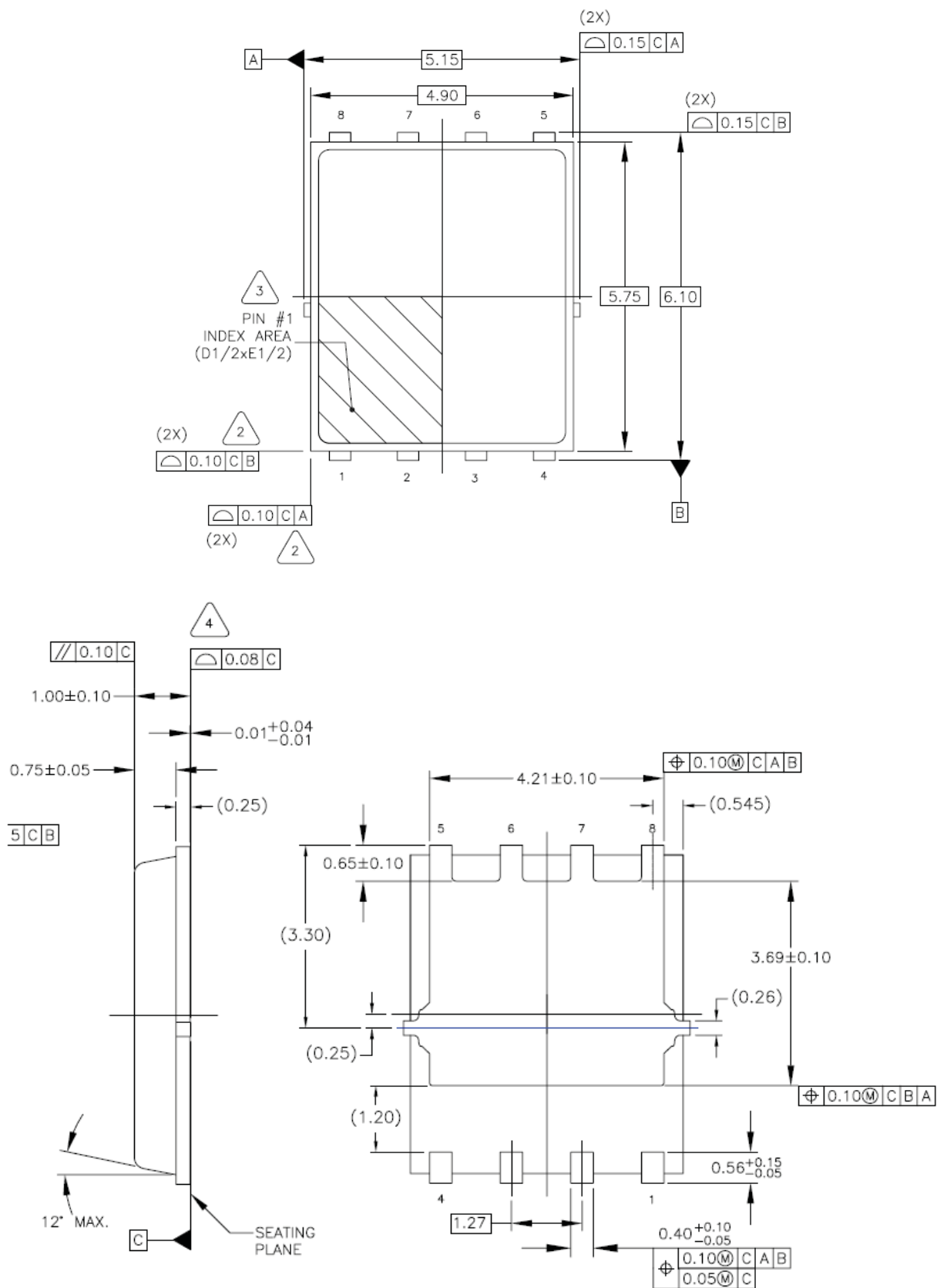


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

## DFN5X6-8L Package Information



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