Title	***Reference Design Report for a 140 W USB PD 3.1 / EPR Power Supply with 5 V / 9 V / 12 V / 15 V / 20 V / 28 V Outputs Using InnoSwitch™5-Pro PowiGaN™ INN5377F-H905, HiperPFS™-5 PFS5277F***
Specification	90 VAC – 265 VAC Input; 5 V / 3 A; 9 V / 3 A; 12 V / 5 A; 15 V / 5 A; 20 V / 5 A; 28 V / 5 A Outputs
Application	USB PD Adapter and Power Strips
Author	Applications Engineering Department
Document Number	RDR-1002
Date	April 26, 2024
Revision	1.2

Summary and Features

- InnoSwitch5-Pro – SR ZVS flyback switcher IC with integrated high-voltage PowiGaN, synchronous rectification and FluxLink™ feedback
- 140 W USB PD 3.1 design supports EPR 28 V / 5 A output
- >95% full load efficiency at 28 V / 5A, 230 VAC
- >94% full load efficiency at 28 V / 5 A, 90 VAC
- <50 mW no-load input power
- Ultra-compact 80.5 x 63.5 x 20 mm PCB design includes AC prong space
- Zero voltage switching in DCM operating conditions
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
- Meets DOE6 and CoC v5 2016 efficiency requirement
- Output overvoltage and overcurrent protection
- Integrated thermal protection

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a high power density 140 W USB PD 3.1 Extended Power Range (EPR) power supply using two PowiGaN-based devices: HiperPFS-5 PFS5277F for the Power Factor Correction (PFC) stage and InnoSwitch5-Pro INN5377F-H905 for the flyback stage, paired with Injoinic IP2756 as the USB PD controller. The USB PD source capabilities of the power supply are listed below.

- 5 V / 3 A (Fixed Supply)
- 9 V / 3 A (Fixed Supply)
- 12 V / 5 A (Fixed Supply)
- 15 V / 5 A (Fixed Supply)
- 20 V / 5 A (Fixed Supply)
- 28 V / 5 A (EPR Fixed Supply)
- 15 V – 28 V / 5 A (EPR Adjustable Voltage Supply)

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics specifications, and performance data.

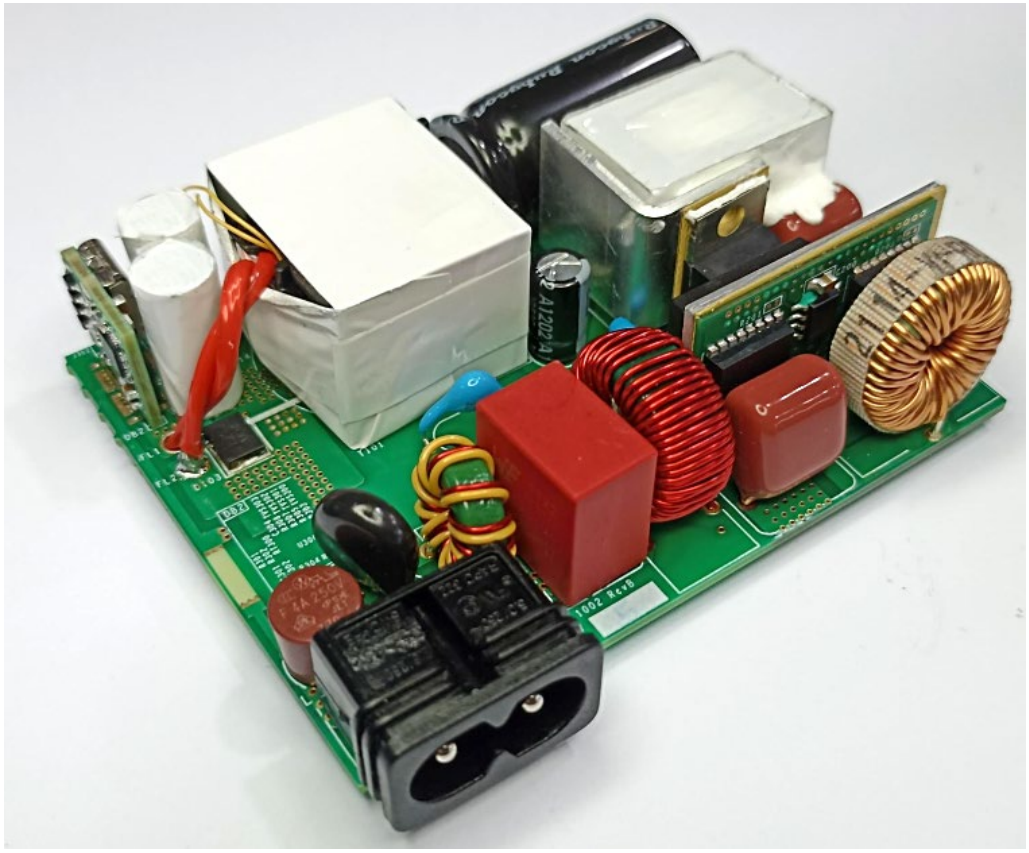


Figure 1 – RDR-1002 Board Picture.

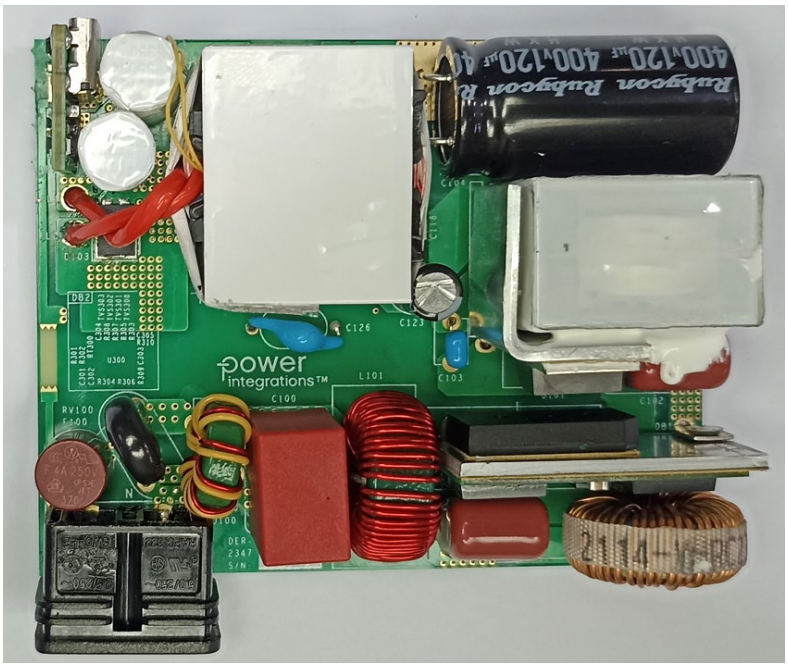


Figure 2 – Populated Circuit Board Photograph – Mainboard Top.

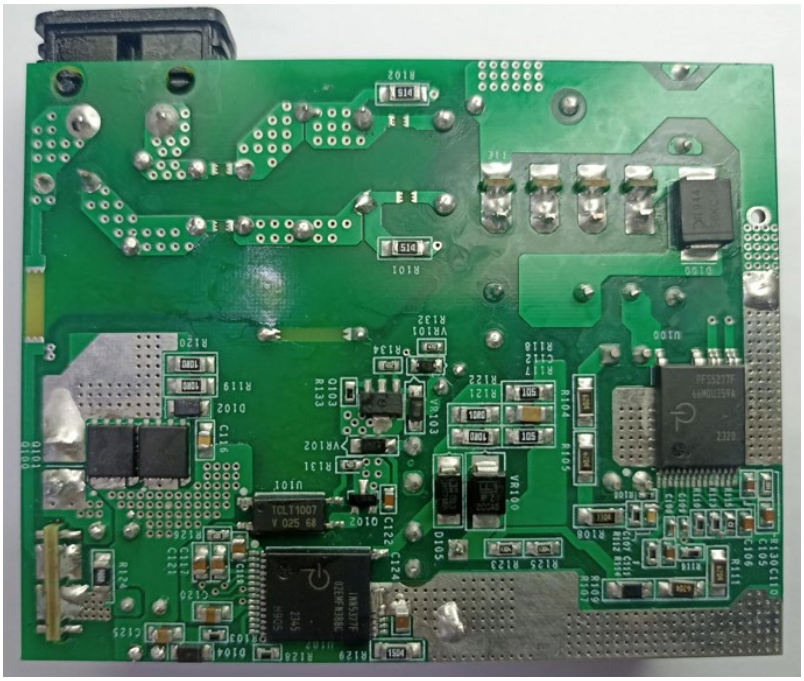


Figure 3 – Populated Circuit Board Photograph –Mainboard Bottom.

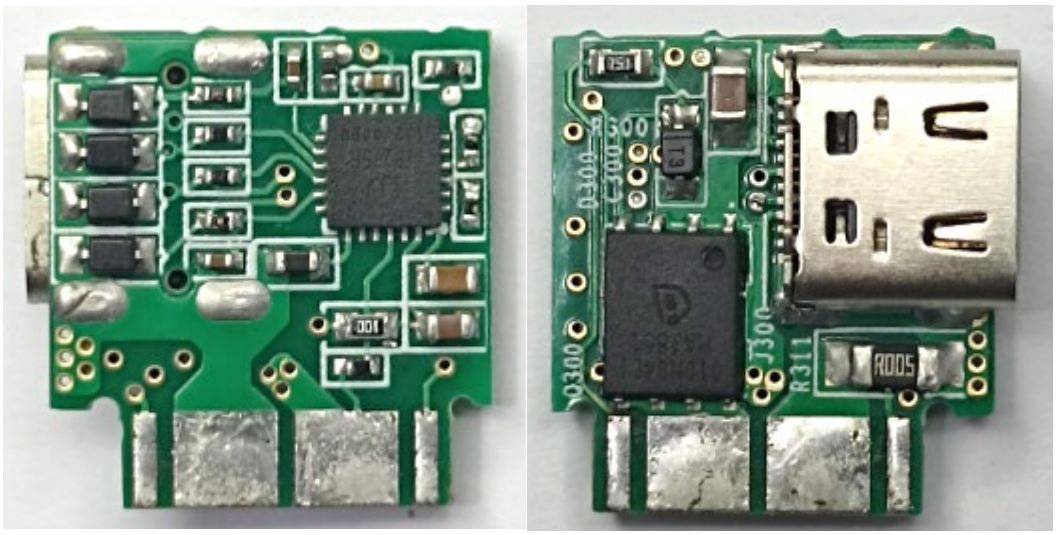


Figure 4 – Populated Circuit Board Photograph – USB PD Board (Left: Top, Right: Bottom).

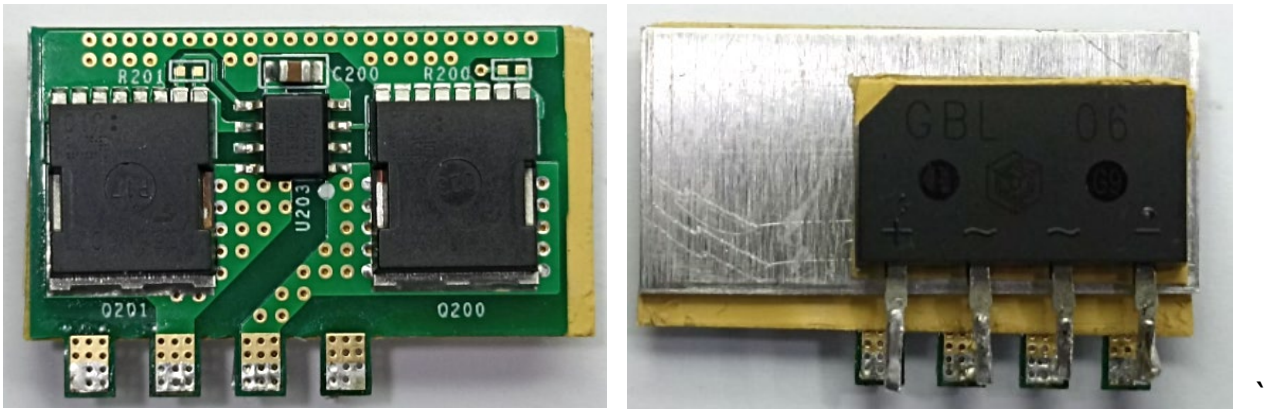


Figure 5 – Populated Circuit Board Photograph – Active Bridge Assembly (Left: Top, Right: Bottom).

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				75	mW	Measured at 230 VAC.
5 V Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			200	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(5\ V)}$			3.0	A	±3%
Full Load Efficiency	$\eta_{(5\ V)}$		93.8		%	Measured at 230 VAC from AC Receptacle to the Flyback output capacitor.
Continuous Output Power	$P_{OUT(5\ V)}$			15	W	
9 V Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			200	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(9\ V)}$			3.0	A	±3%
Full Load Efficiency	$\eta_{(9\ V)}$		94.5		%	Measured at 230 VAC from AC Receptacle to the Flyback output capacitor.
Continuous Output Power	$P_{OUT(9\ V)}$			27	W	
12 V Setting						
Output Voltage	$V_{OUT(15\ V)}$		12.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			175	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(15\ V)}$			5.0	A	±3%
Full Load Efficiency	$\eta_{(15\ V)}$		94.2		%	Measured at 230 VAC from AC Receptacle to the Flyback output capacitor.
Continuous Output Power	$P_{OUT(15\ V)}$			75	W	
15 V Setting						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			150	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(15\ V)}$			5.0	A	±3%
Full Load Efficiency	$\eta_{(15\ V)}$		94.5		%	Measured at 230 VAC from AC Receptacle to the Flyback output capacitor.
Continuous Output Power	$P_{OUT(15\ V)}$			75	W	
20 V Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			150	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(20\ V)}$			5	A	±3%
Full Load Efficiency	$\eta_{(20\ V)}$		94.6		%	Measured at 230 VAC from AC Receptacle to the Flyback output capacitor.
Continuous Output Power	$P_{OUT(20\ V)}$			100	W	

28 V Setting						
Output Voltage	$V_{OUT(28\ V)}$		28.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(28\ V)}$			125	mV	Measured at End of Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(28\ V)}$			5	A	±3%
Full Load Efficiency	$\eta_{(28\ V)}$		94.7		%	Measured at 230 VAC from AC Receptacle to the Flyback output capacitor.
Continuous Output Power	$P_{OUT(28\ V)}$			140	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

3 Schematic

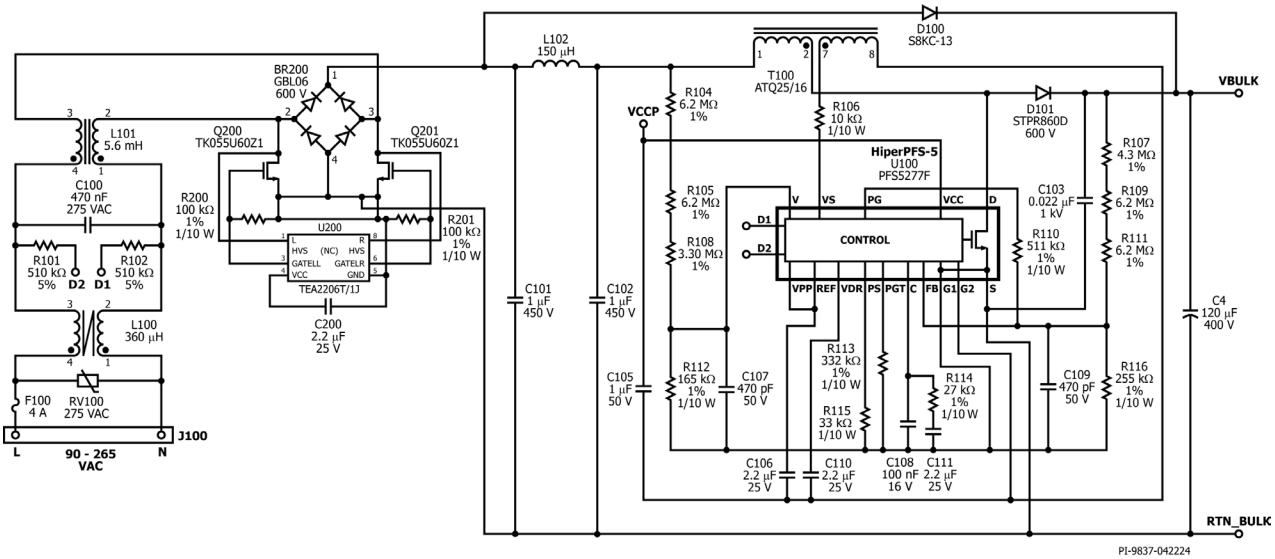


Figure 6 – Schematic, Input and PFC Section.

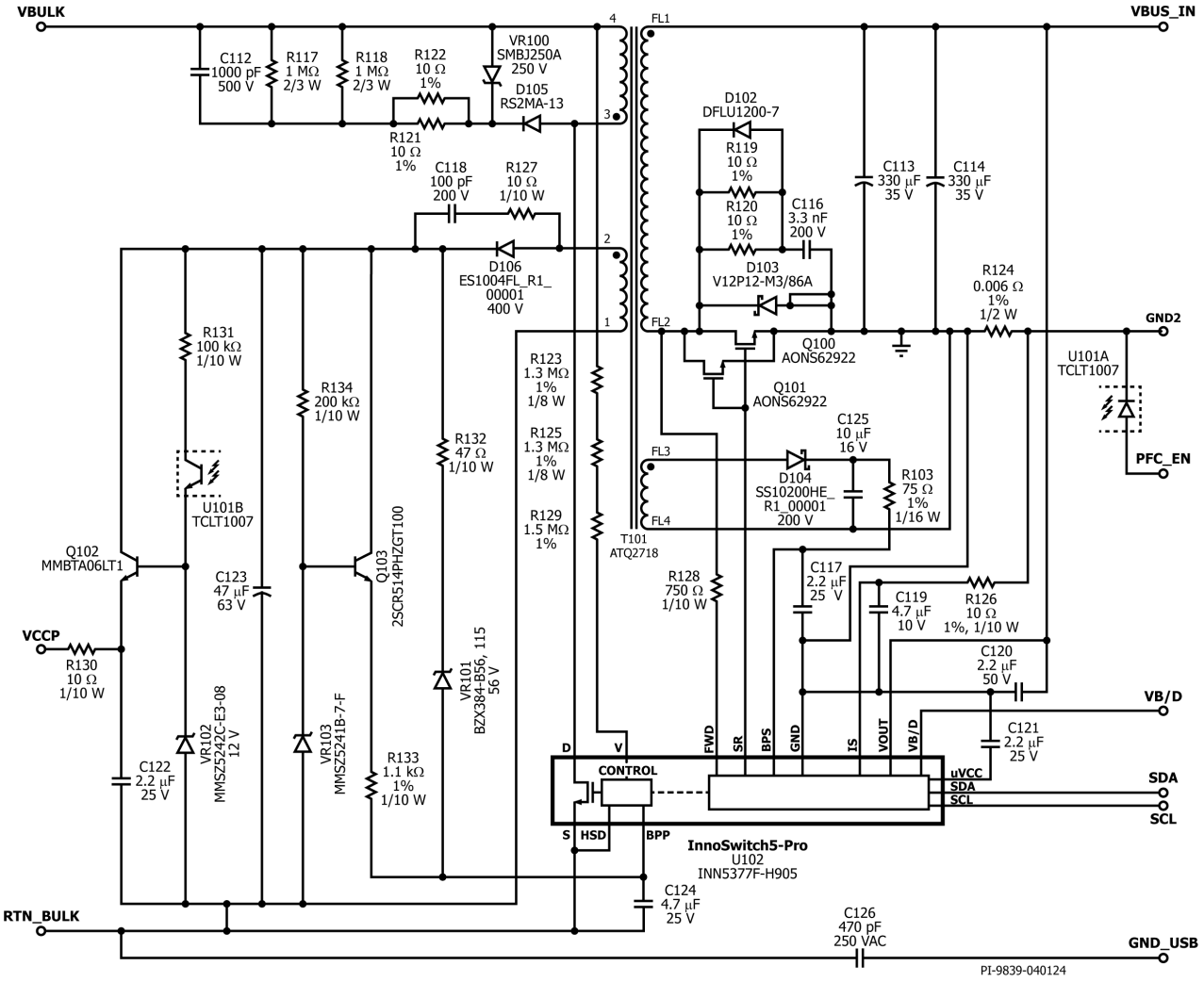


Figure 7 – Schematic, Flyback Section.

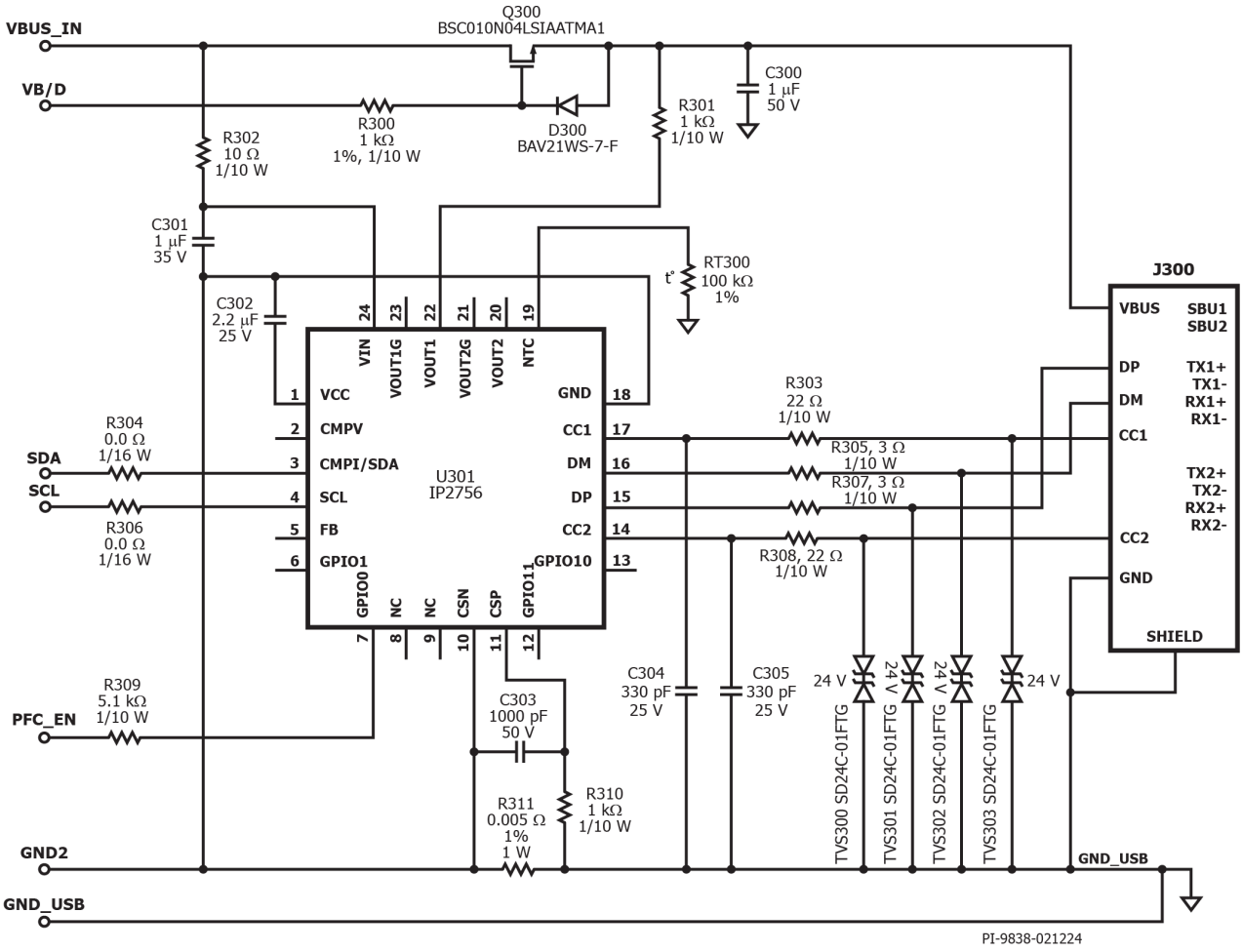


Figure 8 – Schematic, USB PD Section.

4 Circuit Description

The input stage is a boost PFC powered by a HiperPFS-5 IC and the second stage is a DC-DC flyback converter using a InnoSwitch5-Pro IC. The AC input is rectified using a semi-active bridge to reduce diode losses. The circuit is separated into 3 assemblies: mainboard, active bridge assembly and USB PD board.

4.1 Input EMI Filter

Input fuse F100 provides safety protection from catastrophic failure, varistor RV100 protects against line transients. EMI suppression components are comprised of common-mode chokes L100 and L101, X capacitor C100, differential-mode choke L102, film capacitors C101 and C102. Resistors R101 and R102 are required to discharge the energy stored in the X capacitors once the AC input lines are disconnected.

4.2 Active Bridge Assembly

Bridge rectifier BR200 rectifies the AC line voltage and provides a full wave rectified voltage to the PFC stage. Active Bridge FETs Q200 and Q201 effectively reduce the power consumption of the two low-side diodes in the bridge rectifier. The FETs are paralleled across the diode and turn on when the diodes are supposed to turn on. The low resistance of the FETs result in lower voltage drop compared to the diode which result in significant efficiency increase. Active Bridge controller U200 drives the active bridge FETs at the proper timings.

4.3 HiperPFS-5 PFC Controller

The HiperPFS-5 family incorporates a novel quasi-resonant DCM PFC controller with 750 V PowiGaN, X capacitor discharge, and high-voltage self-start-up in a low-profile power package. HiperPFS-5 devices eliminate the need for external current sense resistors and their associated power loss and use an innovative control technique that adjusts the switching frequency over output load, input line voltage, and input line cycle. Low switching and conduction losses with PowiGaN, and other efficiencies of high integration allows for designs of up to 220 W without a heat sink.

The PFC power stage comprises of the boost inductor T100, boost diode D101, bypass diode D100, bulk capacitor C104, and HiperPFS-5 U100. A small decoupling capacitor C103 is added for EMI.

The VALLEY SENSING (VS) pin is connected to the auxiliary winding on inductor T100 through an external resistor R106. The resistor is used to limit the current through VS pin and for fine adjustment of timing for valley switching.

The VOLTAGE MONITOR (V) pin is tied to the rectified high-voltage DC rail through an approximately 100:1 high impedance resistor dividers R104, R105, R108 and R112. A small ceramic capacitor C107 form an 80 μs time constant to bypass any switching noise present on the rectified DC bus.

The POWER SELECTION (PS) resistor R115 programs the power limit of the device to 70% of its nominal output power. This scheme maximizes efficiency by selecting PFS5277F that has lower $R_{DS(ON)}$ while keeping the RMS current low.

The REF pin is connected to a bypass capacitor C106 while the VPP pin must be connected to REF pin. Capacitor C108 and series R-C circuit R114/C111 connected to COMPENSATION (C) pin for loop pole / zero compensation.

The FEEDBACK (FB) pin is connected to the main voltage regulation feedback resistor divider network of upper FB resistors R107, R109, and R111 and bottom FB resistor R116. This design utilizes the boost follower function of the HiperPFS-5 IC which enables low output voltage for low-line input and higher output voltage for high-line input. This allows higher efficiency at low-line due to the lower boost ratio.

The divider ratio was selected to ensure that nominal low-line PFC output voltage is 255 V. At high-line input, the PG pin is pulled low which connects the resistor R110 across the bottom FB resistor thereby increasing the PFC output voltage. The value of R110 was selected to set the nominal high-line PFC output voltage to 380 V. A small ceramic filter capacitor C109 is added to form an 80 μs time constant with the bottom FB resistor.

The BIAS POWER (VCC) pin is used to power the IC and comes from the output of the linear regulator that is part of the PFC disable circuit. Capacitor C105 is the bypass capacitor of VCC.

4.3.1 PFC Disable Circuit

The PFC is disabled during lower output power (input power <75 W) to optimize the system efficiency. The USB PD controller at the output stage computes the output power and decides whether to turn the PFC on or off. The PFC enable signal drives the optocoupler U101 connected to the base of the linear regulator comprised of linear pass BJT Q102, base resistor R131, Zener diode VR102 and filter capacitor C122. When the signal from the secondary is high, base current for the BJT passes through the output side of the optocoupler and the VCC of the HiperPFS-5 IC is supplied, turning it on. On the other hand, when the PFC Enable signal from the secondary is low, no base current flows on the transistor and the HiperPFS-5 IC is disabled. Note that this method of disabling the PFC stage works only with the non self-bias parts PFS527xF.

4.4 InnoSwitch5-Pro IC Primary

InnoSwitch5-Pro IC (U102) controls the DC-DC stage flyback converter. One end of the transformer T101 primary is connected to the PFC output DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch5-Pro IC (U102).

The UNDER/OVER INPUT VOLTAGE (V) pin of the InnoSwitch5-Pro IC provides input under/over voltage sensing and is connected to the DC bus via resistor network R123, R125, and R129.

The value of PRIMARY BYPASS (BPP) capacitor C124 sets the current limit of the InnoSwitch5-Pro to either Standard mode or Increased I_{LIM} mode. In this design, increased I_{LIM} mode was selected.

The primary RCD clamp limits the peak drain voltage of U102 at the instant of the switch inside U102. The energy stored in the leakage inductance of transformer T101 is transferred to the capacitor C112 through the diode D105. Resistors R121 and R122 limit the peak current going into the capacitor C112. Resistors R117 and R118 dissipate the energy in C112.
Transient voltage suppressor VR100 is used to protect the InnoSwitch5-Pro IC from excessive drain voltages during abnormal conditions applied to the power supply.

The InnoSwitch5-Pro IC is self-starting, using an internal high-voltage current source to charge the BPP capacitor C124 when AC input is first applied. During normal operation, the primary-side block of the IC is powered by the primary auxiliary bias supply.

Output of the auxiliary (or bias) winding is rectified using diode D106 and filtered using capacitor C123. Linear regulator circuit is composed of BJT Q103, R134, and Zener diode VR103 ensures sufficient current flows through R133 into the BPP pin of the InnoSwitch5-Pro IC. By injecting sufficient current into BPP pin, the internal current source of U102 is not required to charge C124, and power consumption is minimized during no-load condition and at normal operation.

Output regulation is achieved using modulation control, where the frequency and I_{LIM} of switching cycles are adjusted based on the output load. At high load, the converter operates at a high switching frequency with a high value of I_{LIM} in the selected current limit range while at light load or no-load, the converter switches at a low frequency with a low value of I_{LIM}. Once a cycle is enabled, the switch remains on until the primary current ramps to the device current limit for the specific operating state.

The latch-off/auto-restart primary-side overvoltage protection is implemented using Zener diode VR101 with current limiting resistor R132. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR101, which then causes a current to flow into the BPP pin of InnoSwitch5-Pro IC U102. If the current flowing into the BPP pin increases above the I_{SD} threshold, the U102 controller latches off to prevent any further increase in output voltage.

Y capacitor C126 connected between bridge rectifier return and secondary return rail is used to reduce common-mode EMI.

4.5 InnoSwitch5-Pro IC Secondary

The secondary-side of the InnoSwitch5-Pro IC provides output voltage, output current sensing, and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by SR FETs Q100, Q101, and diode D103, and filtered by capacitors C113 and C114. Resistors R119 and R20, and capacitor C116 reduce the peak drain voltage of SR FETs. Diode D102 is used to reduce the losses that happen when the SR FET's body diode conducts.

The gates of Q100/Q101 are turned on by the secondary-side controller of IC U102, based on the winding voltage sensed via resistor R128 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off, when the voltage drop across the MOSFET falls below a threshold of approximately $V_{SR(TH)}$ mV.

Zero Voltage Switching (ZVS) can be achieved with InnoSwitch5-Pro IC during DCM. If the device is configured via I^2C to operate in SR-ZVS mode, prior to primary switch turn on, the SR FET is turned on to make the output capacitor energize the transformer magnetizing inductance. This causes magnetizing current to build up such that when the SR FET is then turned off, the primary magnetizing current discharges the capacitance at the drain of the primary switch before it is turned on. The duration of the SR FET turn-on and the delay after turn off before primary switch turn on can both be configured through an I^2C command.

The secondary-side of the IC U102 is self-powered from either the secondary winding forward voltage or the output voltage. However, to improve the system efficiency and reduce the secondary-side internal consumption, a bias winding circuit was used. It is designed to supply current to the IC when the output voltage is set to 28 V. At lower output voltage setting, the supply comes from the OUTPUT VOLTAGE (VOUT) pin. Bias winding voltage is rectified by diode D104 and filtered by capacitor C125. Resistor R103 limits the current flowing to the BPS pin of U102. Capacitor C117 connected to the BPS pin of IC U102 provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R124. The current measurement is filtered with resistor R126 and capacitor C119, and then monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of up to 32 mV configured by the USB PD controller via I^2C interface is used to reduce losses. Once the threshold is exceeded, the InnoSwitch5-Pro IC responds depending on its configuration. In this design, the InnoSwitch5-Pro IC is set to shut down the power supply during an overcurrent event, but it can also be configured to maintain a fixed output current by using variable frequency and variable primary switch current limit control schemes.

For constant current (CC) operation, when the output voltage falls below 5 V, the secondary-side controller inside InnoSwitch5-Pro IC will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C117 via resistor R128 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level, the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch5-Pro IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set by the USB PD controller via the I^2C interface. Output voltage regulation is achieved by variable frequency and variable primary switch peak current limit control schemes. Capacitor C120 is used as a decoupling capacitor for the VOUT pin.

4.6 USB Type-C and PD Interface

In this design, Injoinic IP2756 (U301) is the USB Type-C and USB PD3.1/EPR 28 V controller. The IP2756 device is powered directly from the flyback output voltage VBUS_IN. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which the USB Type-C plug is connected.

The IP2756 IC communicates with InnoSwitch5-Pro IC through the I^2C interface using the SCL and SDA lines in which it sets several command registers, such as the CV, CC, VKP, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold and output undervoltage threshold registers of the InnoSwitch5-Pro IC, respectively. The status of the InnoSwitch5-Pro IC is read by the IP2756 IC from the telemetry registers also using the I^2C interface.

N-channel MOSFET Q300 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle J300. MOSFET Q300 is controlled by-the VB/D pin on the InnoSwitch5-Pro IC which can provide around 7 V above the output voltage to drive the N-channel MOSFET. Diode D300 is connected across the Source and Gate terminals of Q300 and resistor R300 is connected from the Gate terminal of Q300 to the VB/D pin to provide a discharge path for the bus voltage when Q300 is turned off. Capacitor C300 is used as decoupling capacitor at the output for ESD protection and output voltage ripple reduction.

The IP2756 IC senses the output current through resistor R311. Capacitor C301 is used as decoupling capacitor on the VIN pin of U301 and capacitor C302 is used as decoupling capacitor on VCC pin of U301. Resistors R303, R305, R307, R308, capacitors C304, C305 and transient voltage suppressors TVS300, TVS301, TVS302, and TVS303 are used to protect the CC1/CC2 and D+/D- lines from ESD events. Thermistor RT300 is used to sense USB Type-C connector temperature.

5 PCB Layout

5.1 Main Board

Material: FR4, 2 oz copper, 1.6 mm thick

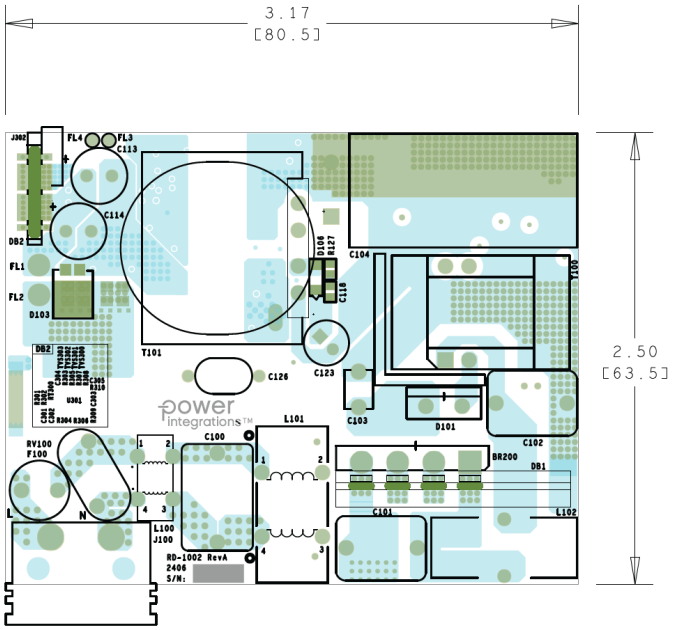


Figure 9 – Main Board Printed Circuit Layout, Top.

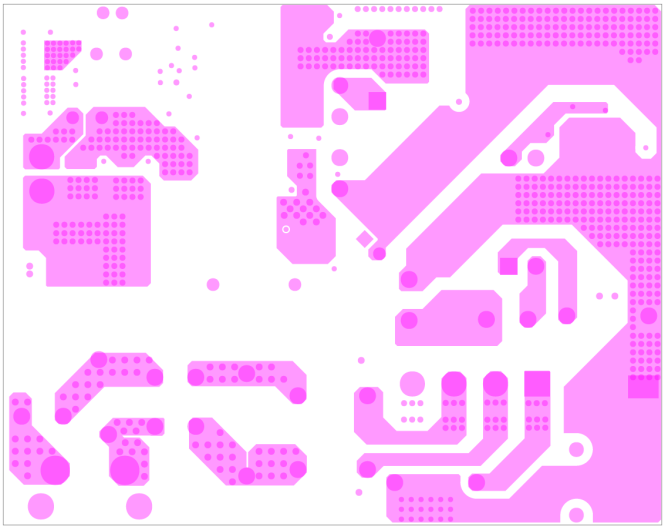


Figure 10 – Main Board Printed Circuit Layout, Inner 1.

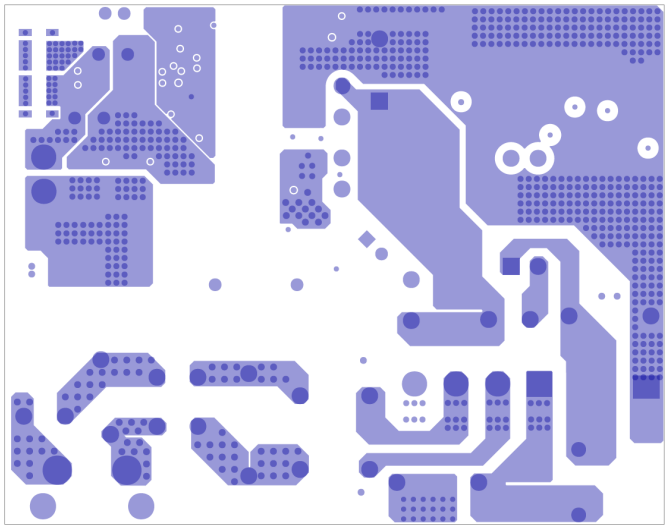


Figure 11 – Main Board Printed Circuit Layout, Inner 2.

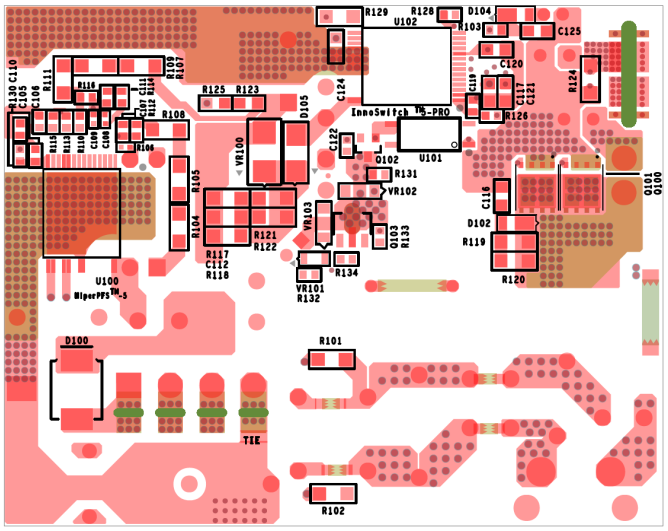


Figure 12 – Main Board Printed Circuit Layout, Bottom.

5.2 Active Bridge Board

Material: FR4, 2 oz copper, 0.8 mm thick

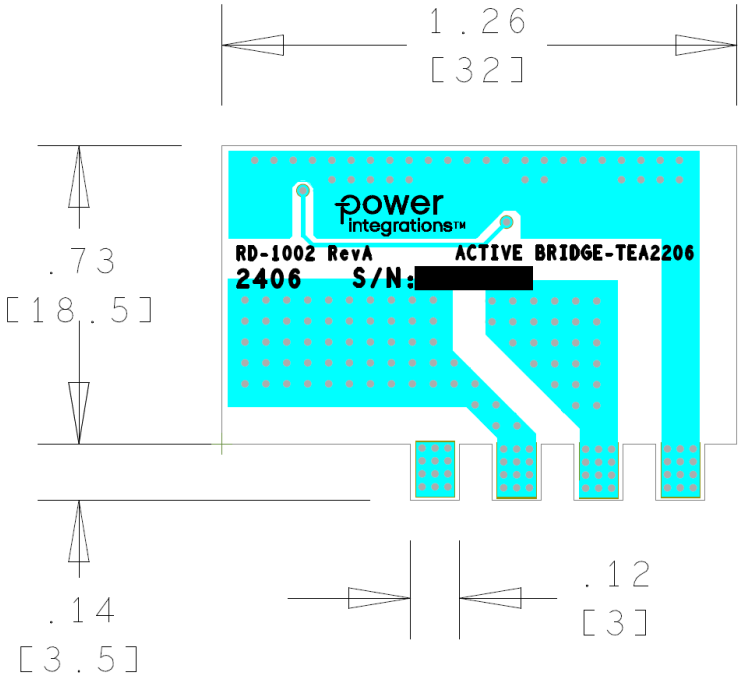


Figure 13 – Active Bridge Board Printed Circuit Layout, Top.

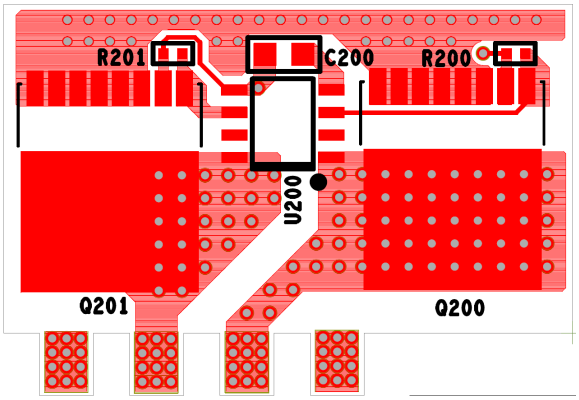


Figure 14 – Active Bridge Board Printed Circuit Layout, Bottom.

5.3 USB PD Board

Material: FR4, 2 oz copper, 1.6 mm inches thick

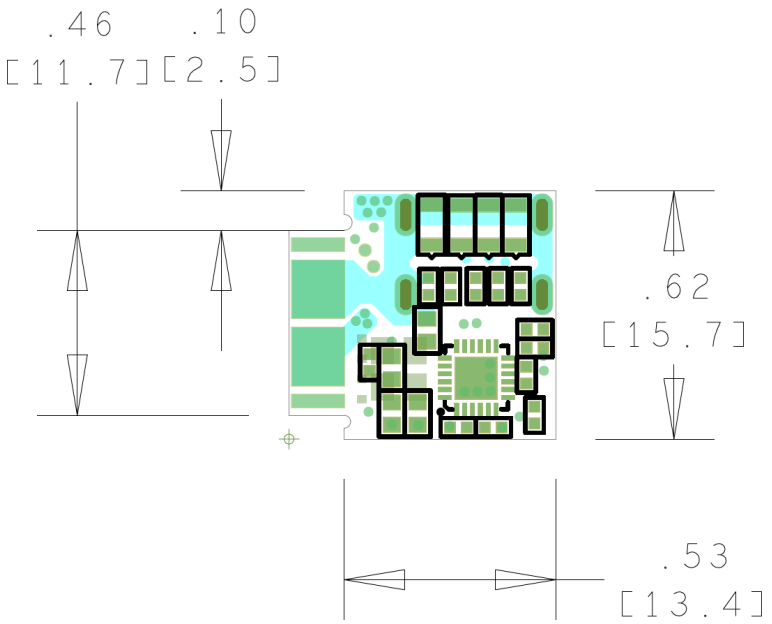


Figure 15 – USB PD Board Printed Circuit Layout, Top.

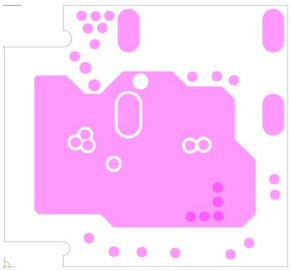


Figure 16 – USB PD Board Printed Circuit Layout, Inner 1.

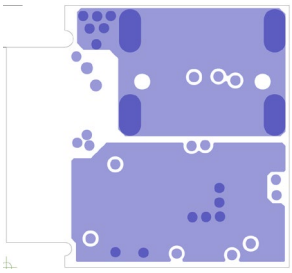


Figure 17 – USB PD Board Printed Circuit Layout, Inner 2

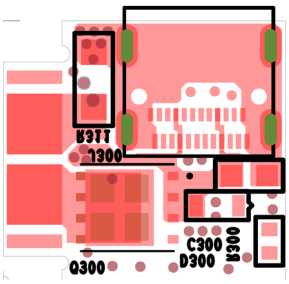


Figure 18 – USB PD Board Printed Circuit Layout, Bottom.

6 Bill of Materials

6.1 Electrical Parts

6.1.1 Main Board

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C100	CAP, FILM, 0.47 µF, 10%, 275 VAC, X2, RAD	890324024005	Würth
2	2	C101 C102	CAP, FILM, 1.0 µF, 10%, 450VDC, RADIAL	ECW-FD2W105Q1	Panasonic
3	1	C103	0.022 µF, ±10%, 1KV, X7R, Radial, -55°C ~ 125°C, 0.217" L x 0.157" W (5.50 mm x 4.00 mm)	RDER73A223K3M1H03A	Murata
4	1	C104	CAP, 120 µF 400 V Aluminum Electrolytic Cap Radial, Can 2000 Hrs @ 105°C	400HXW120MEFR16X30	Rubycon
5	1	C105	1 µF, ±10%, 50V, Ceramic Cap, X7R, 0603	06035C105KAT2A	AVX
6	2	C106 C110	2.2 µF, ±10%, 25V, Ceramic, X5R, 0603	GRM188R61E225KA12D	Murata
7	1	C107	470 pF, ±10%, 50V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CL10B471KB8NFNC	Samsung
8	1	C108	100 nF 16 V, Ceramic, X7R, 0402	L05B104KO5NNNC	Samsung
9	1	C109	470 pF, ±5%, 50V, C0G, NP0, -55°C ~ 125°C, Low ESL, 0402	C0402C471J5GACTU	Kemet
10	1	C111	2.2 µF, ±10%, 25 V, Ceramic, X7R, 0603, -55 to 125 °C	GRM188Z71E225KE43D	Murata
11	1	C112	1000 pF, ±10%, 500V, Ceramic Cap X7R, 1206	CL31B102KGFNNNE	Samsung
12	2	C113 C114	330 µF, ±20%, 35 V, Aluminum - Polymer Cap Radial, Can, 20 mΩ, 2000 Hrs @ 105°C, (8 x 16)	A750KW337M1VAAE020	KEMET
13	1	C116	3.3 nF, 200 V, Ceramic, X7R, 0805	08052C332KAT2A	AVX
14	2	C117 C121	2.2 µF, ±10%, 25V, X7R, r, -55°C ~ 125°C, 0805	CL21B225KAFVPNE	Samsung
15	1	C118	100 pF 200 V, Ceramic, NP0, 0603	C0603C101J2GAC7867	Kemet
16	1	C119	4.7 µF, ±10%, 10 V, Ceramic, X7S, 0603, -55°C ~ 125°C, Low ESL	C1608X7S1A475K080AC	TDK
17	1	C120	2.2 µF, ±10%, 50 V, Ceramic Cap, X7R, 0805	CGA4J3X7R1H225K125AE	TDK
18	1	C123	47 µF, 63 V, Electrolytic, Gen. Purpose, (6.3 x 13)	63YXJ47M6.3X11	Rubycon
19	1	C124	4.7 µF, ±20%, 25V, Ceramic Cap, X7R, 0805	CGA4J1X7R1E475M125AE	TDK
20	1	C125	10 µF, ±10%, 16V, X7R, Ceramic Cap, Surface Mount, MLCC 0805	CL21B106KOQNNNE	Samsung
21	1	C126	470 pF, ±10%, 250VAC, X1, Y1, Ceramic Cap, B, Radial, Disc	DE1B3RA471KN4AN01F	Murata
22	1	D100	Diode GEN PURPOSE, 800V, 8A, SMC	S8KC-13	Diodes, Inc.
23	1	D101	Diode, 600 V, 8 A, Through Hole, TO-220AC	STPR860D	Diodes, Inc.
24	1	D102	Diode, UFAST, 200 V, 1A, POWERDI123	DFLU1200-7	Diodes, Inc.
25	1	D103	Diode, Schottky, 120 V, 12 A, Surface Mount, TO-277A (SMPC)	V12P12-M3/86A	Vishay
26	1	D104	Diode, Schottky, 200 V, 1 A, SMT SOD-123HE	SS10200HE_R1_00001	Panjit
27	1	D105	1000 V, 1.5 A, Glass Passivated, DO-214AC	RS2MA-13-F	Diodes, Inc.
28	1	D106	Diode, Standard, 400 V, 1 A, SMT SOD-123FL	ES1004FL_R1_00001	Panjit
29	1	F100	4 A, 250 V, Fast, TR5	37014000410	Wickman
30	1	L100	CMC, 360 µH, Common Mode Choke (L100), wound on Toroid Core: 32-00315-00 (Green Color).	32-00459-00 TSD-5142	Power Integrations Premier Magnetics
31	1	L101	CMC, 5.6 mH, Common Mode Choke (L101), wound on Toroid Core: 32-00343-00 (Green Color).	32-00460-00 TSD-5143	Power Integrations Premier Magnetics
32	1	L102	150 µH, 3.4A, Vertical Toroidal	2114-V-RC	Bourns
33	2	Q100 Q101	MOSFET, N-CH, 120 V, 85 A (at VGS=10 V), Trench Power AlphaSGT 120 V TM technology, DFN5X6	AONS62922	Alpha & Omega Semi
34	1	Q102	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1	Infineon
35	1	Q103	NPN, 80V 0.7A, MEDIUM POWER, TO-243AA, SOT-89	2SCR514PHZGT100	Rohm Semi
36	2	R101 R102	RES, 510 kΩ, ±5%, ¼ W, Chip Resistor 1206, Moisture Resistant, Thick Film	RC1206JR-07510KL	YAGEO
37	1	R103	RES, 75 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF75R0V	Panasonic
38	4	R104 R105 R109 R111	RES, 6.2 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm Semi
39	1	R106	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ103X	Panasonic
40	1	R107	RES, 4.3 MΩ, ±1%, 1/4W Chip Resistor, 1206, Moisture Resistant, Thick Film	RC1206FR-074M3L	Yageo
41	1	R108	RES, 3.30 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF3304	Rohm Semi

42	1	R110	RES, 511 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF5113V	Panasonic
43	1	R112	RES, 165 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1653V	Panasonic
44	1	R113	RES, 332 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3323V	Panasonic
45	1	R114	RES, 27 kΩ, 1%, 1/10 W, Thick Film, 0603	RC0603FR-1327KL	YAGEO
46	1	R115	RES, 33 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ333V	Panasonic
47	1	R116	RES, 255 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2553V	Panasonic
48	2	R117 R118	RES, 1.0 MΩ, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J105V	Panasonic
49	2	R119 R120	RES, 10 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
50	2	R121 R122	RES, 10 Ω ±1%, 1/4W Chip Resistor 1206, Moisture Resistant Thick Film	RK73H2BTTD10R0F	KOA Speer
51	2	R123 R125	RES, 1.3 MΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1304V	Panasonic
52	1	R124	RES, 6 mΩ ±1%, 1/2W Chip Resistor 1206 Current Sense Metal Element	PR1206FKE7W0R006Z	Yageo
53	1	R126	RES, 10 Ω, ±1%, 1/10 W, Chip Resistor 0603, Moisture Resistant, Thick Film	RC0603FR-0710RL	Yageo
54	2	R127 R130	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
55	1	R128	RES, 750 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ751V	Panasonic
5	1	R129	RES, 1.50 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
57	1	R131	RES, 100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
58	1	R132	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
59	1	R133	RES, 1.1 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1101V	Panasonic
60	1	R134	RES, 200 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ204V	Panasonic
61	1	RV100	275 VAC, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
62	1	T100	Custom, RDR-1002 PFC Choke, ATQ25/16	POL-HP014	Power Integrations Premier Magnetics
63	1	T101	Custom, RDR-1002 Flyback Transformer, ATQ27/18.4	POL-INN062	Power Integrations Premier Magnetics
64	1	U100	HiperPFS-5, 185 W, Non self-biased, InSOP-T28F	PFS5277F	Power Integrations
65	1	U101	OPTOISOLATOR, 5 kV, TRANSISTOR, 4-SOP	TCLT1007	Vishay
66	1	U102	InnoSwitch5-Pro, InSOP-T28D	INN5377F-H905	Power Integrations
67	1	VR100	TVS Diode, UNIDIRECTIONAL, 250 VWM, 405 VC, DO214AA	SMBJ250A	Littelfuse
68	1	VR101	Diode, ZENER, 56 V, 300 mW, ±2%, SOD323	BZX384-B56,115	NXP Semi
69	1	VR102	Zener Diode, 12V, ±2%, 500 mW, SMT, SOD-123	MMSZ5242C-E3-08	Vishay
70	1	VR103	Diode ZENER 11V 500 mW SOD123	MMSZ5241B-7-F	Diodes, Inc.

6.1.2 Active Bridge Board

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR200	Diode BRIDGE 600V 4A GB	GBL06	Genesic Semi
2	1	C200	2.2 µF, ±10%, 25V, X7R, r, -55°C ~ 125°C, 0805	CL21B225KAFVPNE	Samsung
3	2	Q200 Q201	MOSFET, N-Channel, 600 V, 40A (Ta), 270W (Tc), Surface Mount TOLL, 8-PowerSFN	TK055U60Z1,RQ	Toshiba
4	2	R200 R201	RES, 100.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1003X	Panasonic
5	1	U200	IC, ACTIVE BRIDGE CTRL, SO8, 8-SOIC (0.154", 3.90mm Width), 8SOIC	TEA2206T/1J	NXP

6.1.3 USB PD Board

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	C300	1 µF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
2	1	C301	1 µF, ±10%, 35 V, Ceramic, X7R, 0603	CGA3E1X7R1V105K080AE	TDK
3	1	C302	2.2 µF, ±10%, 25 V, Ceramic, X7R, 0603, -55 to 125 °C	GRM188Z71E225KE43D	Murata
4	1	C303	1000 pF, ±10%, 50 V, X7R, -55°C ~ 125°C, Low ESL, 0402	C0402C102K5RACTU	Kemet
5	2	C304 C305	330 pF, ±10%, 25 V, Ceramic Capacitor, X7R, 0402	04023C331KAT2A	AVX
6	1	D300	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
7	1	Q300	MOSFET, N-CH, 40 V, 37 A (Ta), 100 A (Tc) 2.5 W (Ta), 139 W (Tc), SMD, PG-TSDSON-8 FL	BSC010N04LSIATMA1	Infineon
8	1	R300	RES, 1 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1001V	Panasonic
9	2	R301 R310	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ102X	Panasonic
10	1	R302	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
11	2	R303 R308	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
12	2	R304 R306	RES, 0 Ω, 1/16 W, Thick Film, 0402	CRCW04020000Z0ED	Vishay
13	2	R305 R307	RES, 3 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ3R0X	Panasonic
14	1	R309	RES, 5.1 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ512X	Panasonic
15	1	R311	RES, 5 mΩ, ±1%, 1 W, Chip Resistor 1206, Pulse Withstanding Thick Film	CRF1206-FZ-R005ELF	Bourns
16	1	RT300	NTC Thermistor, 100 kΩ, 1%, 0603	NTCG164KF104FT1S	TDK
17	4	TVS300-TVS303	Bidirectional TVS Diode, Voltage - Reverse Standoff (Typ) 24 Vmax, 42 V Clamp, 7 A (8/20µs) Ipp, SMT,SC-76, SOD-323	SD24C-01FTG	Littelfuse
18	1	U301	IC, Fast Charging Controller IC for USB Interfaces, 24QFN	IP2756	INJOINIC

6.2 Mechanical

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	J100	Power Entry Connector Receptacle, Male Pins, IEC 320-C8, Non-Polarized, Panel Mount, Snap-In; Through Hole, Right Angle	RAPC322X	Switchcraft
2	1	J300	Connector, USB TYPE C, R/A, Receptacle	12402143E512A	Amphenol

7 Flyback Transformer (T101) Specification

7.1 Electrical Diagram

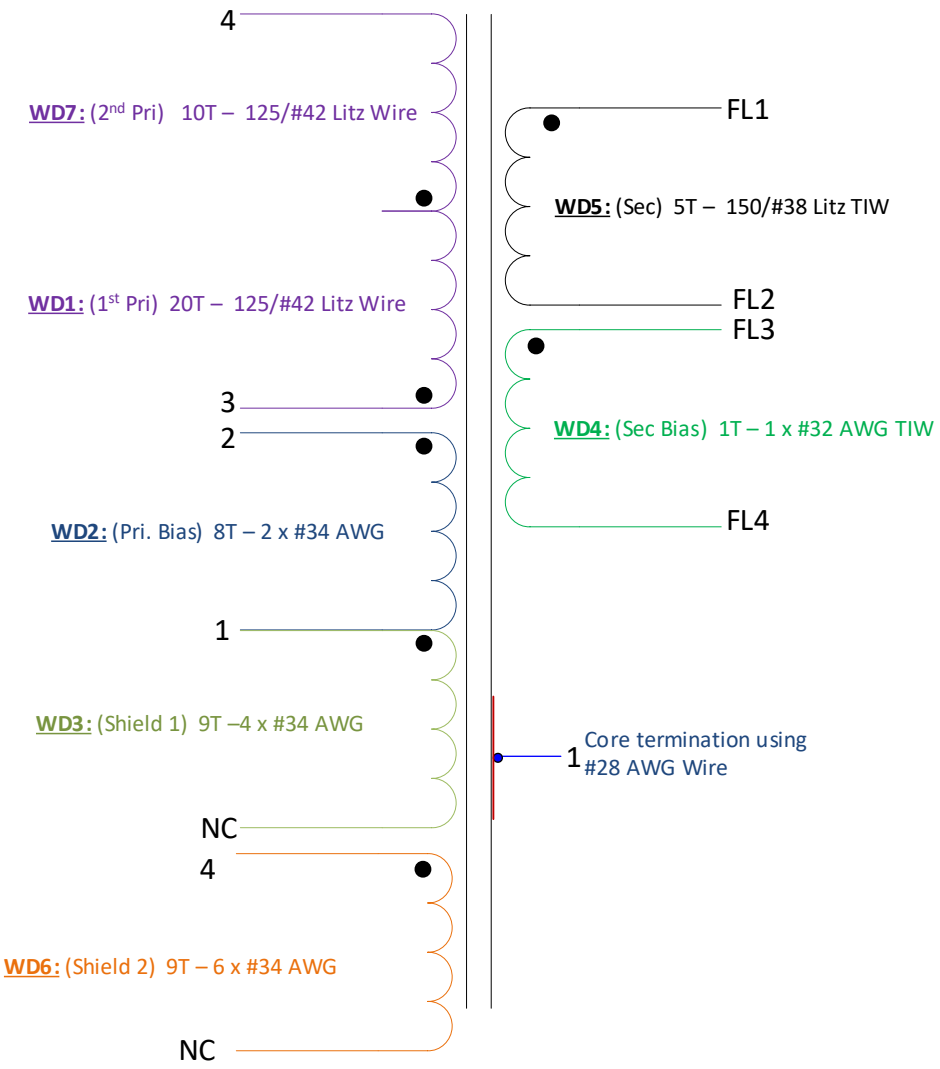


Figure 19 – Flyback Transformer (T101) Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 3 and 4, with all other windings open.	280 µH ±5%
Primary Leakage Inductance	Between pin 3 and 4, with pins: FL1-FL2 shorted.	5.9 µH (Max.)
Primary DC Resistance	Between pin 3 and 4.	80 mΩ ±5%

7.3 Material List

Item	Description
[1]	Core: ATQ27/18 P/N: 99-00079-00.
[2]	Bobbin: Bobbin, ATQ27/18, Vertical, 4 pins. P/N: 25-01178-00.
[3]	Magnet Wire: Served Litz 125 / #42.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	TIW Magnet Wire: #32 AWG, Triple Insulated Wire.
[6]	TIW Litz Wire: 150 / #38, Triple Insulated Wire.
[7]	Bus Wire: #30 AWG, Alpha Wire, Tinned Copper.
[8]	Copper Foil, 2 mil Thickness, 0.75 in Width.
[9]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 11 mm Width.
[10]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 19.5 mm Width.
[11]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 22 mm Width.
[12]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 40 mm width
[13]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

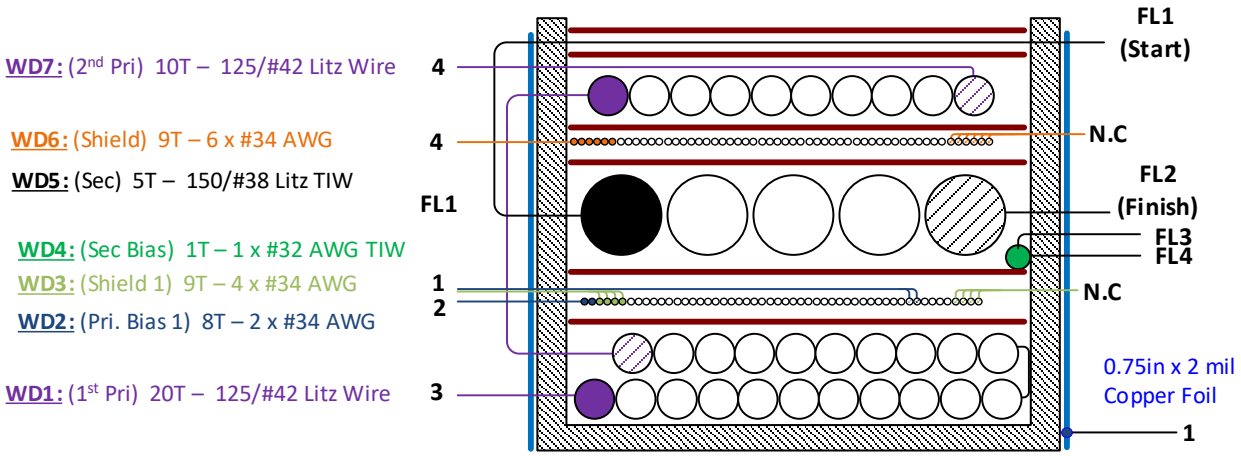
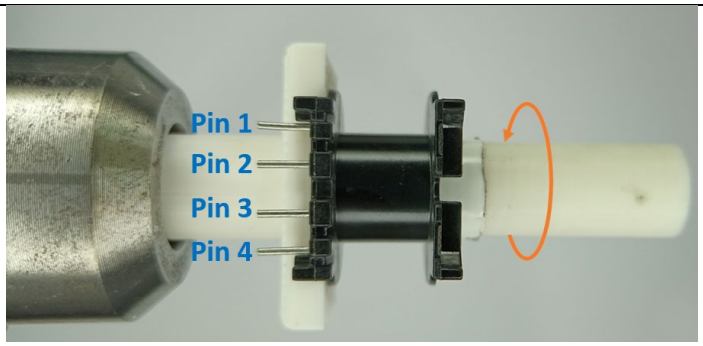


Figure 20 – Flyback Transformer (T7) Build Diagram.

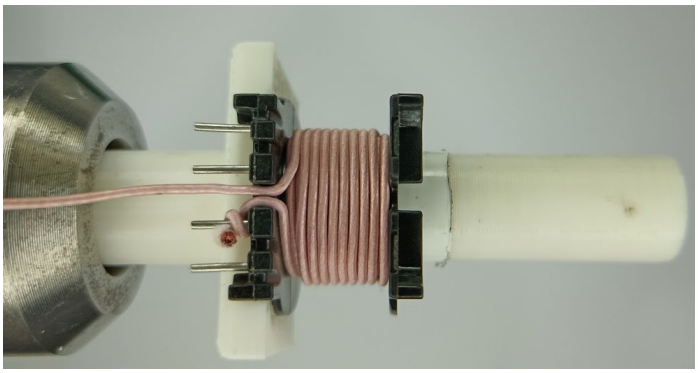
7.5 Transformer Winding Instruction

Note: Please follow below transformer build illustration to prevent shorting of wires from 2 adjacent terminals.

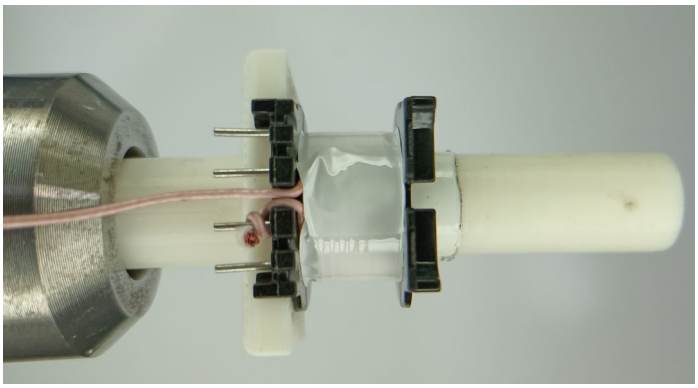
Winding Direction
Use ATQ27/18.4 Bobbin (Item 2). Position the bobbin on the winding jig such that the primary side of the bobbin is on the left side with the primary terminal pins facing upward. The winding direction is clock-wise.



Winding 1 (1st Primary)
Prepare 185cm of 125/#42 Litz wire (Item 3). Start on pin 3 and wind 10 turns to the right and 10 turns back to the left side.
Set aside the remaining wires on the left side and fix it with tape

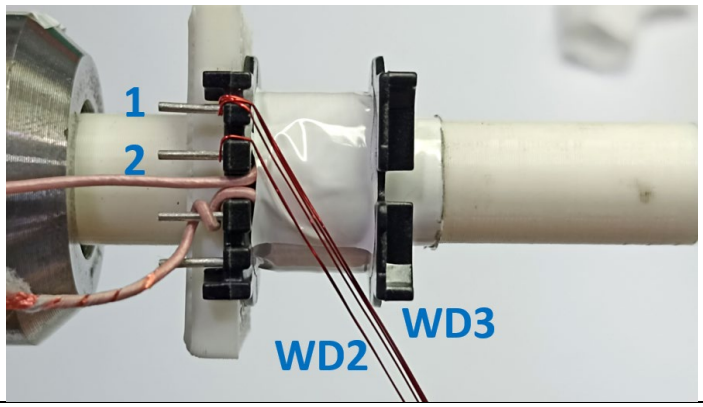


Tape Insulation
Apply 1 layer of 11mm polyester tape (Item 9) for insulation.

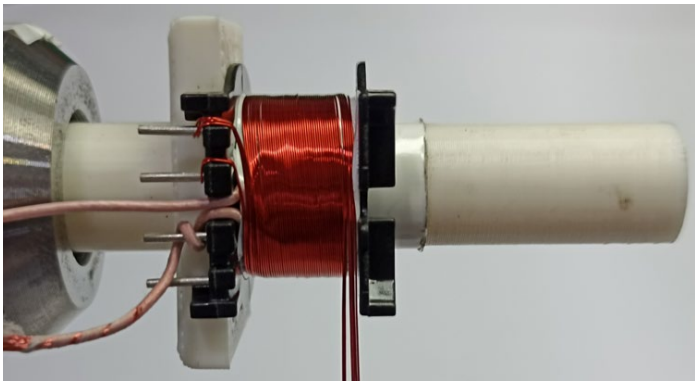


WD2 & WD3: Primary Bias and Shield 1
Prepare 65cm of 6 x AWG#34 (Item 4).

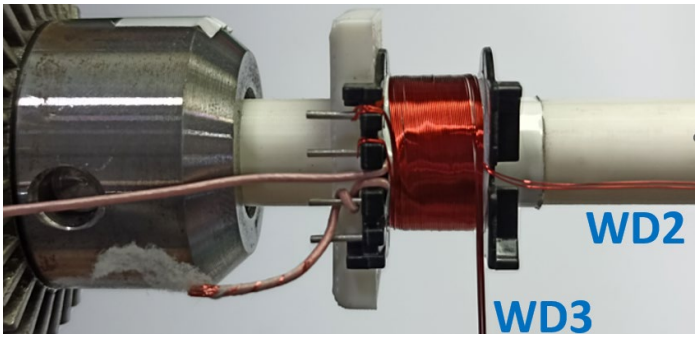
Start WD3 at pin 1 with 4 strands
Start WD2 at pin 2 with 2 strands. Mark the end of WD2 to avoid confusion.
Use the same slots used in the image to avoid shorts during soldering.



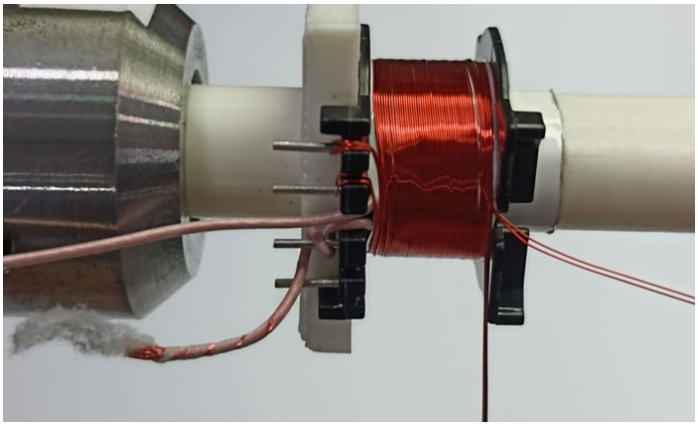
Wind all the wires together for 8 turns.



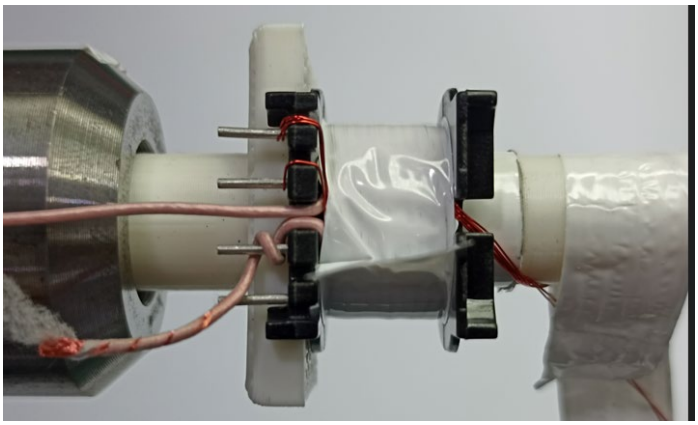
Exit WD2 to the right slot by passing it under WD3 and secure it by tape on the right side..



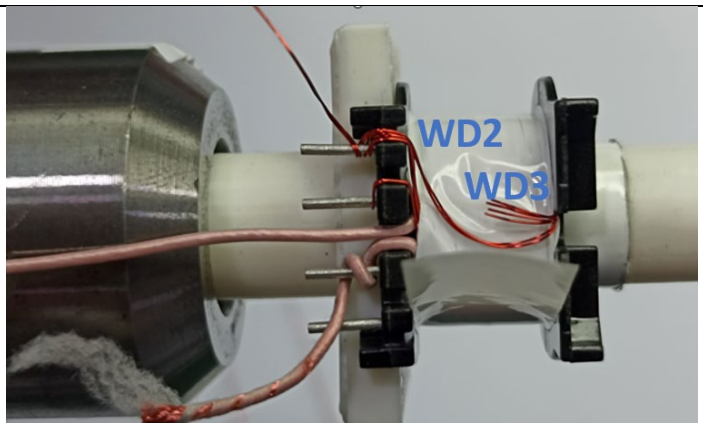
Wind the remaining 1 turn for WD3



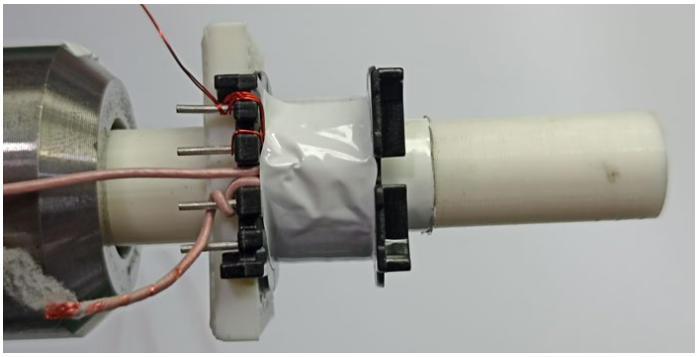
Apply 1 layer of 11mm tape and leave enough to cover the wire going back to the pin side.



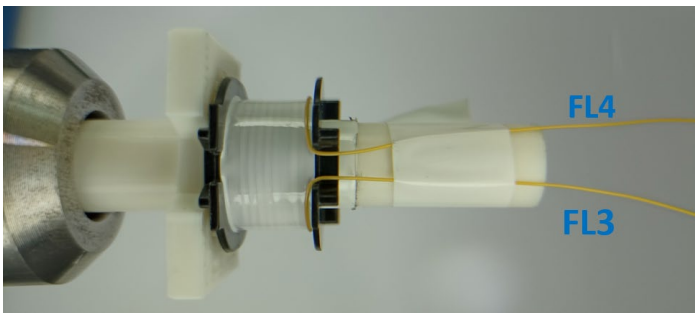
Terminate WD2 to pin 1.
Cut WD3 and leave it floating.
Make sure to use the same slot in the image for the WD2 termination to avoid shorts during soldering.



Wrap the tape to cover WD2 and WD3.

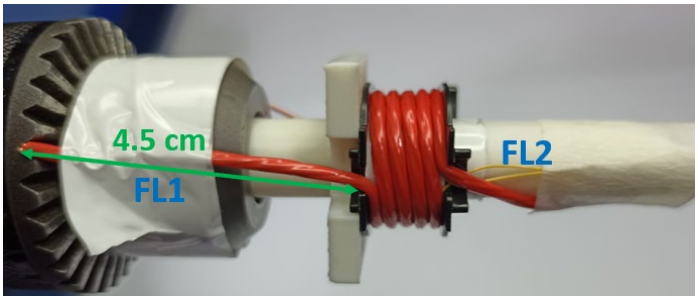


WD3: Secondary Bias Winding
Prepare 15cm AWG#32 Triple Insulated Wire (Item 5).
Wind 1 turn and secure the fly leads with tape.
Mark the wires according to the picture on the right.



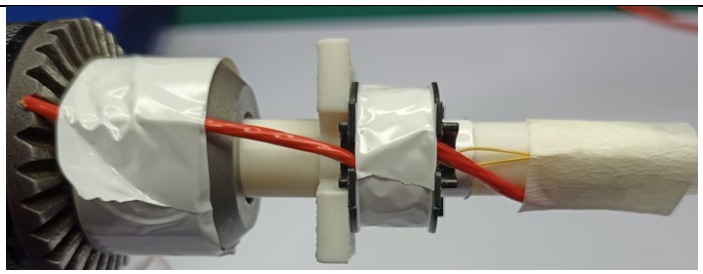
WD4: Secondary Winding
Position the bobbin such that the secondary wire slot is facing upward.
Prepare 39.5 cm of 150x#38 Triple Insulated Litz wire (Item 6) and bend it by 90° at 4.5cm. Place the corner of the bend on the slot and use tape to hold the wire in place.

Wind 5 turns to the right and secure it with tape.



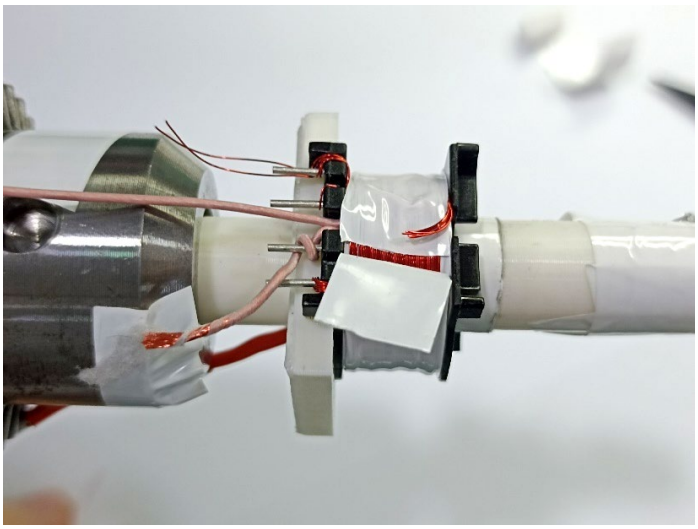
Tape Insulation

Apply 1 layer of 11mm polyester tape (Item 11).



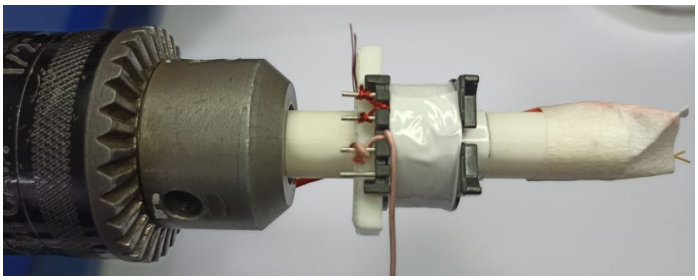
WD5: Shield Winding

Prepare 6 strands AWG#34 magnet wire (Item 4). Start at Pin 4 and evenly wind 9 turns and exit the winding through the slot on the right.
Wrap 1 layer of tape (Item 9). Cut the wires and leave it floating as shown. Finish wrapping the tape to cover the winding end.

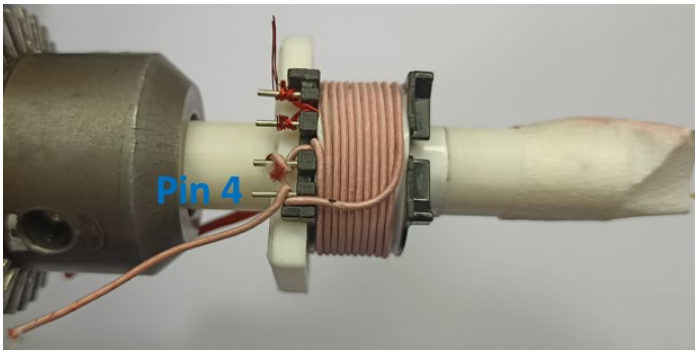


Winding 6 (2nd Primary)

Use the wire that was set aside from WD1.

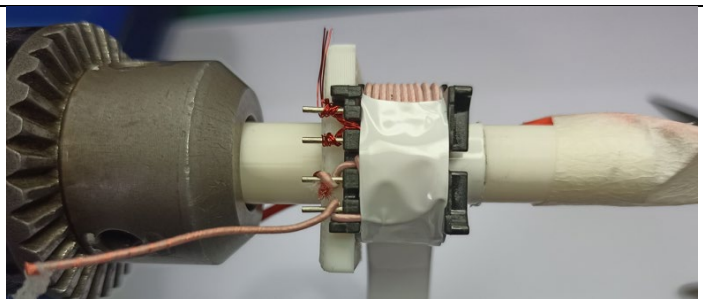


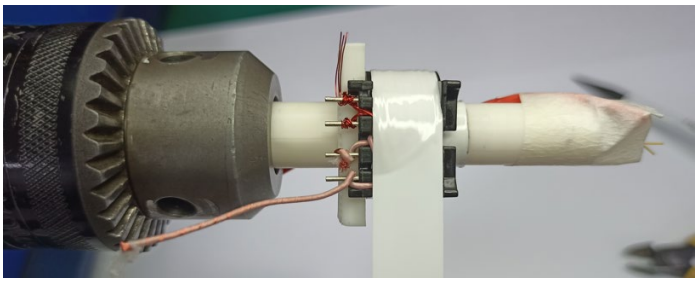
Wind 10 turns to the right and terminate the winding at Pin 4.



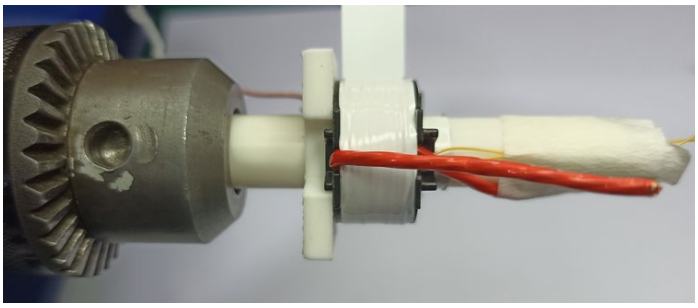
Tape Insulation

Apply 1-layer of 11mm polyester tape (Item 9) for insulation. Do not cut the tape yet.

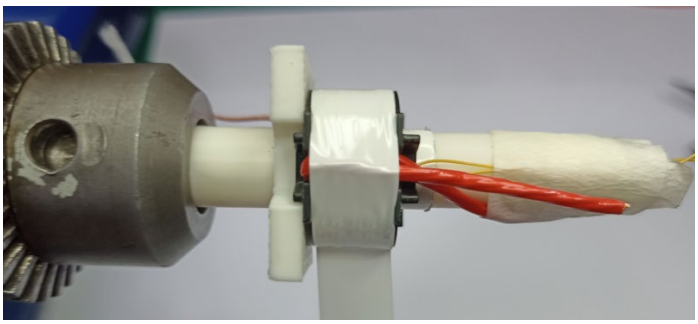




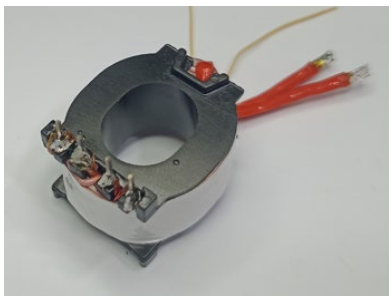
Secondary Termination fold
Fold the secondary winding start FL1 so that it is on the same side as FL2.



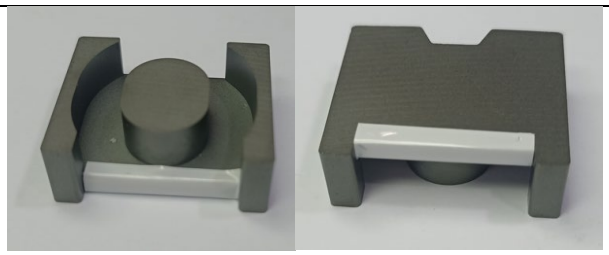
Wrap it with the tape to secure.



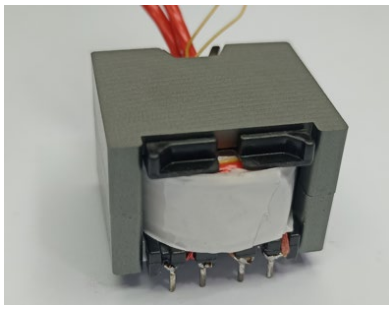
Solder the wires to the pins



Prepare the lower core half by placing an 8mm strip of 19.5 mm tape (Item 10) on the part shown on the right. This prevents the wires soldered on the pins of the transformer from touching the core.

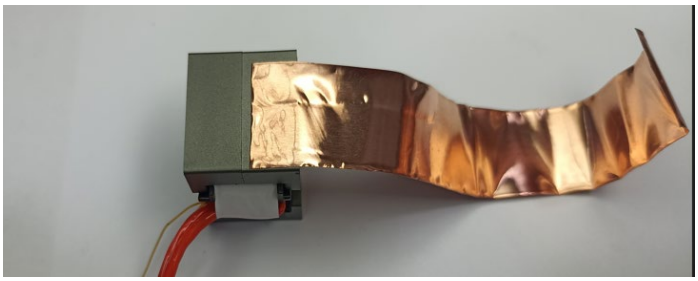


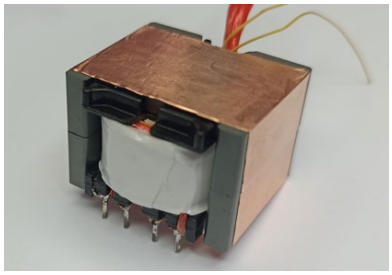
Magnetizing Inductance
Grind the center leg of the ferrite core evenly to meet the required inductance



Add Core Grounding

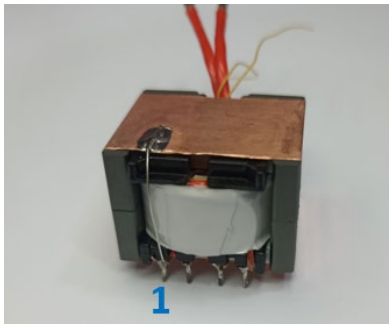
Wrap a 9cm strip of 0.75 in copper tape(Item 8) around the core.





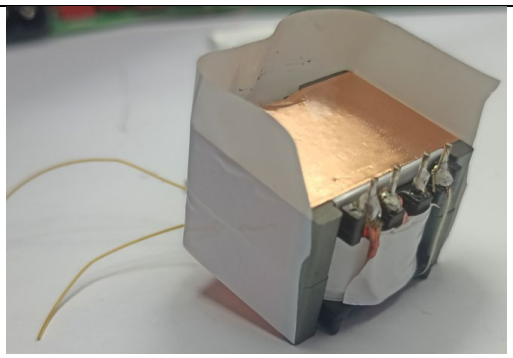
Core Grounding Connection

Connect the copper foil to Pin 1 by soldering a 3cm length AWG #28 wire (Item 7).

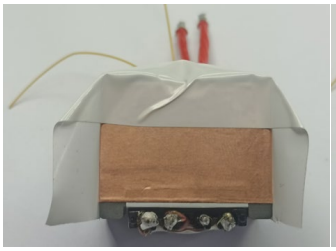


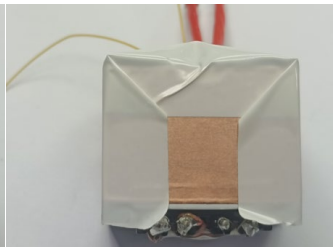
Tape Insulation

Apply 28mm tape (Item 12) to the sides and back of the transformer.

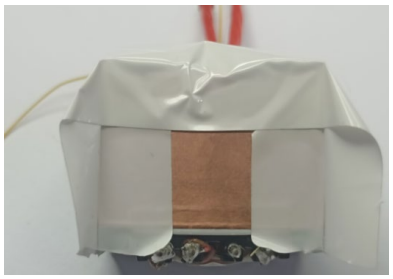


Fold the tape as shown in the right.

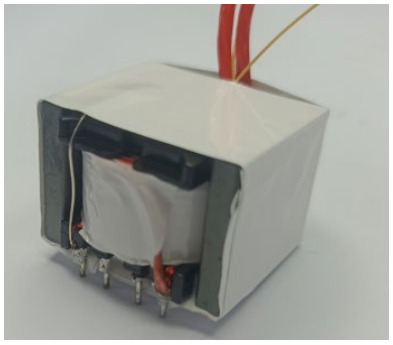




Apply another layer of tape with the same steps to reinforce the isolation.



Apply 2 layers of 22 mm tape (Item 11) around the top, sides and bottom of the transformer to secure the previously applied tape and also to lock the cores in place.



Transformer Varnishing

Dip the whole transformer in a pure varnish solution (Item 13) for 10 minutes. Cure the varnished transformer in hot (100^0C) oven for 1 hr.

8 Common Mode Choke (L100) Specification

8.1 Electrical Diagram

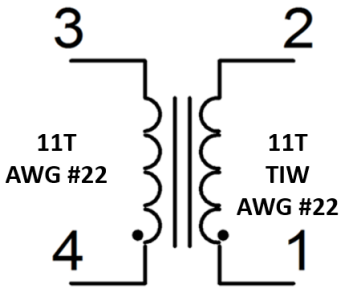


Figure 21 – CMC Electrical Diagram.

8.2 Electrical Specifications

Winding Inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 and pin 2 or pin 3 and pin 4 with all other windings open.	360 µH ±20%

8.3 Material List

Item	Description
[1]	Toroid Core: 32-00315-00 (Green Color).
[2]	Magnet Wire: #22 AWG.
[3]	TIW Wire: #22 AWG.

8.4 Assembled Picture

Figure 22 – CMC Assembled Photo.

8.5 Inductor Construction

1. Winding 1 - Wind 11 turns of item 2 and 3 in bifilar wound as shown in above figure.

9 Common Mode Choke (L101) Specification

9.1 Electrical Diagram

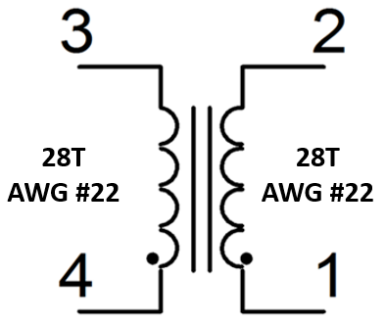


Figure 23 – CMC Electrical Diagram.

9.2 Electrical Specifications

Winding Inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 and pin 2 or pin 3 and pin 4 with all other windings open.	5.6 H ±20%

9.3 Material List

Item	Description
[1]	Toroid Core: 32-00343-00 (Green Color).
[2]	Spacer 1mm x 9.7mm x 6 mm.
[3]	Magnet Wire: #22 AWG.

9.4 Assembled Picture

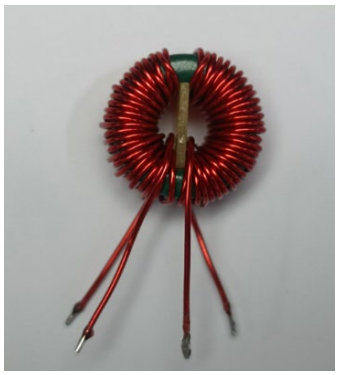


Figure 24 – CMC Assembled Photo.

9.5 Inductor Construction

1. Place the spacer inside the core to separate the winding areas for each winding.
2. Prepare 2 strands of 80 cm #22 AWG magnet wire (Item 3)
3. Wind 28 turns of #22 AWG for each winding

10 Boost Inductor (T100) Specification

10.1 Electrical Diagram

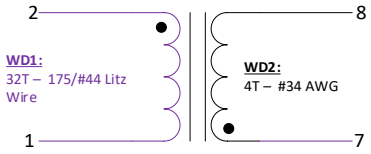


Figure 25 – Boost Inductor (T8) Electrical Diagram.

10.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and 2, with all other windings open.	175 µH ±5%
Resonant Frequency	Between pin 1 and 2, other windings open.	100 kHz (Min.)
Primary DC Resistance	Between pin 1 and 2.	85 mΩ

10.3 Material List

Item	Description
[1]	Core: ATQ25 PC95, P/N: 99-00069-00.
[2]	Bobbin: ATQ25-16, P/N: 25-01167-00.
[3]	Magnet Wire: Served Litz 175 / #44.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Copper Tape, 3 mm.
[6]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 8.5 mm Width.
[7]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 14 mm Width.
[8]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 18 mm Width.
[9]	Varnish: Dolph BC-359.

10.4 Boost Inductor Build Diagram

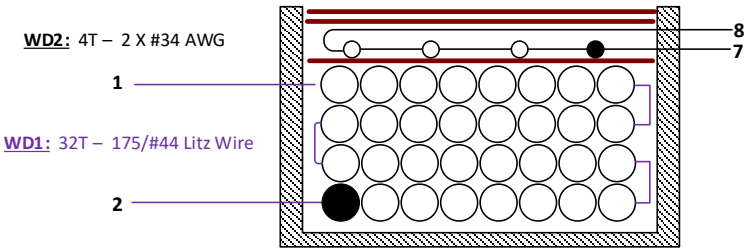
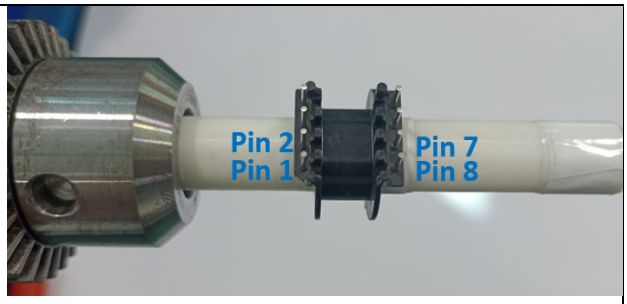


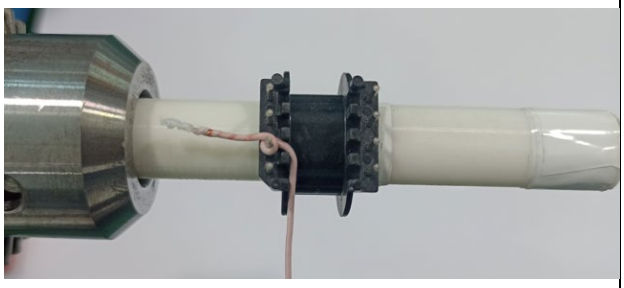
Figure 26 – Boost Inductor Build Diagram.

10.5 Boost Inductor Winding Instructions

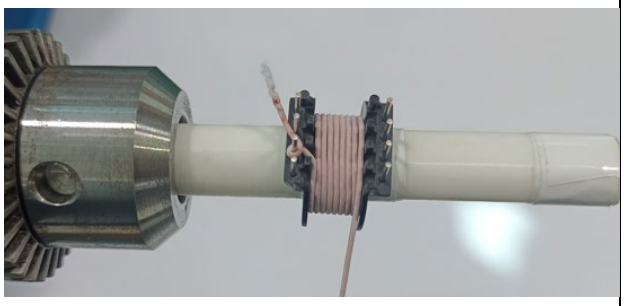
Winding Directions
Bobbin is positioned on winder jig such that terminal Pin 1- 4 are in the left side facing upward. The inductor winding direction is clockwise.



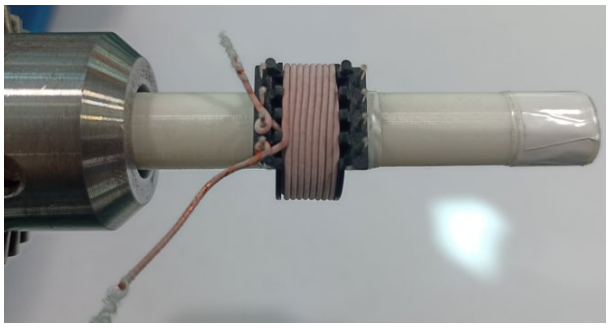
Winding 1
Prepare 170 cm of Served Litz wire 175/#42 (Item 3).
Start at Pin 2 and wind 32 turns evenly.



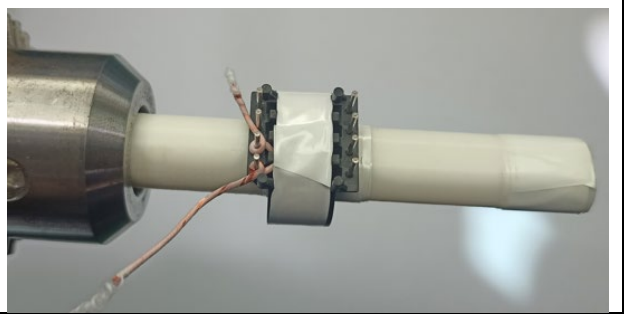
8 turns can fit for every winding layer.



At the end of 32 turns, terminate the winding at pin 1.

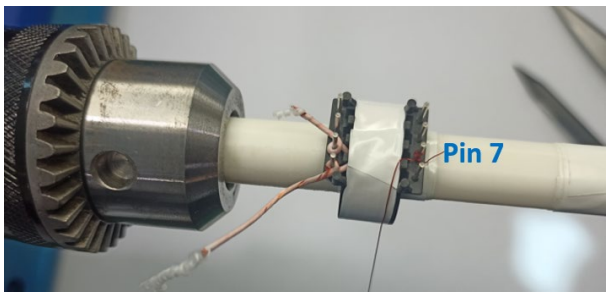


Wrap 1 layer of 8.5mm tape (Item 6)

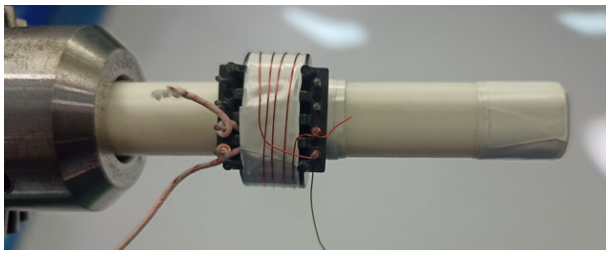


Winding 2

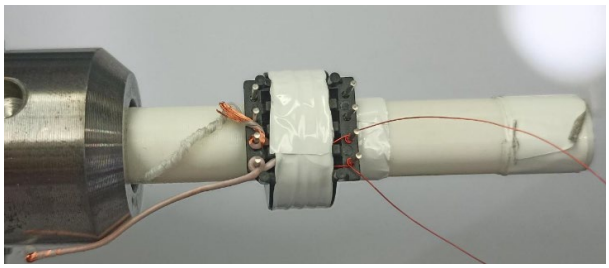
Prepare 35 cm of #34 AWG wire (Item x) and start the winding at pin 7.



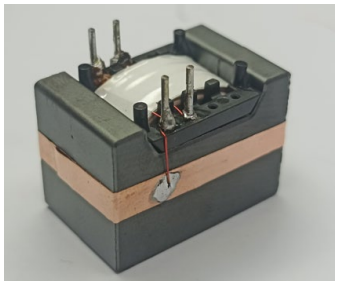
Wind 4 turns and terminate the winding at pin 8.



Wrap 2 layers of 8.5mm tape to secure the winding.



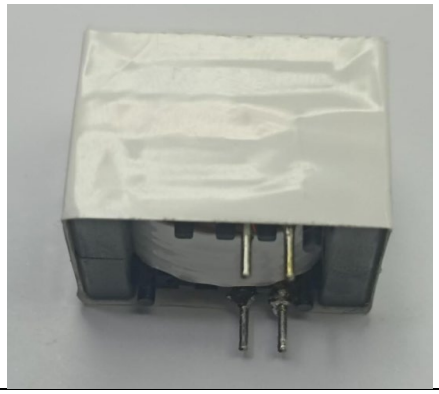
Solder the wires to the bobbin pins.



Inductance
Grind the center leg of the top ferrite core evenly until it matches the required inductance.

Core Grounding
Wrap a 3mm copper tape (Item 5) around the core and connect it to Pin 8 using a wire.

Insulating Tape
Wrap an 18 mm (Item 8) tape around the top and sides of the choke as shown. This tape insulates from the heatsink beside the choke.

Fold the tape as shown on the right.	
Core Fixing and Varnishing Apply 14 mm polyester tape (Item 7) to fix the top and bottom core. Dip the transformer in varnish (Item 9). Cure the varnished inductor into 100 ^{0}C hot oven for 30 mins	

11 InnoSwitch5-Pro Design Spreadsheet

1	ACDC_InnoSwitch5-Pro_Flyback_012524 ; Rev.1.0; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch5-Pro Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	DC		DC		Input Type
4	VIN_MIN	255		255	V	Minimum DC input voltage
5	VIN_MAX	385		385	V	Maximum DC input voltage
6	VIN_RANGE			PFC INPUT		Input voltage range
7	FLINE				Hz	AC Input voltage frequency
8	CAP_INPUT				uF	Input capacitance
10	**SET-POINT 1**					
11	VOUT1	28.000		28.000	V	Output voltage; should be the highest output voltage required
12	CDC1	0.000		0.000	V	Cable-drop compensation required
13	IOUT1	5.000		5.000	A	Output current
14	POUT1			140.00	W	Output power
15	EFFICIENCY1	0.96		0.96		Estimated converter efficiency
16	Z_FACTOR1	0.60		0.60		Estimated Z-factor
17	TYPE	PDO	Info	PDO		The voltage entered is not a standard PDO(Power Delivery Object)
19	**SET-POINT 2**					
20	VOUT2	20.000		20.000	V	Output voltage
21	CDC2	0.000		0.000	V	Cable-drop compensation required
22	IOUT2	5.000		5.000	A	Output current
23	POUT2			100.00	W	Output power
24	EFFICIENCY2	0.96		0.96		Estimated converter efficiency
25	Z_FACTOR2	0.60		0.60		Estimated Z-factor
26	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
28	**SET-POINT 3**					
29	VOUT3	15.000		15.000	V	Output voltage
30	CDC3	0.000		0.000	V	Cable-drop compensation required
31	IOUT3	5.000		5.000	A	Output current
32	POUT3			75.00	W	Output power
33	EFFICIENCY3	0.91		0.91		Estimated converter efficiency
34	Z_FACTOR3	0.60		0.60		Estimated Z-factor
35	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
37	**SET-POINT 4**					
38	VOUT4	9.000		9.000	V	Output voltage
39	CDC4	0.000		0.000	V	Cable-drop compensation required
40	IOUT4	3.000		3.000	A	Output current
41	POUT4			27.00	W	Output power
42	EFFICIENCY4	0.90		0.90		Estimated converter efficiency
43	Z_FACTOR4	0.60		0.60		Estimated Z-factor
44	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
46	**SET-POINT 5**					
47	VOUT5	5.000		5.000	V	Output voltage
48	CDC5	0.000		0.000	V	Cable-drop compensation required
49	IOUT5	3.000		3.000	A	Output current
50	POUT5			15.00	W	Output power
51	EFFICIENCY5	0.89		0.89		Estimated converter efficiency
52	Z_FACTOR5	0.60		0.60		Estimated Z-factor

53	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
92	**PRIMARY CONTROLLER SELECTION**					
93	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
94	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
95	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
96	DEVICE_GENERIC	INN5377-H905	Info	INN5377-H905		The INN53xx series is optimized for universal AC designs. The INN54xx series is optimized for peak power designs with PFC input. Please verify thermal performance on the bench
97	DEVICE_CODE			INN5377F-H905		Device code
98	PDEVICE_MAX			145	W	Device maximum power capability
99	RDSON_100DEG			0.29	Ω	Primary switch on-time resistance at 100°C
100	ILIMIT_MIN			2.990	A	Primary switch minimum current limit
101	ILIMIT_TYP			3.250	A	Primary switch typical current limit
102	ILIMIT_MAX			3.510	A	Primary switch maximum current limit
103	VDRAIN_ON_PRSW			0.16	V	Primary switch on-time voltage drop
104	VDRAIN_OFF_PRSW		Warning	666.5	V	The peak drain voltage on the primary switch is higher than 650V: Decrease the device VOR
108	**WORST CASE ELECTRICAL PARAMETERS**					
109	FSWITCHING_MAX	117262	Info	117262	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
110	VOR	168.0		168.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
111	VMIN			255.00	V	Minimum DC input voltage at full load
112	KP			1.109		Measure of continuous/discontinuous mode of operation
113	MODE_OPERATION			DCM		Mode of operation
114	DUTYCYCLE			0.373		Primary switch duty cycle
115	TIME_ON			3.83	us	Primary switch on-time
116	TIME_OFF			5.36	us	Primary switch off-time
117	LPRIMARY_MIN			266.0	uH	Minimum primary magnetizing inductance
118	LPRIMARY_TYP			274.3	uH	Typical primary magnetizing inductance
119	LPRIMARY_TOL	3.0		3.0	%	Primary magnetizing inductance tolerance
120	LPRIMARY_MAX			282.5	uH	Maximum primary magnetizing inductance
122	**PRIMARY CURRENT**					
123	IAVG_PRIMARY			0.563	A	Primary switch average current
124	IPEAK_PRIMARY			3.472	A	Primary switch peak current
125	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
126	IRIPPLE_PRIMARY			3.472	A	Primary switch ripple current
127	IRMS_PRIMARY			1.142	A	Primary switch RMS current
129	**SECONDARY CURRENT**					
130	IPEAK_SECONDARY			20.831	A	Secondary winding peak current
131	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
132	IRMS_SECONDARY			8.436	A	Secondary winding RMS current
133	IRIPPLE_CAP_OUT			6.795	A	Output capacitor ripple current
137	**TRANSFORMER CONSTRUCTION PARAMETERS**					
138	**CORE SELECTION**					
139	CORE	ATQ27		ATQ27		Core selection. Refer to the "Transformer Construction" tab for the detailed report.
140	CORE NAME			ATQ27/18.4		Core code
141	AE			129.0	mm^2	Core cross sectional area
142	LE			51.0	mm	Core magnetic path length

143	AL			6200	nH	Ungapped core effective inductance per turns squared
144	VE			6579	mm^3	Core volume
145	BOBBIN NAME			ATQ27/18.4 - 1 (P2-S2)		Bobbin name
146	AW			56.2	mm^2	Bobbin window area
147	BW			10.40	mm	Bobbin width
148	MARGIN			0.0	mm	Bobbin safety margin
150	**PRIMARY WINDING**					
151	NPRIMARY			30		Primary winding number of turns
152	BPEAK			2672	Gauss	Peak flux density
153	BMAX			2521	Gauss	Maximum flux density
154	BAC			1260	Gauss	AC flux density (0.5 x Peak to Peak)
155	ALG			305	nH	Typical gapped core effective inductance per turns squared
156	LG			0.506	mm	Core gap length
158	**PRIMARY BIAS WINDING**					
159	NBIAS_PRIMARY			8		Primary bias winding number of turns
161	**SECONDARY WINDING**					
162	NSECONDARY	5		5		Secondary winding number of turns
164	**SECONDARY BIAS WINDING**					
165	NBIAS_SECONDARY			2		Secondary bias winding number of turns
168	**PRIMARY COMPONENTS SELECTION**					
169	RCD CLAMP					
170	LLEAK	5.40		5.40	uH	Primary winding leakage inductance
171	CSWNODE			15.00	pF	Primary switching node capacitance (InnoSwitch Coss + Transformer lumped winding capacitance)
172	CCLAMP			3.40	nF	Primary clamp capacitor
173	RCLAMP			25.09	kΩ	Primary Clamp Resistor
175	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
176	BROWN-IN REQURED	113.00		113.00	V	Required AC RMS/DC line brown-in threshold
177	RLS			4.10	MΩ	Connect two 2.05 MOhm resistors to the V-pin for the required UV/OV threshold
178	BROWN-IN ACTUAL			94.4V - 114.5V	V	Actual AC RMS/DC brown-in threshold using standard resistors
179	BROWN-OUT ACTUAL			83.9V - 104.2V	V	Actual AC RMS/DC brown-out threshold using standard resistors
180	OVERVOLTAGE_LINE		Warning	430.9V - 489.3V	V	The device voltage stress (770.8V) will be higher than 750V when overvoltage is trigerred
182	**PRIMARY BIAS WINDING**					
183	VBIAS_PRIMARY	7.00	Info	7.00	V	The rectified primary bias voltage maybe too low to supply the BPP pin: Increase the rectified primary bias voltage to a value higher than 9V
184	VF_BIAS_PRIMARY	0.70		0.70	V	Primary bias winding diode forward drop
185	VREVERSE_BIASDIODE_ PRIMARY			147.47	V	Primary bias diode reverse voltage (not accounting parasitic voltage ring)
186	CBIAS_PRIMARY			22	uF	Primary bias winding rectification capacitor
187	CBPP			4.70	uF	BPP pin capacitor
191	**SECONDARY COMPONENTS SELECTION**					
192	**RECTIFIER**					
193	VDRAIN_OFF_SRFET			92.17	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
194	SRFET	AONS62922		AONS62922		Secondary rectifier (Logic MOSFET)
195	VBREAKDOWN_SRFET			120	V	Secondary rectifier breakdown voltage
196	RDSON_SRFET			7.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
198	**SECONDARY BIAS WINDING**					
199	USE_SECONDARYBIAS	AUTO		YES		Select to use secondary bias winding or not
200	VBIAS_SECONDARY			6.00	V	Rectified secondary bias voltage at full load

201	VF_BIAS_SECONDARY			0.70	V	Secondary bias winding diode forward drop
202	VREVERSE_BIASDIODE_ SECONDARY			31.67	V	Secondary bias diode reverse voltage (not accounting parasitic voltage ring)
203	CBIAS_SECONDARY			2.20	uF	Secondary bias winding rectification capacitor
204	CBPS			2.20	uF	BPS pin capacitor
206	**SYNCHRONOUS RECTIFIER ZERO-VOLTAGE SWITCHING TIMING**					
207	SRZVS_ENABLE	YES		YES		Enable/Disable SRZVS operation
208	TIME_SRZVS_ON	425		425	ns	Output rectifier on time during SR-ZVS operation
209	IP_SRZVS_ON			1.56	A	Secondary switch peak current after SR-ZVS on-time
210	TIME_SRZVS_DELAY	510		510	ns	Output rectifier delay time during SR-ZVS operation
211	VDS_SRZVS_DELAY			0.0	V	Primary switch drain voltage at the end of SRZVS delay

12 HiperPFS-5 Design Spreadsheet

12.1 High Line

1	Hiper_PFS-5_Boost_051923; Rev.1.2; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	Discontinuous Mode Boost Converter Design Spreadsheet
2	**Enter Application Variables**					
3	Input Voltage Range	Universal		Universal		Input voltage range
4	VACMIN	170		170	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX	265		265	VAC	Maximum AC input voltage
6	VBROWNIN		Info	82	VAC	Brown-IN voltage has been modified since the V-pin ratio is no longer 100:1
7	VBROWNOUT		Info	71	VAC	Brown-OUT voltage has been modified since the V-pin ratio is no longer 100:1
8	VO	380	Info	380	VDC	Brown IN/OUT voltage has changed due to modifications in the V-pin ratio from 100:1. Recommend Vpin ratio= FB pin ratio for optimized operation. Check the PF, input current distortion, brown in/out and power delivery
9	PO	145		145	W	Nominal Output power
10	fL			50	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	Efficiency Estimate			0.9500		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			361	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX	15		15	VDC	Maximum Output voltage ripple
15	T_HOLDUP			20	ms	Holdup time
16	VHOLDUP_MIN			304	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	Yes		Yes		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
20	**KP and INDUCTANCE**					
21	LPFC_MIN (0 bias)			169	uH	Minimum PFC inductance value
22	LPFC_TYP (0 bias)	175		175	uH	LPFC value used for calculations. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation.
23	LPFC_MAX (0 bias)			180	uH	Maximum PFC inductance value
24	LP_TOL	3.0		3.0	%	Tolerance of PFC Inductor Value (ferrite only)
25	LPFC_PEAK			175	uH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
26	KP_ACTUAL			1.32		Actual KP calculated from LPFC_DESIRED
28	**Basic Current Parameters**					
29	IAC_RMS			0.90	A	AC input RMS current at VACMIN and Full Power load
30	IL_RMS			1.57	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
31	IO_DC			0.38	A	Output average current/Average diode current
34	**PFS Parameters**					
35	PFS Package			F		HiperPFS package selection

36	PFS Part Number	PFS5277F		PFS5277F		If examining brownout operation, over-ride autopick with desired device size
37	Self-Supply Feature	No		No		Device self-supply feature. Select "Yes" to select device with self-supply feature or "No" for device without self-supply
38	PS_FACTOR	0.8		0.8		Programmable output power selection factor
39	PO_MAX_DEV			148	W	Maximum output power of the device
40	IOCP min			6.06	A	Minimum Current limit
41	IOCP typ			4.20	A	Typical current limit
42	IOCP max			7.04	A	Maximum current limit
43	IP			3.87	A	MOSFET peak current
44	IRMS			1.12	A	PFS MOSFET RMS current
45	RDSON			0.29	Ohms	Typical RDSon at 100 'C
46	FS_PK			135.0	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
47	FS_AVG			120.3	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
48	PCOND_LOSS_PFS			0.366	W	Estimated PFS Switch conduction losses
49	PSW_LOSS_PFS			0.107	W	Estimated PFS Switch switching losses
50	PFS_TOTAL			0.473	W	Total Estimated PFS Switch losses
51	TJ Max			100	deg C	Maximum steady-state junction temperature
52	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
53	HEATSINK Theta-CA			124.10	°C/W	Maximum thermal resistance of heatsink
56	**INDUCTOR DESIGN**					
57	**Material and Dimensions**					
58	Core Type			Ferrite		Ferrite core
59	Core Material	Auto		PC44/PC95		Select the core material
60	Core Geometry	ATQ		ATQ		Select the core geometry
61	Core	ATQ25/16		ATQ25/16		Core part number
62	Ae			102.00	mm^2	Core cross sectional area
63	Le			40.80	mm	Core mean path length
64	AL			6700.00	nH/t^2	Core AL value
65	Ve			4.16	cm^3	Core volume
66	HT (EE/PQ/EQ/RM/POT) / ID (toroid)			3.20	mm	Core height/Height of window; ID if toroid
67	MLT			48.8	mm	Mean length per turn
68	BW			8.00	mm	Bobbin width
69	LG			0.72	mm	Gap length (Ferrite cores only)
70	**Flux and MMF Calculations**					
71	BP_TARGET (ferrite only)	3900		3900	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
72	B_OCP (or BP)			3888	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
73	B_MAX			2075	Gauss	Peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance,minimum IOCP
77	I_TEST			4.2	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
78	B_TEST			2319	Gauss	Flux density at I_TEST and maximum tolerance inductance
80	**Wire**					
81	TURNS			32		Inductor turns. To adjust turns, change the BP_TARGET
82	ILRMS			1.57	A	Inductor RMS current
83	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire
84	AWG	44		44	AWG	Inductor wire gauge

85	Filar	175		175		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
86	OD (per strand)			0.051	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			0.94	mm	Will be different than OD if Litz
88	DCR			0.097	ohm	Choke DC Resistance
89	P AC Resistance Ratio			0.48		Ratio of total copper loss, including HF AC, to the DC component of the loss
90	J		Info	4.41	A/mm^2	Current density is low. If copper loss is low, you can use thinner wire or fewer strands
91	Layers			3.98		Estimated layers in winding
92	**Auxiliary Winding**					
93	N_AUX	4		4		Recommended auxiliary winding number of turns to ensure the supply to the VS pin
94	V_VS_MAX		Warning	-0.28	V	The maximum voltage across thhe auxiliary winding is less than the threshold voltage of the VS pin (0.88 V). Increase N_AUX.
95	V_VS_MIN			-46.85	V	Minimum voltage across the auxiliary winding
96	RVS			10.00	kohm	Recommended series resistor to the VS pin. Place as close as possible to the VS pin of Hiper-PFS5
97	**Loss Calculations**					
98	BAC-p-p			2568	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
99	LPFC_CORE_LOSS			0.252	W	Estimated Inductor core Loss
100	LPFC_COPPER_LOSS			0.262	W	Estimated Inductor copper losses
101	LPFC_TOTAL_LOSS			0.514	W	Total estimated Inductor Losses
104	**PFC Diode**					
105	PFC Diode Part Number	STTH8L06		STTH8L06		PFS Diode Part Number
106	Type / Part Number			Ultrafast		PFC Diode Type / Part Number
107	Manufacturer			ST		Diode Manufacturer
108	VRRM			600.0	V	Diode rated reverse voltage
109	IF			8.00	A	Diode rated forward current
110	Qrr			900.0	nC	Qrr at High Temperature
111	VF			1.05	V	Diode rated forward voltage drop
112	PCOND_DIODE			0.555	W	Estimated Diode conduction losses
113	PSW_DIODE			0.000	W	Estimated Diode switching losses
114	P_DIODE			0.555	W	Total estimated Diode losses
115	TJ Max			100.0	deg C	Maximum steady-state operating temperature
116	Rth-JS			2.50	degC/W	Maximum thermal resistance (Junction to heatsink)
117	HEATSINK Theta-CA			105.16	degC/W	Maximum thermal resistance of heatsink
118	IFSM			120.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
121	**Output Capacitor**					
122	COUT	120		120	uF	Minimum value of Output capacitance
123	VO_RIPPLE_EXPECTED			10.7	V	Expected ripple voltage on Output with selected Output capacitor
124	T_HOLDUP_EXPECTED			21.5	ms	Expected holdup time with selected Output capacitor
125	ESR_LF			1.38	ohms	Low Frequency Capacitor ESR
126	ESR_HF			0.55	ohms	High Frequency Capacitor ESR
127	IC_RMS_LF			0.37	A	Low Frequency Capacitor RMS current
128	IC_RMS_HF			0.91	A	High Frequency Capacitor RMS current
129	CO_LF_LOSS			0.192	W	Estimated Low Frequency ESR loss in Output capacitor
130	CO_HF_LOSS			0.459	W	Estimated High frequency ESR loss in Output capacitor
131	Total CO LOSS			0.651	W	Total estimated losses in Output Capacitor
134	**Input Bridge (BR1) and Fuse (F1)**					
135	I^2t Rating			8.43	A^2*s	Minimum I^2t rating for fuse
136	Fuse Current rating			2.60	A	Minimum Current rating of fuse

137	VF			0.90	V	Input bridge Diode forward Diode drop
138	IAVG			1.62	A	Input average current at VBROWNOUT.
139	PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
140	PCOND_LOSS_BRIDGE			1.455	W	Estimated Bridge Diode conduction loss
141	CIN	1.00		1.00	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
142	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
143	CIN_PLOSS			0.020	W	Input Capacitor Loss
144	RT1			9.37	ohms	Input Thermistor value. Adjust I_INRUSH to get the closest standard thermistor value
145	D_Precharge			1N5407		Recommended precharge Diode
148	**PFS5 Small Signal Components**					
149	RVS			10.0	kOhms	VS pin resistor for valley sensing. This resistor should be optimized such that proper delay is introduced from the instant the voltage on the sense winding goes below the Vvs2 threshold to the instant when the cascode turns-on (valley sensing). Must be tested on the bench
150	RPS			25 - 50	kOhms	Power programmability resistor
151	RV1			4.0	MOhms	Line sense resistor 1
152	RV2			6.0	MOhms	Line sense resistor 2
153	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
154	RV4			161.6	kOhms	Description pending, could be modified based on feedback chain R1-R4
155	C_V			0.495	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
156	C_VCC			1.0	uF	Supply decoupling capacitor
157	C_C			100	nF	Feedback C pin decoupling capacitor
158	Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
159	PGT set resistor			337.4	kohm	Power good threshold setting resistor
162	**Feedback Components**					
163	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
164	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
165	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor
166	RFB_4			155.5	kohms	Feedback network, lower divider resistor
167	CFB_1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
168	RFB_5			30.9	kohms	Feedback network: zero setting resistor
169	CFB_2			1000	nF	Feedback component- noise suppression capacitor
172	**Loss Budget (Estimated at VACMIN)**					
173	PFS Losses			0.473	W	Total estimated losses in PFS
174	Boost diode Losses			0.555	W	Total estimated losses in Output Diode
175	Input Bridge losses			1.455	W	Total estimated losses in input bridge module
176	Input Capacitor Losses			0.020	W	Total estimated losses in input capacitor
177	Inductor losses			0.514	W	Total estimated losses in PFC choke
178	Output Capacitor Loss			0.651	W	Total estimated losses in Output capacitor
179	EMI choke copper loss			0.081	W	Total estimated losses in EMI choke copper
180	Total losses			3.748	W	Overall loss estimate
181	Efficiency			97.48	%	Estimated efficiency at VACMIN, full load.
184	**HiperPFS-5 Integrated CAPZero Function**					
185	Total Series Resistance (Rcapzero1+Rcapzero2)			0.730	MOhms	Maximum total series resistor value to discharge X-capacitors with time constant of 1 second. Resistors must be connected to D1 and D2 pins

						of the HiperPFS-5 part for integrated CAPZero function
188	**EMI Filter Components Recommendation**					
189	CX2			470	nF	X-capacitor after differencial mode choke and before bridge, ratio with Po
190	LDM_calc			172	uH	Estimated minimum differential inductance to avoid <10kHz resonance in input current
191	CX1			470	nF	X-capacitor before common mode choke, ratio with Po
192	LCM			10.0	mH	Typical common mode choke value
193	LCM_leakage			30	uH	Estimated leakage inductance of CM choke, typical from 30~60uH
194	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
195	LDM_Actual			142	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
196	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
197	DCR_LDM			0.030	Ohms	Total DCR of DM choke(or CM #2) for estimating copper loss
199	**Note: CX2 can be placed between CM choke and DM choke depending on EMI design requirement.**					

12.2 Low Line

1	Hiper_PFS-5_Boost_051923; Rev.1.2; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	Discontinuous Mode Boost Converter Design Spreadsheet
2	**Enter Application Variables**					
3	Input Voltage Range	Universal		Universal		Input voltage range
4	VACMIN	90		90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX	170		170	VAC	Maximum AC input voltage
6	VBROWNIN		Info	82	VAC	Brown-IN voltage has been modified since the V-pin ratio is no longer 100:1
7	VBROWNOUT		Info	71	VAC	Brown-OUT voltage has been modified since the V-pin ratio is no longer 100:1
8	VO	255	Info	255	VDC	Brown IN/OUT voltage has changed due to modifications in the V-pin ratio from 100:1. Recommend Vpin ratio= FB pin ratio for optimized operation. Check the PF, input current distortion, brown in/out and power delivery
9	PO	145		145	W	Nominal Output power
10	fL			50	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	Efficiency Estimate			0.9500		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			242	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX	16		16	VDC	Maximum Output voltage ripple
15	T_HOLDUP		Warning	20	ms	Expected holdup time is smaller than specified value. Please use larger Output capacitance
16	VHOLDUP_MIN			204	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	Yes		Yes		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
20	**KP and INDUCTANCE**					
21	LPFC_MIN (0 bias)			169	uH	Minimum PFC inductance value
22	LPFC_TYP (0 bias)	175		175	uH	LPFC value used for calculations. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation.
23	LPFC_MAX (0 bias)		Warning	180	uH	LPFC_MAX exceeds the maximum required inductance (168 uH) for power delivery
24	LP_TOL	3.0		3.0	%	Tolerance of PFC Inductor Value (ferrite only)
25	LPFC_PEAK			175	uH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
26	KP_ACTUAL			0.85		Actual KP calculated from LPFC_DESIRED
28	**Basic Current Parameters**					
29	IAC_RMS			1.70	A	AC input RMS current at VACMIN and Full Power load
30	IL_RMS			2.60	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
31	IO_DC			0.57	A	Output average current/Average diode current
34	**PFS Parameters**					
35	PFS Package			F		HiperPFS package selection
36	PFS Part Number	PFS5277F		PFS5277F		If examining brownout operation, over-ride autopick with desired device size

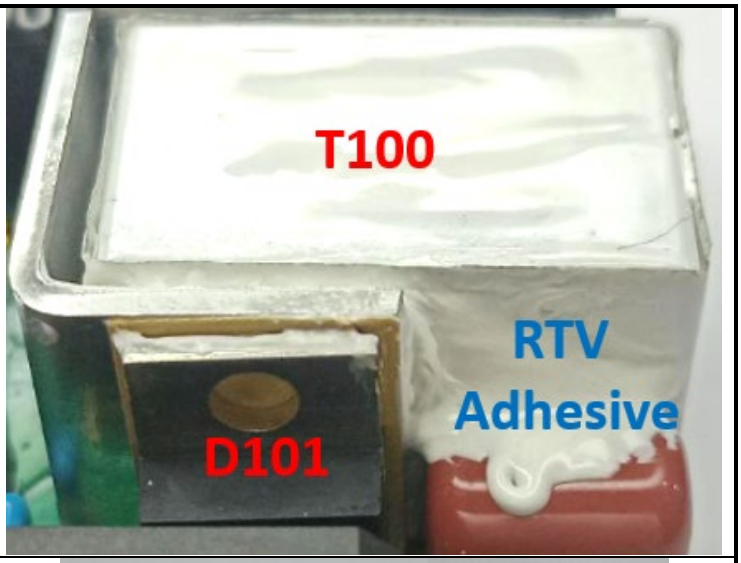
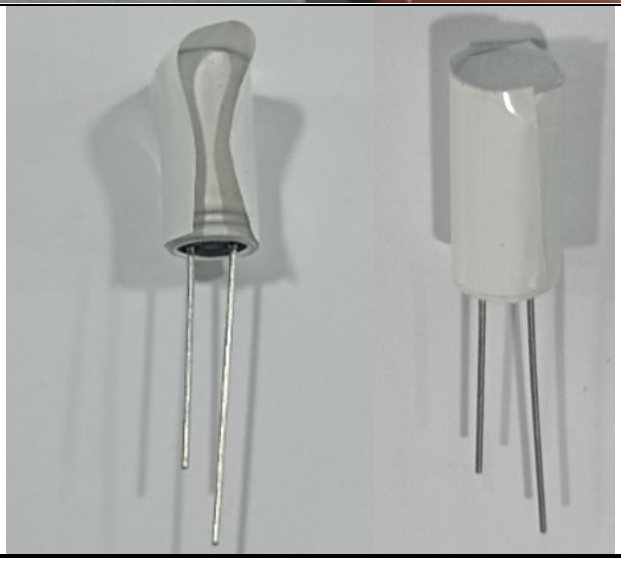
37	Self-Supply Feature	No		No		Device self-supply feature. Select "Yes" to select device with self-supply feature or "No" for device without self-supply
38	PS_FACTOR	0.8		0.8		Programmable output power selection factor
39	PO_MAX_DEV			148	W	Maximum output power of the device
40	IOCP min			6.06	A	Minimum Current limit
41	IOCP typ			6.60	A	Typical current limit
42	IOCP max			7.04	A	Maximum current limit
43	IP		Warning	6.07	A	MOSFET IOCP is reached. Input AC waveform will undergo clipping, reducing PF. Reduce KP or select larger PFS
44	IRMS			2.05	A	PFS MOSFET RMS current
45	RDSON			0.29	Ohms	Typical RDSon at 100 'C
46	FS_PK			79.8	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
47	FS_AVG			70.9	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
48	PCOND_LOSS_PFS			1.224	W	Estimated PFS Switch conduction losses
49	PSW_LOSS_PFS			2.956	W	Estimated PFS Switch switching losses
50	PFS_TOTAL			4.180	W	Total Estimated PFS Switch losses
51	TJ Max			100	deg C	Maximum steady-state junction temperature
52	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
53	HEATSINK Theta-CA			11.56	°C/W	Maximum thermal resistance of heatsink
56	**INDUCTOR DESIGN**					
57	**Material and Dimensions**					
58	Core Type			Ferrite		Ferrite core
59	Core Material	Auto		PC44/PC95		Select the core material
60	Core Geometry	ATQ		ATQ		Select the core geometry
61	Core	ATQ25/16		ATQ25/16		Core part number
62	Ae			102.00	mm^2	Core cross sectional area
63	Le			40.80	mm	Core mean path length
64	AL			6700.00	nH/t^2	Core AL value
65	Ve			4.16	cm^3	Core volume
66	HT (EE/PQ/EQ/RM/POT) / ID (toroid)			3.20	mm	Core height/Height of window; ID if toroid
67	MLT			48.8	mm	Mean length per turn
68	BW			8.00	mm	Bobbin width
69	LG			0.72	mm	Gap length (Ferrite cores only)
70	**Flux and MMF Calculations**					
71	BP_TARGET (ferrite only)	3900		3900	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
72	B_OCP (or BP)			3888	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
73	B_MAX			3252	Gauss	Peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance,minimum IOCP
77	I_TEST			6.6	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
78	B_TEST			3645	Gauss	Flux density at I_TEST and maximum tolerance inductance
80	**Wire**					
81	TURNS			32		Inductor turns. To adjust turns, change the BP_TARGET
82	ILRMS			2.60	A	Inductor RMS current
83	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire
84	AWG	44		44	AWG	Inductor wire gauge
85	Filar	175		175		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz

86	OD (per strand)			0.051	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			0.94	mm	Will be different than OD if Litz
88	DCR			0.097	ohm	Choke DC Resistance
89	P AC Resistance Ratio			0.23		Ratio of total copper loss, including HF AC, to the DC component of the loss
90	J			7.27	A/mm^2	Estimated current density of wires. It is recommended that 6 < J < 8
91	Layers			3.98		Estimated layers in winding
92	**Auxiliary Winding**					
93	N_AUX			5		Recommended auxiliary winding number of turns to ensure the supply to the VS pin
94	V_VS_MAX			1.03	V	Maximum voltage across the auxiliary winding
95	V_VS_MIN			-37.57	V	Minimum voltage across the auxiliary winding
96	RVS			10.00	kohm	Recommended series resistor to the VS pin. Place as close as possible to the VS pin of Hiper-PFS5
97	**Loss Calculations**					
98	BAC-p-p			2715	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
99	LPFC_CORE_LOSS			0.234	W	Estimated Inductor core Loss
100	LPFC_COPPER_LOSS			0.670	W	Estimated Inductor copper losses
101	LPFC_TOTAL_LOSS			0.903	W	Total estimated Inductor Losses
104	**PFC Diode**					
105	PFC Diode Part Number	STTH8L06		STTH8L06		PFS Diode Part Number
106	Type / Part Number			Ultrafast		PFC Diode Type / Part Number
107	Manufacturer			ST		Diode Manufacturer
108	VRRM			600.0	V	Diode rated reverse voltage
109	IF			8.00	A	Diode rated forward current
110	Qrr			900.0	nC	Qrr at High Temperature
111	VF			1.05	V	Diode rated forward voltage drop
112	PCOND_DIODE			0.775	W	Estimated Diode conduction losses
113	PSW_DIODE			0.961	W	Estimated Diode switching losses
114	P_DIODE			1.736	W	Total estimated Diode losses
115	TJ Max			100.0	deg C	Maximum steady-state operating temperature
116	Rth-JS			2.50	degC/W	Maximum thermal resistance (Junction to heatsink)
117	HEATSINK Theta-CA			31.56	degC/W	Maximum thermal resistance of heatsink
118	IFSM			120.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
121	**Output Capacitor**					
122	COUT	120		120	uF	Minimum value of Output capacitance
123	VO_RIPPLE_EXPECTED			15.9	V	Expected ripple voltage on Output with selected Output capacitor
124	T_HOLDUP_EXPECTED			9.7	ms	Expected holdup time with selected Output capacitor
125	ESR_LF			0.68	ohms	Low Frequency Capacitor ESR
126	ESR_HF			0.27	ohms	High Frequency Capacitor ESR
127	IC_RMS_LF			0.55	A	Low Frequency Capacitor RMS current
128	IC_RMS_HF			1.32	A	High Frequency Capacitor RMS current
129	CO_LF_LOSS			0.201	W	Estimated Low Frequency ESR loss in Output capacitor
130	CO_HF_LOSS			0.468	W	Estimated High frequency ESR loss in Output capacitor
131	Total CO LOSS			0.669	W	Total estimated losses in Output Capacitor
134	**Input Bridge (BR1) and Fuse (F1)**					
135	I^2t Rating			3.47	A^2*s	Minimum I^2t rating for fuse
136	Fuse Current rating			2.60	A	Minimum Current rating of fuse
137	VF			0.90	V	Input bridge Diode forward Diode drop
138	IAVG			1.62	A	Input average current at VBROWNOUT.
139	PIV_INPUT BRIDGE			240	V	Peak inverse voltage of input bridge
140	PCOND_LOSS_BRIDGE			2.748	W	Estimated Bridge Diode conduction loss
141	CIN	1.00		1.00	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating

142	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
143	CIN_PLOSS			0.008	W	Input Capacitor Loss
144	RT1			6.01	ohms	Input Thermistor value. Adjust I_INRUSH to get the closest standard thermistor value
145	D_Precharge			1N5407		Recommended precharge Diode
148	**PFS5 Small Signal Components**					
149	RVS			10.0	kOhms	VS pin resistor for valley sensing. This resistor should be optimized such that proper delay is introduced from the instant the voltage on the sense winding goes below the Vvs2 threshold to the instant when the cascode turns-on (valley sensing). Must be tested on the bench
150	RPS			25 - 50	kOhms	Power programmability resistor
151	RV1			4.0	MOhms	Line sense resistor 1
152	RV2			6.0	MOhms	Line sense resistor 2
153	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
154	RV4			161.6	kOhms	Description pending, could be modified based on feedback chain R1-R4
155	C_V			0.495	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
156	C_VCC			1.0	uF	Supply decoupling capacitor
157	C_C			100	nF	Feedback C pin decoupling capacitor
158	Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
159	PGT set resistor			502.8	kohm	Power good threshold setting resistor
162	**Feedback Components**					
163	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
164	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
165	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor
166	RFB_4			155.5	kohms	Feedback network, lower divider resistor
167	CFB_1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
168	RFB_5			14.0	kohms	Feedback network: zero setting resistor
169	CFB_2			1000	nF	Feedback component- noise suppression capacitor
172	**Loss Budget (Estimated at VACMIN)**					
173	PFS Losses			4.180	W	Total estimated losses in PFS
174	Boost diode Losses			1.736	W	Total estimated losses in Output Diode
175	Input Bridge losses			2.748	W	Total estimated losses in input bridge module
176	Input Capacitor Losses			0.008	W	Total estimated losses in input capacitor
177	Inductor losses			0.903	W	Total estimated losses in PFC choke
178	Output Capacitor Loss			0.669	W	Total estimated losses in Output capacitor
179	EMI choke copper loss			0.288	W	Total estimated losses in EMI choke copper
180	Total losses			10.533	W	Overall loss estimate
181	Efficiency			93.23	%	Estimated efficiency at VACMIN, full load.
184	**HiperPFS-5 Integrated CAPZero Function**					
185	Total Series Resistance (Rcapzero1+Rcapzero2)			0.730	MOhms	Maximum total series resistor value to discharge X-capacitors with time constant of 1 second. Resistors must be connected to D1 and D2 pins of the HiperPFS-5 part for integrated CAPZero function
188	**EMI Filter Components Recommendation**					
189	CX2			470	nF	X-capacitor after differencial mode choke and before bridge, ratio with Po
190	LDM_calc			172	uH	Estimated minimum differential inductance to avoid <10kHz resonance in input current

191	CX1			470	nF	X-capacitor before common mode choke, ratio with Po
192	LCM			10.0	mH	Typical common mode choke value
193	LCM_leakage			30	uH	Estimated leakage inductance of CM choke, typical from 30~60uH
194	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
195	LDM_Actual			142	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
196	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
197	DCR_LDM			0.030	Ohms	Total DCR of DM choke(or CM #2) for estimating copper loss
199	**Note: CX2 can be placed between CM choke and DM choke depending on EMI design requirement.**					

13 Special Assembly Instructions

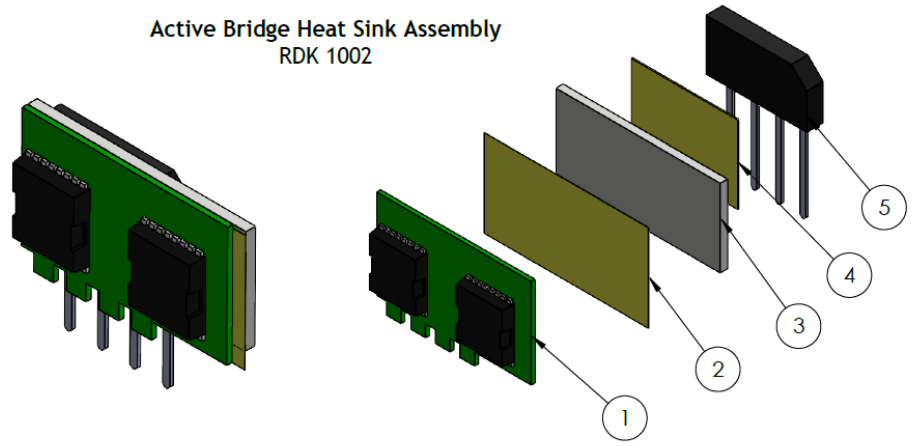
D101 – Boost Diode Apply RTV glue between the heatsink and PFC choke to prevent movement	
C113 and C114 – Output Capacitors Wrap the capacitors with tape to increase the creepage distance between the core and secondary side. Wrap the side and top of the capacitor first then add another layer going around the cylinder of the capacitor.	

14 Heat Sink Assemblies

14.1 Active Bridge (Q200 and Q201) Heat Sink

14.1.1 Active Bridge Heat Sink Assembly Instructions

Active Bridge Heat Sink Assembly
RDK 1002



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	RD-1002 Rev A	Active Bridge Board	1
2	61-00347-00	Berquist Bond Ply TBP1400	1
3	61-00345-00	Active Bridge Heat Sink	1
4	61-00346-00	Berquist Bond Ply TBP1400	1
5	15-01112-00	600V, 4A Bridge Diode GBL case	1

MATERIAL:
Aluminum 6061 0.063"

Drawn By: Michael Madson
Date: 28 Mar 2024
Checked by: Ron Nueda
Date:

General Tolerances
.XX ± .01

Do not Scale Drawing

power integrations
5245 Hellyer Avenue.
San Jose, CA 95138

Active Bridge Heat Sink Assembly
RDK 1002

PI Part NO. 61-00350-02
REV 1
WEIGHT:
SHEET 1 OF 1

Dimensions are mm & inch

ASSEMBLY INSTRUCTIONS

1. Assemble the Active Bridge PCB (Item 1).
2. Remove the liner of the TIM (Item 2) and apply the exposed side to the PCB while aligning it with CORNER B of the PCB as shown in Figure 2.
3. Remove the opposite liner of the TIM (Item 2).
4. Attach the heatsink (Item 3) to the exposed side of TIM (Item 2) while aligning it with CORNER A of the PCB.
5. Remove the liner of the TIM (Item 4) and apply the exposed side to the heatsink (Item 3) while aligning it with corner B of the PCB.
6. Remove the opposite liner of the TIM (Item 4).
7. Attach the bridge diode (Item 5 to the exposed side of the TIM (Item 4) and align it to the top edge of the TIM while also ensuring that the leads of the bridge diode are aligned with the terminations of the PCB. This prevents alignment issues when inserting the assembly into the mainboard.
8. Clamp all of the components together then bake in 125 °C for 30 minutes to cure the TIM and make the bonding permanent.

Fig.1

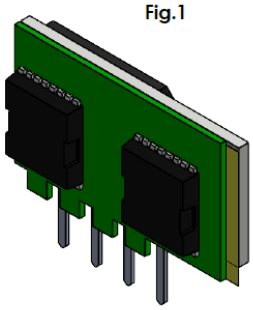
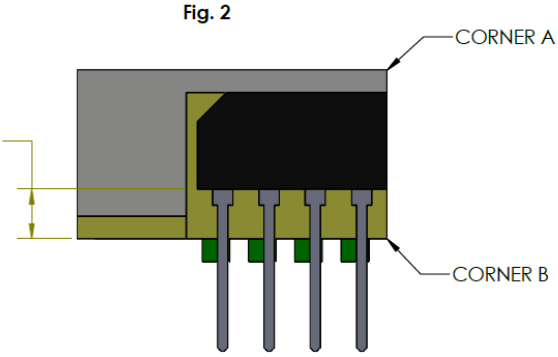


Fig. 2



Drawn By: Ron Nueda
Date: 28 March, 2024
Checked by:
Date:

DIMENSIONS ARE INCHES
INTERPRET GEOMETRIC TOLERANCING PER ASME Y14.5
.X +_.1
.XX +_.01
.XXX +_.005
ANGLES +_ 0'30"
MATERIAL
FINISH X

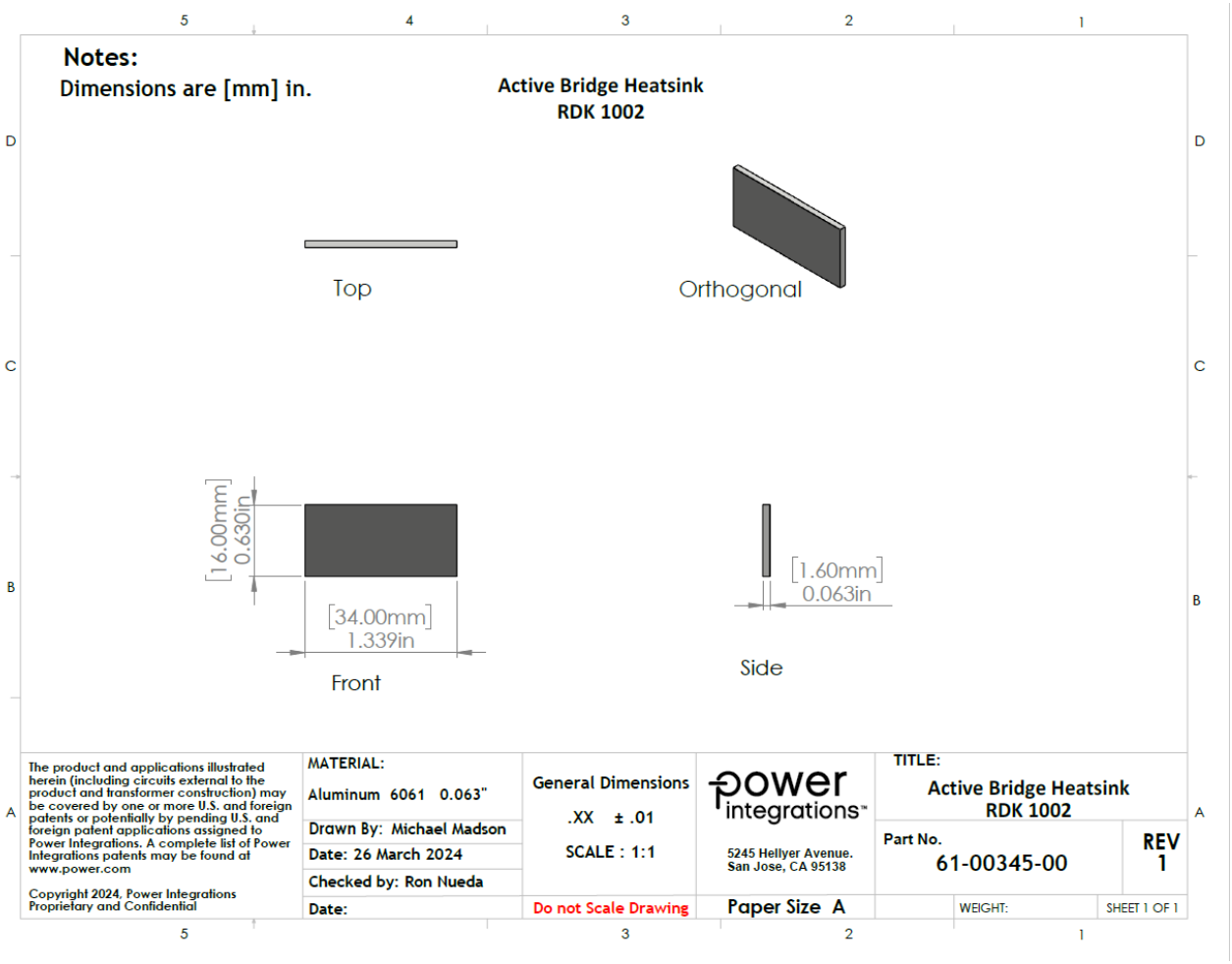
SCALE: 2:1

power integrations
5245 Hellyer Avenue.
San Jose, CA 95138
THIRD ANGLE PROJECTION

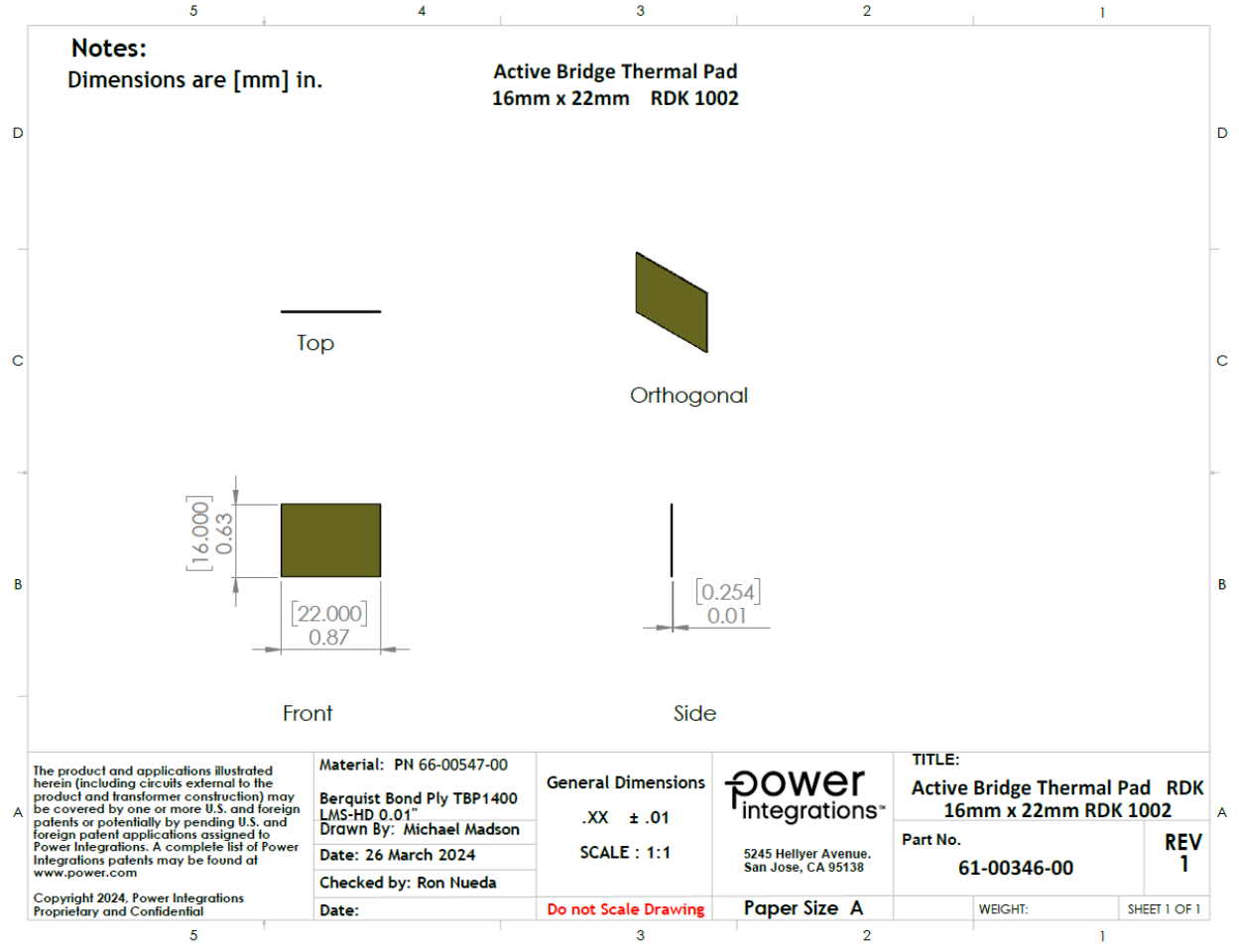
ACTIVE BRIDGE ASSEMBLY
Instructions RDK-1002

P.N. NO. 61-00350-02
REV 1
WEIGHT:
SHEET 2 OF 3

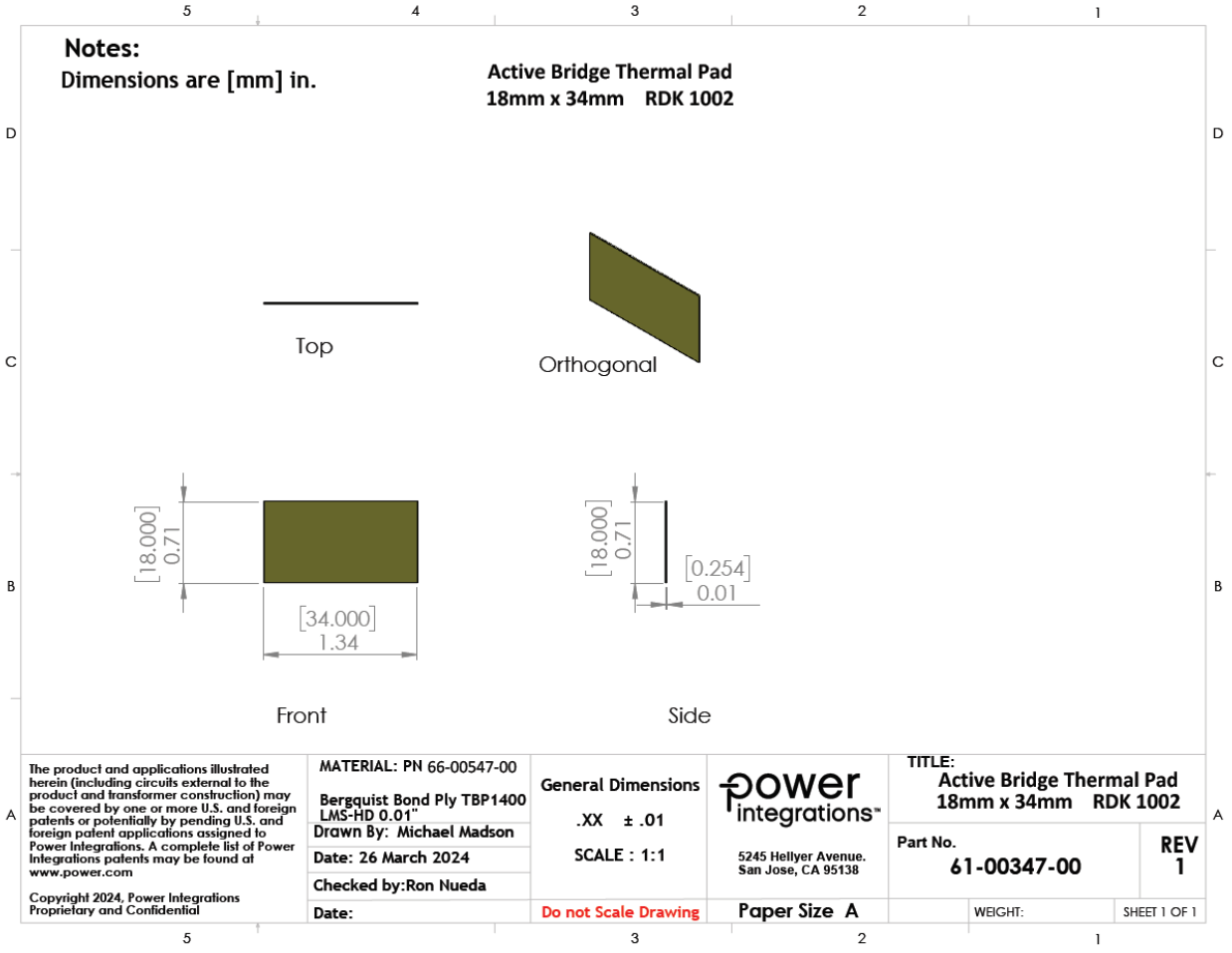
14.1.2 Active Bridge Heat Sink, 16 mm x 34 mm



14.1.3 Active Bridge Thermal Pad, 16 mm x 22 mm



14.1.4 Active Bridge Thermal Pad, 18 mm x 34 mm

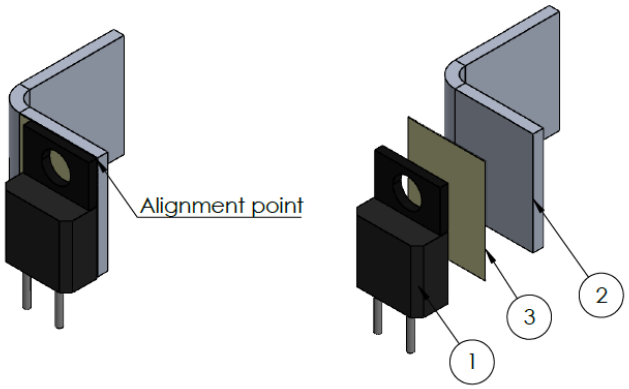


14.2 Boost Diode (D101) Heat Sink

14.2.1 Boost Diode Heat Sink Assembly Instructions

Boost Diode Heat Sink Assembly
RDK 1002

Assembly Instructions
1. Align all the components with the alignment point shown in the isometric view
2. Clamp all of the components together
3. Bake the assembly in 125 °C for 30 minutes.



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	15-02008-00	Diode 600V 8A STPR860D	1
2	61-00348-00	90 degree bent heat sink	1
3	61-00349-00	Thermal Interface Material	1

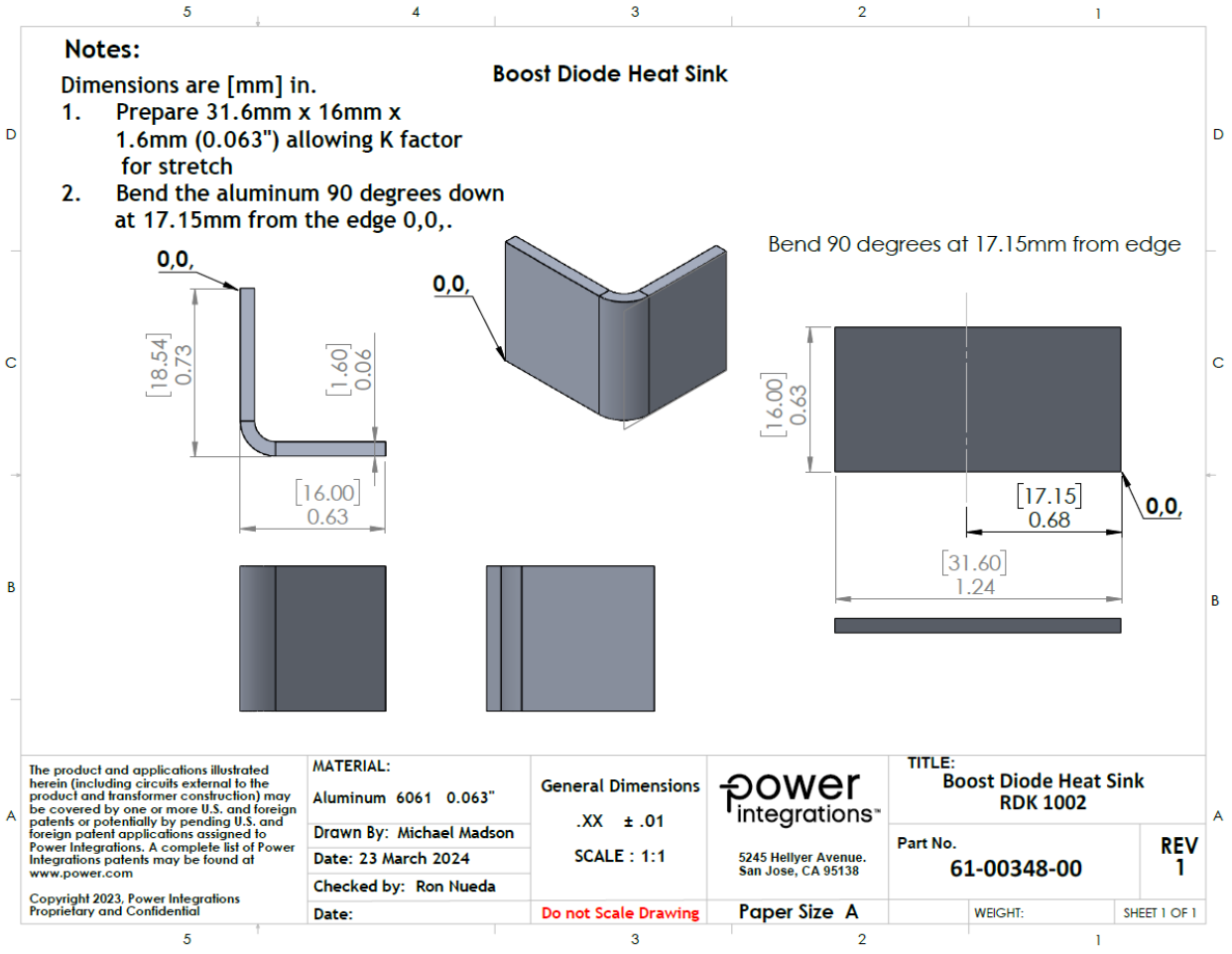
MATERIAL:
Aluminum 6061 0.063" + Diode
Drawn By: Michael Madson
Date: 27 March 2024
Checked by: Ron Nueda
Date:

General Tolerances
.XX ± .01
Do not Scale Drawing

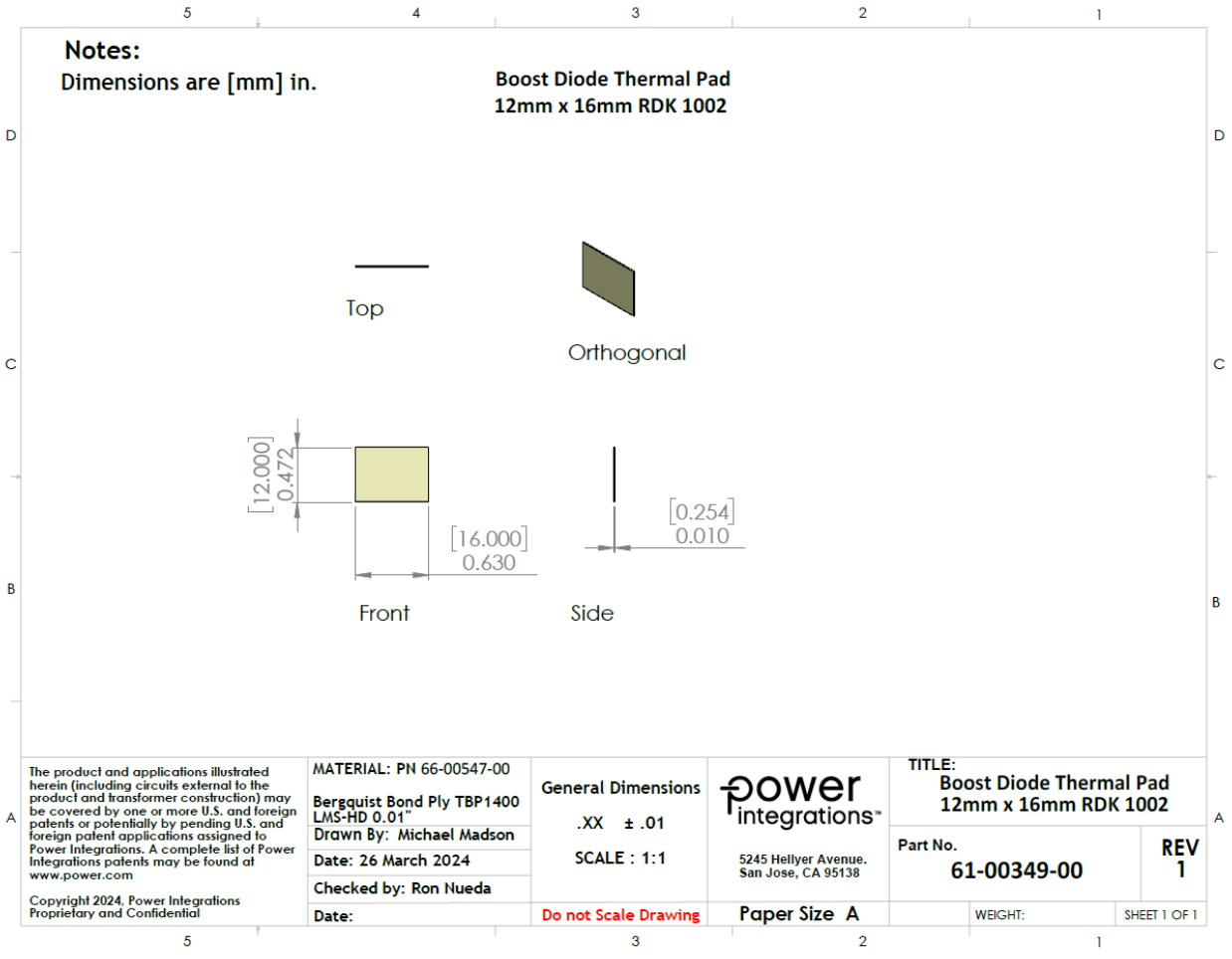
power integrations
5245 Hellyer Avenue.
San Jose, CA 95138

Boost Diode Heat Sink Assembly
RDK 1002
PI Part NO. 61-00348-02
REV 1
WEIGHT:
SHEET 1 OF 1

14.2.2 Boost Diode Heat Sink



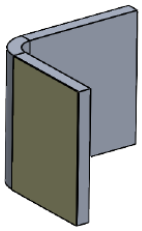
14.2.3 Boost Diode Thermal Pad, 12 mm x 16 mm

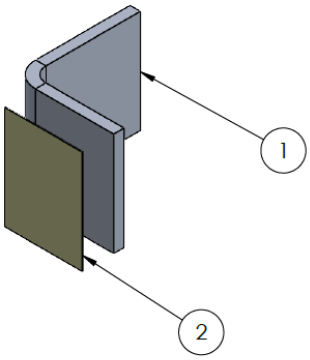


14.2.4 Boost Diode Thermal Pad and Heat Sink Assembly

Notes:
Dimensions are [mm] in.

FAB Boost Diode Heat Sink
RDK 1002





ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00348-00	90 degree bent heat sink	1
2	61-00349-00	Thermal Interface Material	1

MATERIAL: Aluminum 6061 0.063"
Drawn By: Michael Madson
Date: 26 March 2024
Checked by: Ron Nueda
Date:

General Dimensions
.XX ± .01
SCALE : 1:1
Do not Scale Drawing

power integrations™
5245 Hellyer Avenue.
San Jose, CA 95138

Paper Size A

TITLE: Fab Boost Diode Heat Sink RDK 1002
Part No. 61-00348-01
REV 1
WEIGHT:
SHEET 1 OF 1

]

15 Performance Data

Output voltages are measured across the flyback output capacitor and all the measurements are taken at room temperature unless otherwise specified.

15.1 No-Load Input Power at 5 V_{OUT}

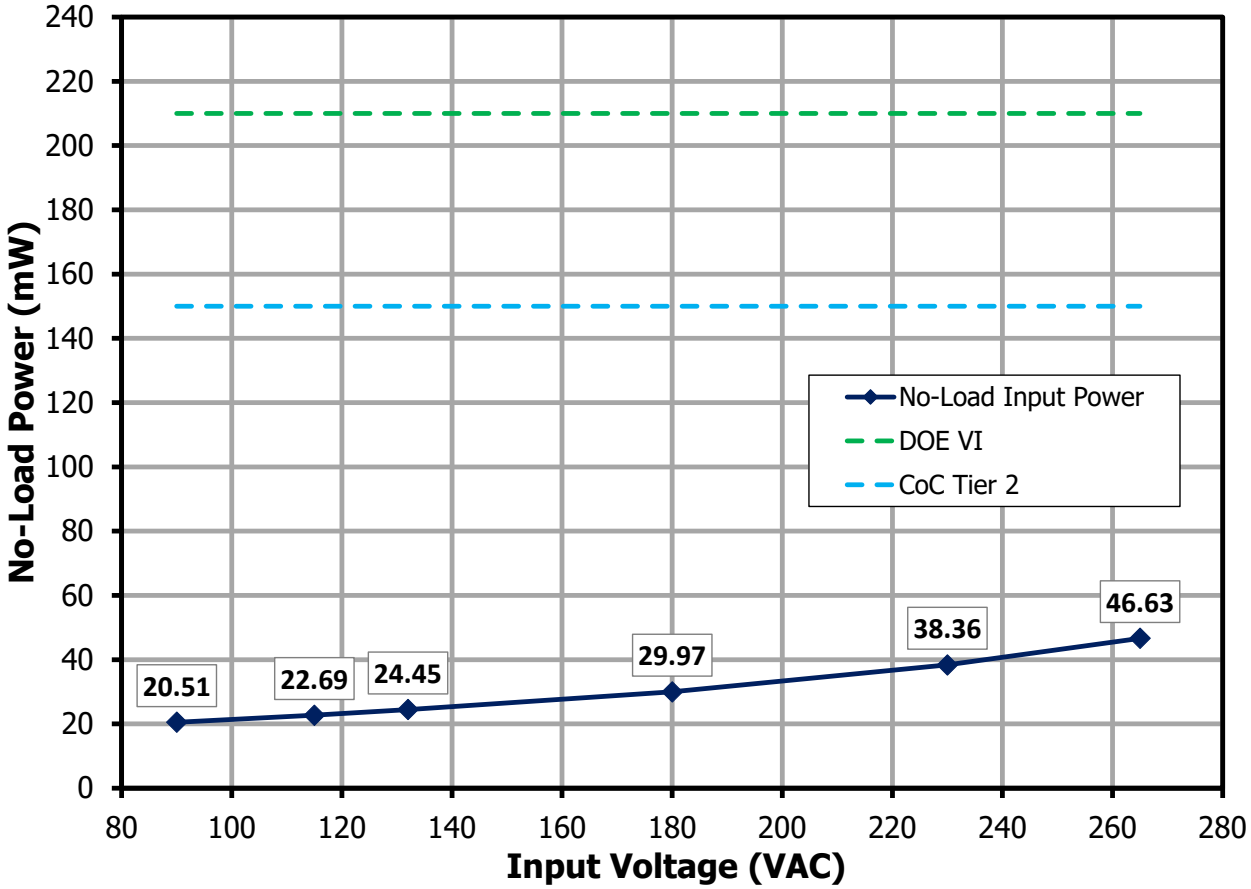


Figure 27 – No-Load Input Power vs. Input Line Voltage.

15.2 Average and 10% Load Efficiency

Note: Output voltage measured across the flyback output capacitor. Efficiency is measured at room temperature after warming up the unit for 15 min @ full load.

15.2.1 Efficiency Requirements

		Test	Average	Average	10% Load
		Effective	2016	Jan-16	Jan-16
V_{OUT} (V)	Model (V)	Power (W)	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
5	<6	15	81.4%	81.8%	72.5%
9	>6	27	86.6%	87.3%	77.3%
12	>6	60	88.0%	89.0%	79.0%
15	>6	75	88.0%	89.0%	79.0%
20	>6	100	88.0%	89.0%	79.0%
28	>6	130	88.0%	89.0%	79.0%

15.2.2 Efficiency Performance Summary (On Board)

V_{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	15	93.52	93.37	91.10	89.07
9	27	93.73	94.09	90.18	89.25
12	60	93.98	93.97	91.92	91.68
15	45	94.11	94.27	91.56	91.74
20	100	93.84	94.16	89.77	89.64
28	140	94.22	94.44	91.06	91.15

15.2.3 Average Efficiency Chart

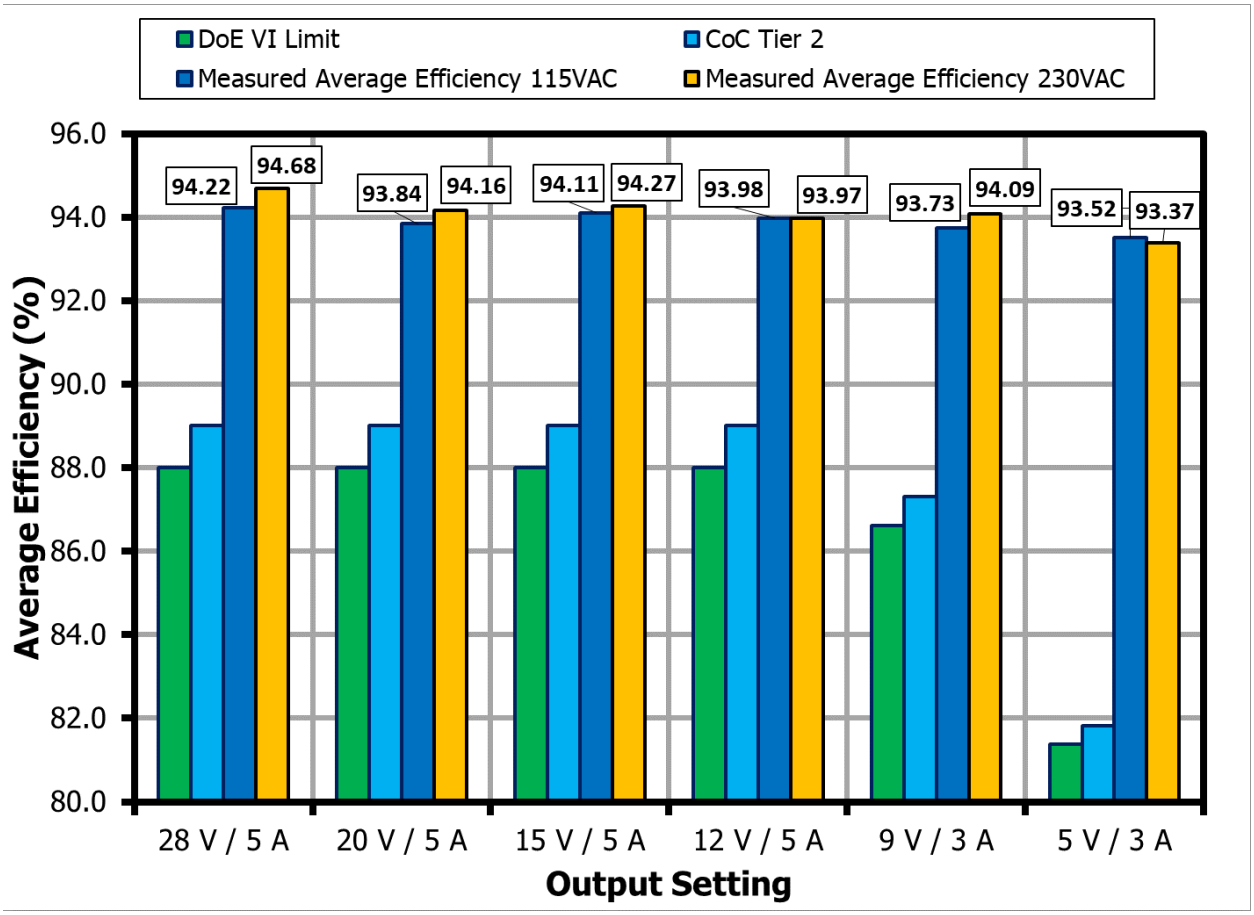


Figure 28 – Average Efficiency at 115 VAC, 60 Hz.

15.2.4 10% Load Efficiency Chart

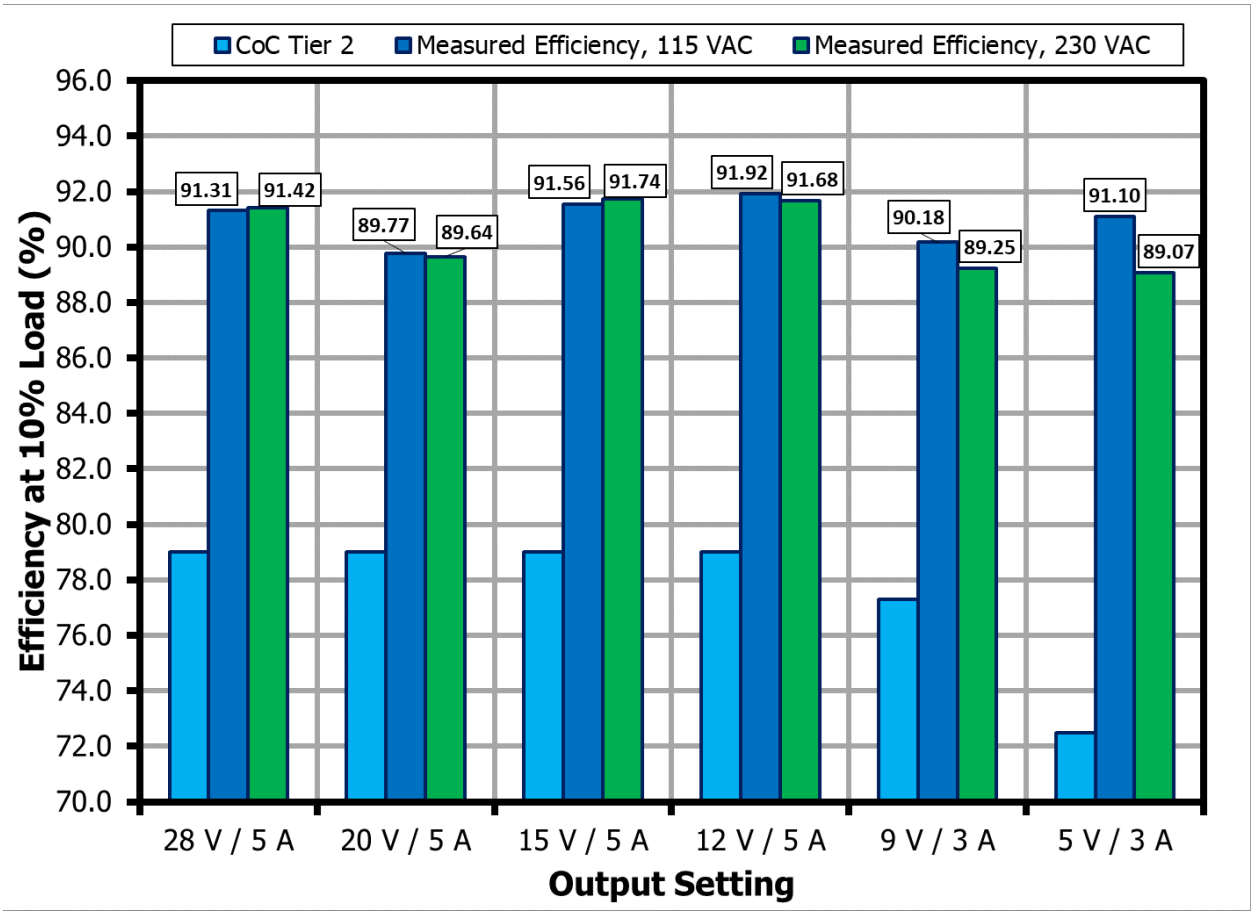


Figure 29 – Efficiency at 10% load, 115 VAC, 60 Hz.

15.2.5 Measured Efficiency, 115 VAC

15.2.5.1 Output: 5 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.68	93.69	**93.52**
75	11.77	93.75	
50	7.85	93.63	
25	3.93	93.01	
10	1.57	91.10	

15.2.5.2 Output: 9 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	27.75	93.95	**93.73**
75	20.82	94.04	
50	13.88	93.96	
25	6.94	92.97	
10	2.78	90.18	

15.2.5.3 Output: 12 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	61.33	94.18	**93.98**
75	46.06	94.06	
50	30.72	93.81	
25	15.34	93.87	
10	6.14	91.92	

15.2.5.4 Output: 15 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	76.38	94.36	**94.11**
75	57.36	94.24	
50	38.25	93.98	
25	19.11	93.85	
10	7.64	91.56	

15.2.5.5 Output: 20 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	101.47	94.38	**93.84**
75	76.14	94.20	
50	50.77	93.78	
25	25.36	92.99	
10	10.14	89.77	

15.2.5.6 Output: 28 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	140.89	94.63	**94.22**
75	105.95	94.58	
50	70.64	94.17	
25	35.31	93.51	
10	14.12	91.06	

15.2.6 Measured Efficiency, 230 VAC

15.2.6.1 Output: 5 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.73	94.06	**93.37**
75	11.80	93.90	
50	7.87	93.46	
25	3.93	92.07	
10	1.57	89.07	

15.2.6.2 Output: 9 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	27.81	94.75	**94.09**
75	20.85	94.62	
50	13.90	94.20	
25	6.94	92.78	
10	2.78	89.25	

15.2.6.3 Output: 12 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	61.42	94.38	**93.97**
75	46.11	94.03	
50	30.74	93.31	
25	15.35	94.13	
10	6.14	91.68	

15.2.6.4 Output: 15 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	76.48	94.69	**94.27**
75	57.40	94.39	
50	38.27	93.74	
25	19.11	94.26	
10	7.64	91.74	

15.2.6.5 Output: 20 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	101.55	94.86	**94.16**
75	76.18	94.48	
50	50.79	93.74	
25	25.37	93.55	
10	10.14	89.64	

15.2.6.6 Output: 28 V / 5 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	141.36	94.90	**94.44**
75	106.03	94.75	
50	70.68	93.91	
25	35.32	94.21	
10	14.13	91.15	

15.3 Full Load Efficiency Data (On Board)

	Input		Input Measurement					Ouput Measurement				
	VAC (RMS)	**Freq (Hz)**	**V_{IN} (RMS)**	**I_{IN} (mA)**	**P_{IN} (W)**	**PF**	**%THD**	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**%V Reg**	**Efficiency (%)**
28 V / 5 A	90	60	90.0	1675.2	149.87	0.99	8.58	28.18	4.999	140.88	0.64	94.00
	115	60	115.0	1304.4	148.90	0.99	4.31	28.18	4.999	140.88	0.65	94.61
	230	50	230.0	649.2	148.07	0.99	10.04	28.20	4.999	140.99	0.73	95.22
	265	50	265.0	670.5	148.28	0.83	54.17	28.27	4.999	141.34	0.97	95.32
	Input		**Input Measurement**					**Ouput Measurement**				
	VAC (RMS)	**Freq (Hz)**	**V_{IN} (RMS)**	**I_{IN} (mA)**	**P_{IN} (W)**	**PF**	**%THD**	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**%V Reg**	**Efficiency (%)**
20 V / 5 A	90	60	90.0	1208.2	108.09	0.99	5.46	20.30	4.999	101.47	1.49	93.87
	115	60	115.0	949.1	107.51	0.98	8.38	20.30	4.999	101.47	1.49	94.38
	230	50	230.0	472.9	107.06	0.99	8.41	20.31	4.999	101.55	1.56	94.86
	265	50	265.0	489.8	106.90	0.82	48.65	20.31	4.999	101.55	1.56	94.99
	Input		**Input Measurement**					**Ouput Measurement**				
	VAC (RMS)	**Freq (Hz)**	**V_{IN} (RMS)**	**I_{IN} (mA)**	**P_{IN} (W)**	**PF**	**%THD**	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**%V Reg**	**Efficiency (%)**
15 V / 5 A	90	60	90.0	912.5	81.38	0.99	4.19	15.29	4.999	76.41	1.91	93.90
	115	60	115.0	718.8	80.95	0.98	10.05	15.28	4.999	76.38	1.86	94.36
	230	50	230.0	364.3	80.77	0.97	9.32	15.30	4.999	76.48	1.99	94.69
	265	50	265.0	382.6	80.80	0.79	45.56	15.30	4.999	76.48	1.99	94.65
	Input		**Input Measurement**					**Ouput Measurement**				
	VAC (RMS)	**Freq (Hz)**	**V_{IN} (RMS)**	**I_{IN} (mA)**	**P_{IN} (W)**	**PF**	**%THD**	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**%V Reg**	**Efficiency (%)**
12 V / 5 A	90	60	90.0	734.5	65.36	0.99	3.60	12.26	4.999	61.31	2.18	93.80
	115	60	115.0	582.0	65.11	0.97	10.42	12.27	4.999	61.33	2.23	94.18
	230	50	230.0	303.3	65.08	0.94	11.45	12.29	4.999	61.42	2.38	94.38
	265	50	265.0	328.6	64.99	0.75	46.70	12.29	4.999	61.42	2.38	94.49
	Input		**Input Measurement**					**Ouput Measurement**				
	VAC (RMS)	**Freq (Hz)**	**V_{IN} (RMS)**	**I_{IN} (mA)**	**P_{IN} (W)**	**PF**	**%THD**	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**%V Reg**	**Efficiency (%)**
9 V / 5 A	90	60	90.0	785.3	29.70	0.42	199.39	9.24	3.000	27.71	2.62	93.29
	115	60	115.0	638.0	29.54	0.40	216.25	9.25	3.000	27.75	2.78	93.95
	230	50	230.0	370.9	29.35	0.34	252.63	9.27	3.000	27.81	3.00	94.75
	265	50	265.0	330.4	29.37	0.34	253.44	9.27	3.000	27.82	3.03	94.71
	Input		**Input Measurement**					**Ouput Measurement**				
	VAC (RMS)	**Freq (Hz)**	**V_{IN} (RMS)**	**I_{IN} (mA)**	**P_{IN} (W)**	**PF**	**%THD**	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**%V Reg**	**Efficiency (%)**
5 V / 5 A	90	60	90.0	463.0	16.80	0.40	213.83	5.22	3.000	15.65	4.36	93.18
	115	60	115.0	378.1	16.74	0.39	225.47	5.23	3.000	15.68	4.56	93.69
	230	50	230.0	231.6	16.73	0.31	252.60	5.25	3.000	15.73	4.90	94.06
	265	50	265.0	209.0	16.77	0.30	244.47	5.25	3.000	15.74	4.94	93.84

15.4 Efficiency Across Line (On Board)

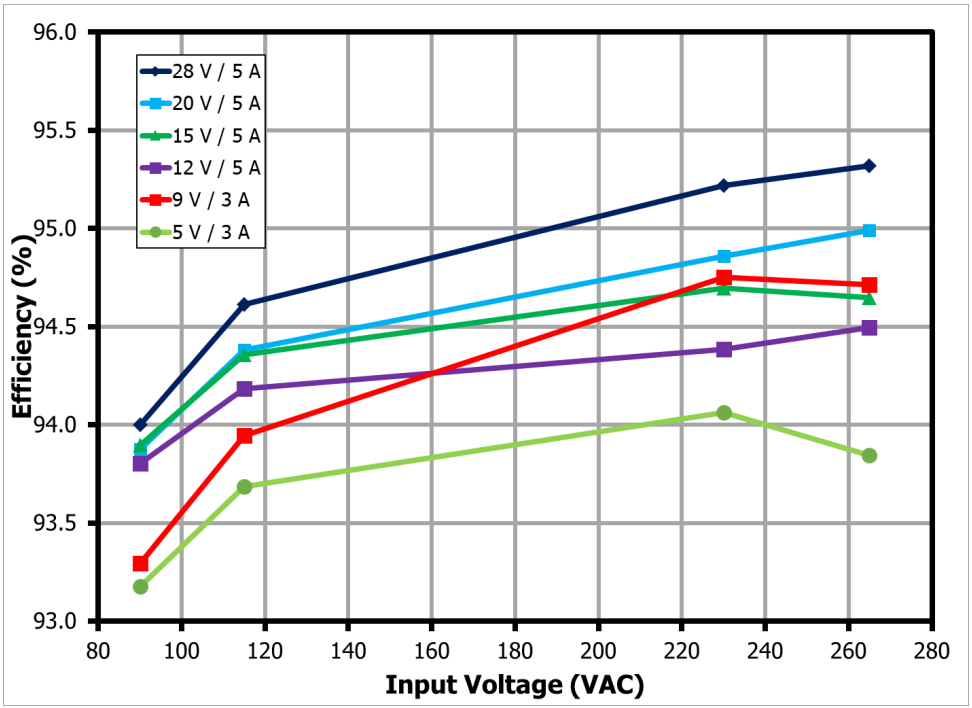


Figure 30 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, 20 V and 28 V Output, Room Temperature.

15.5 Line Regulation (On Board)

15.5.1 Output: 5 V / 3 A

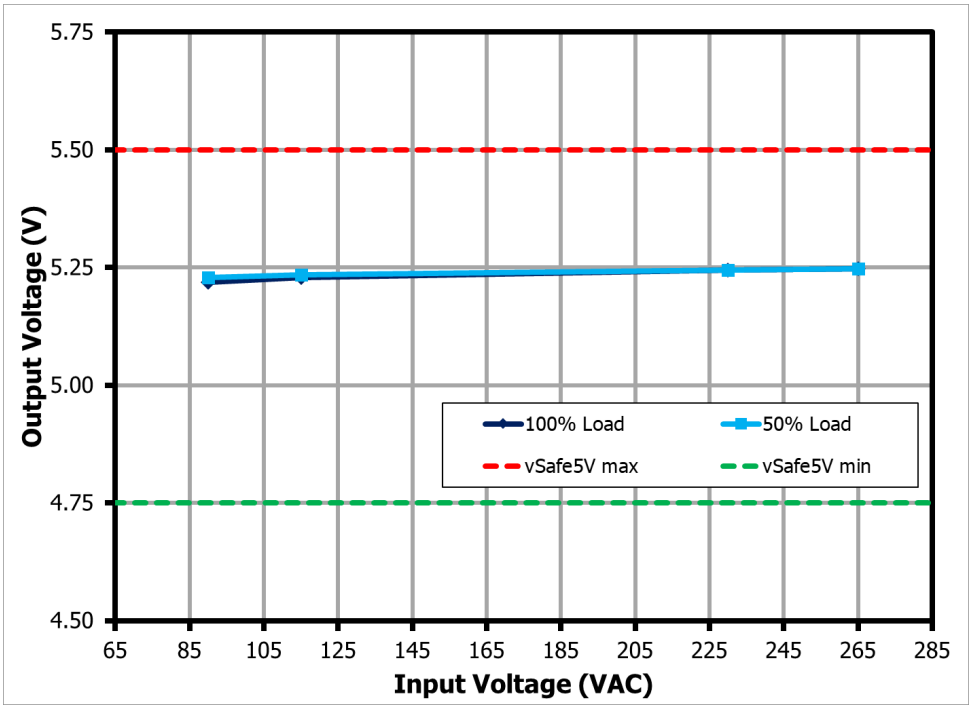


Figure 31 – Output Voltage vs. Input Voltage for 5 V Output, Room Temperature.

Note: USB PD Specification defines vSafe5V (4.75 V to 5.5 V, measured on-board) as the allowable VBUS Voltage range at 5 V operation.

15.5.2 Output: 9 V / 3 A

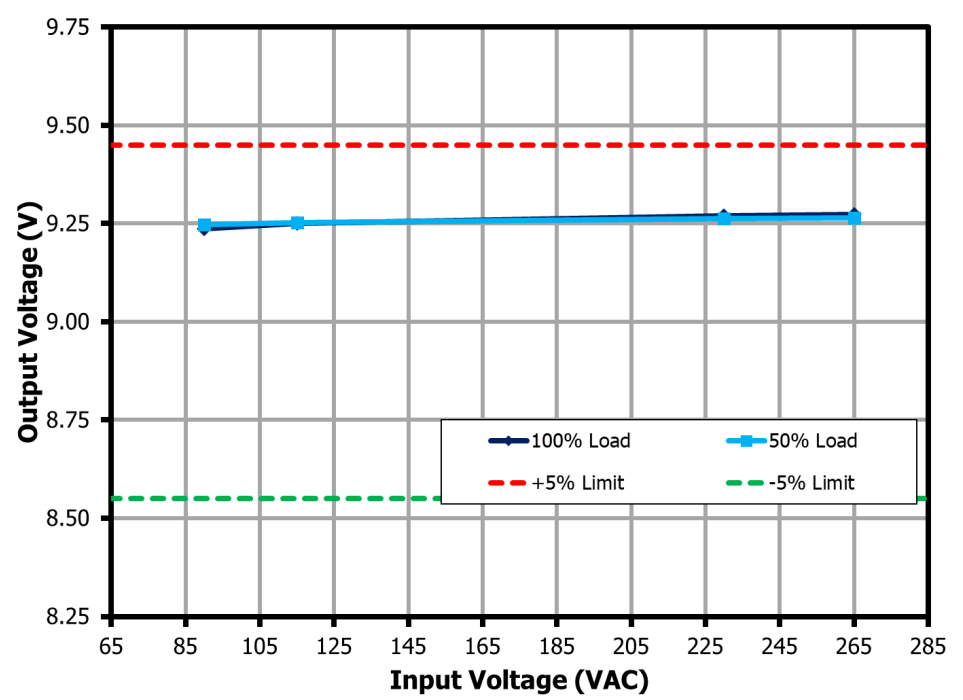


Figure 32 – Output Voltage vs. Input Voltage for 9 V Output, Room Temperature.

15.5.3 Output: 12 V / 5 A

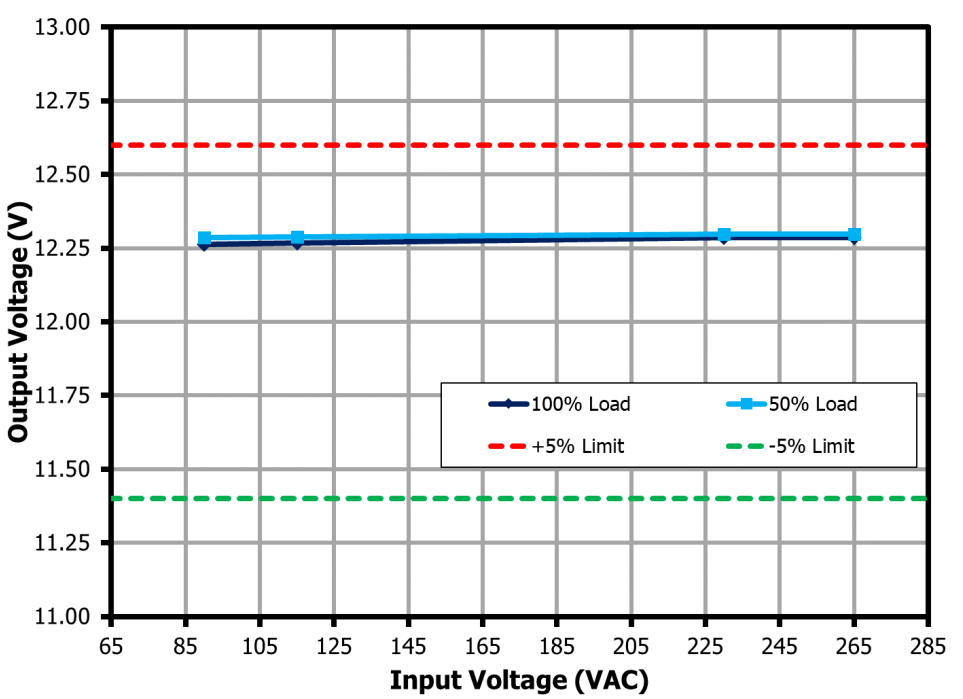


Figure 33 – Output Voltage vs. Input Voltage for 12 V Output, Room Temperature.

15.5.4 Output: 15 V / 3 A

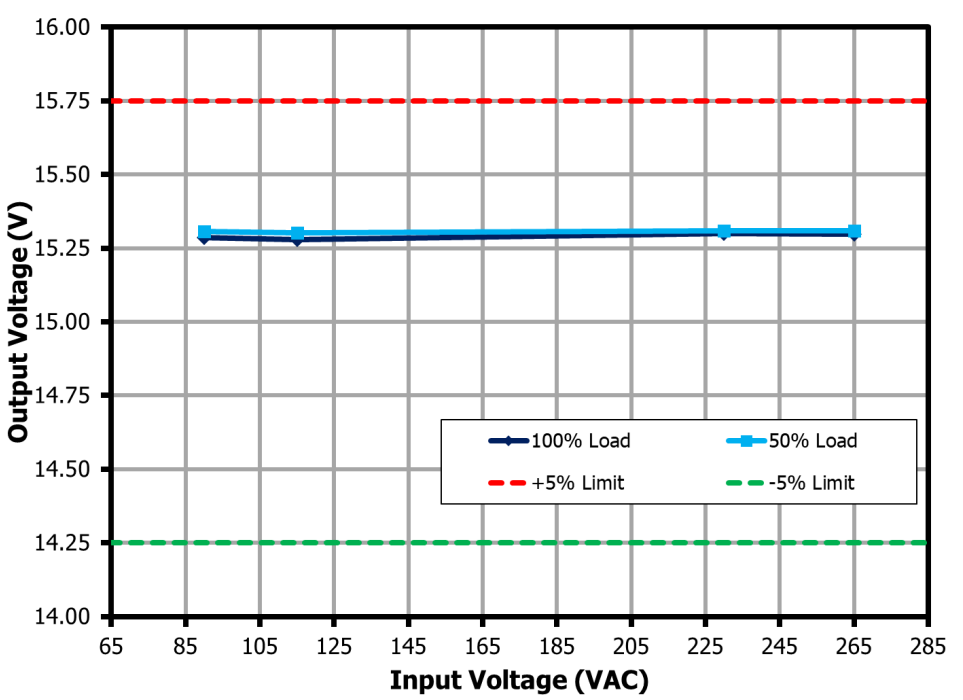


Figure 34 – Output Voltage vs. Input Voltage for 15 V Output, Room Temperature.

15.5.5 Output: 20 V / 3 A

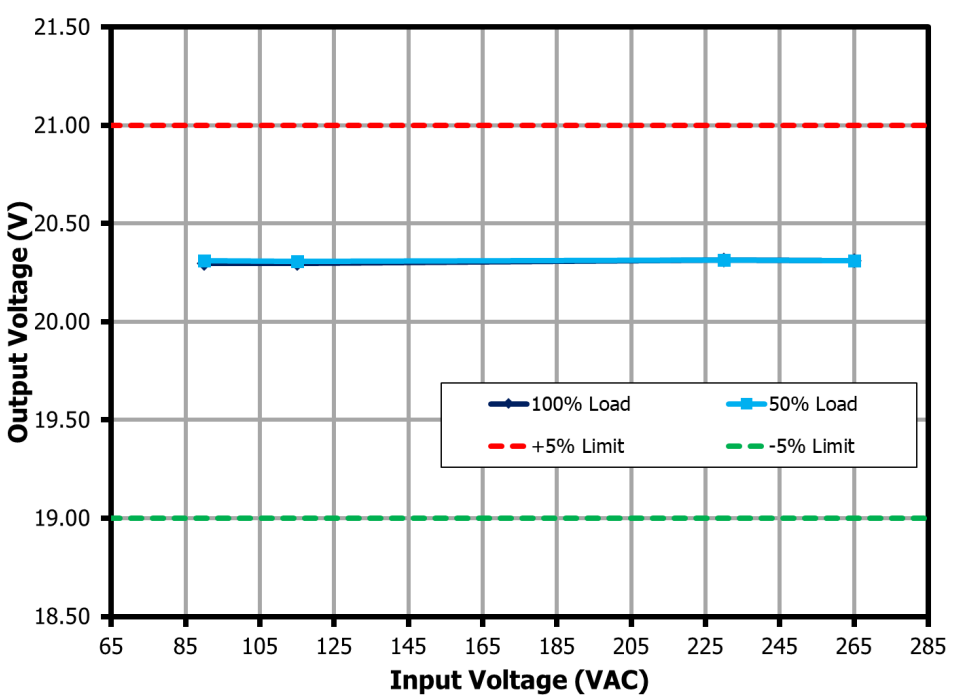


Figure 35 – Output Voltage vs. Input Voltage for 20 V Output, Room Temperature.

15.5.6 Output: 28 V / 3 A

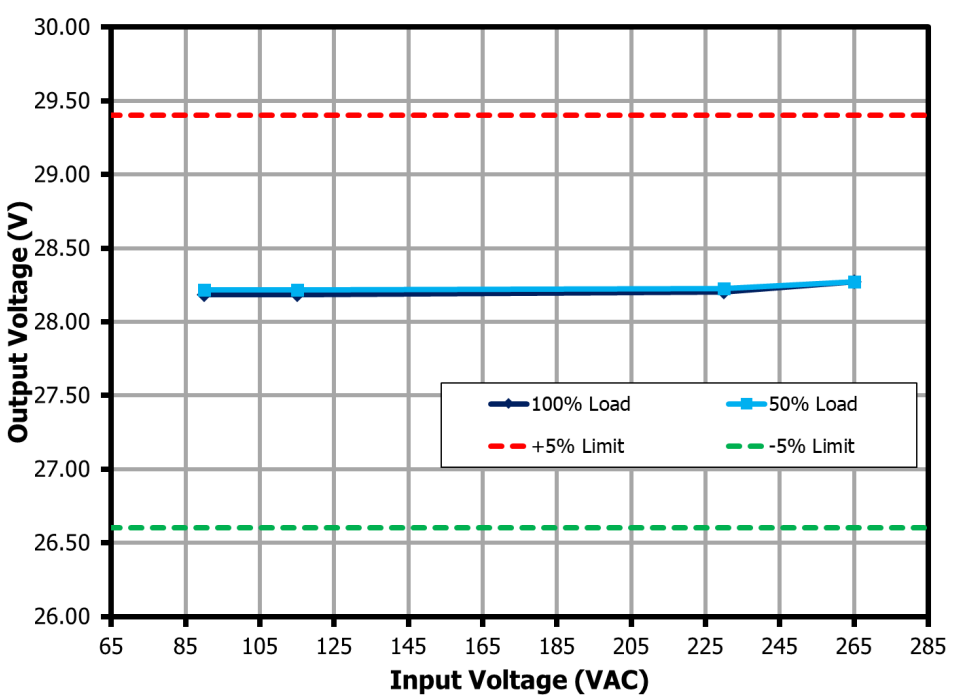


Figure 36 – Output Voltage vs. Input Voltage for 28 V Output, Room Temperature.

15.6 Load Regulation (On Board)

15.6.1 Output: 5 V / 3 A

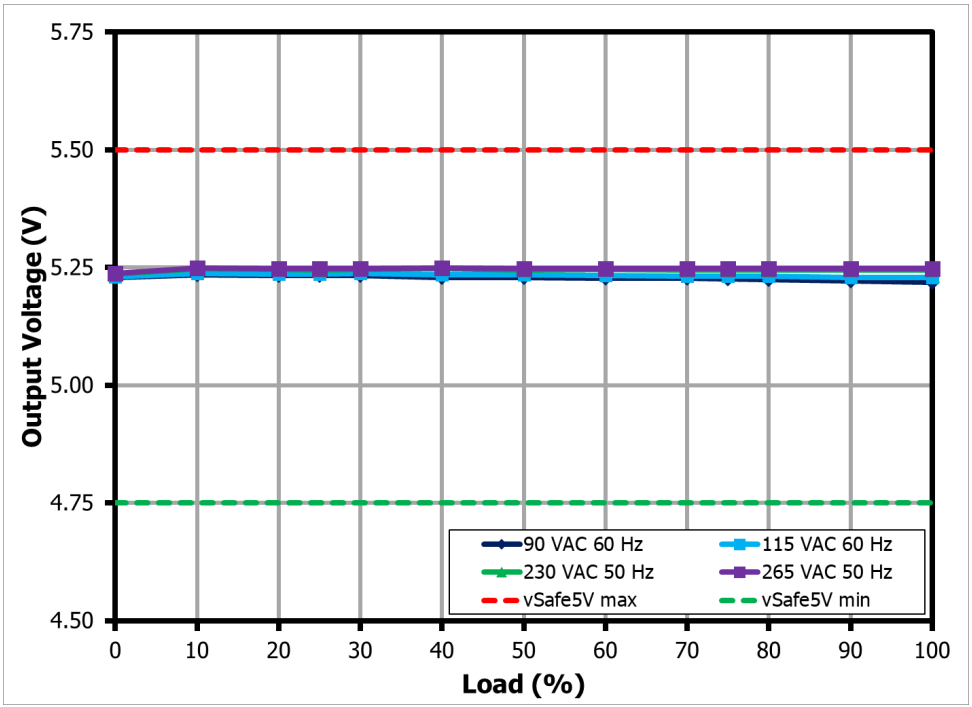


Figure 37 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

Note: USB PD Specification defines vSafe5V (4.75 V to 5.5 V, measured on-board) as the allowable VBUS Voltage range at 5 V operation.

15.6.2 Output: 9 V / 3 A

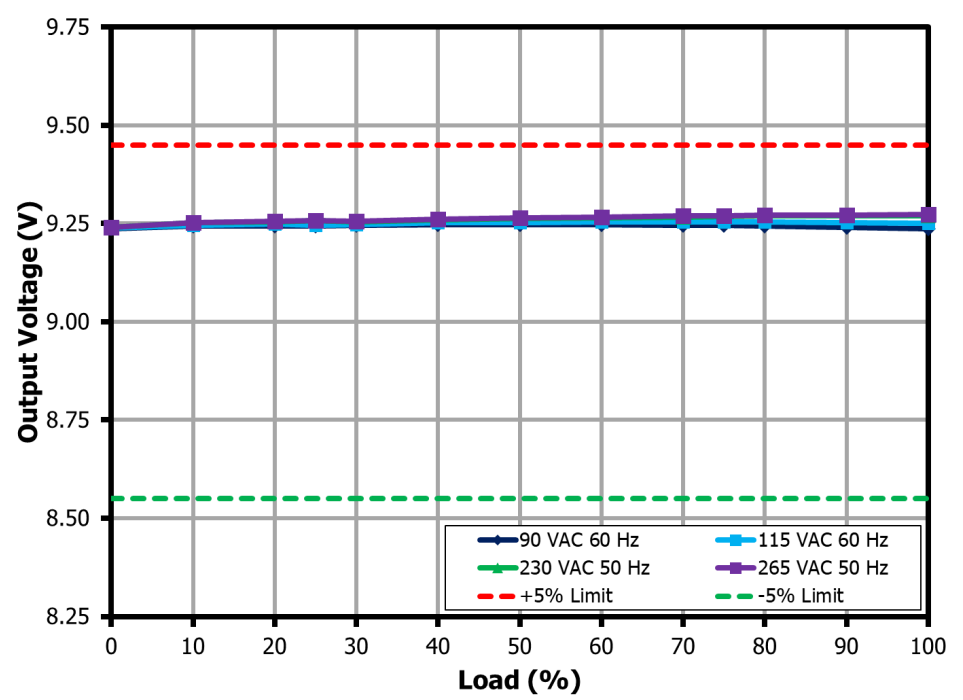


Figure 38 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

15.6.3 Output: 12 V / 5 A

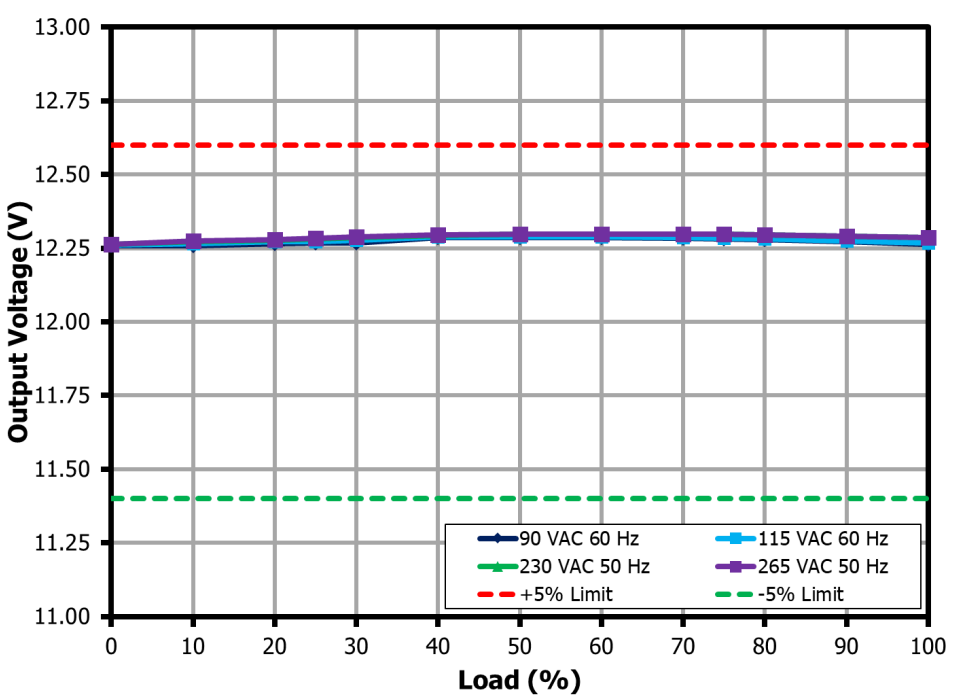


Figure 39 - Output Voltage vs. Output Load for 12 V Output, Room Temperature.

15.6.4 Output: 15 V / 5 A

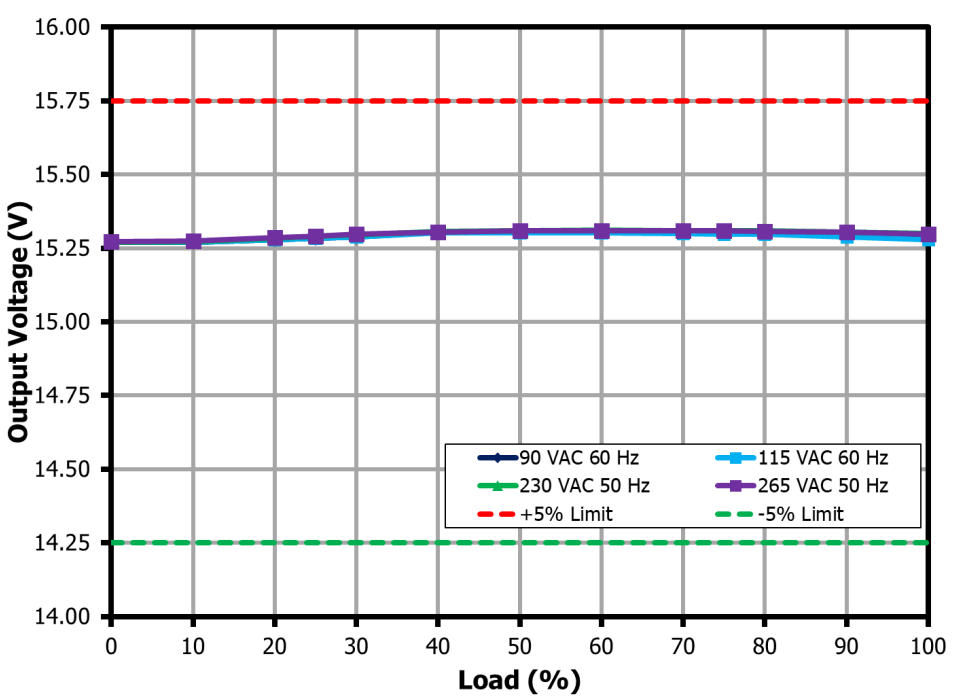


Figure 40 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

15.6.5 Output: 20 V / 5 A

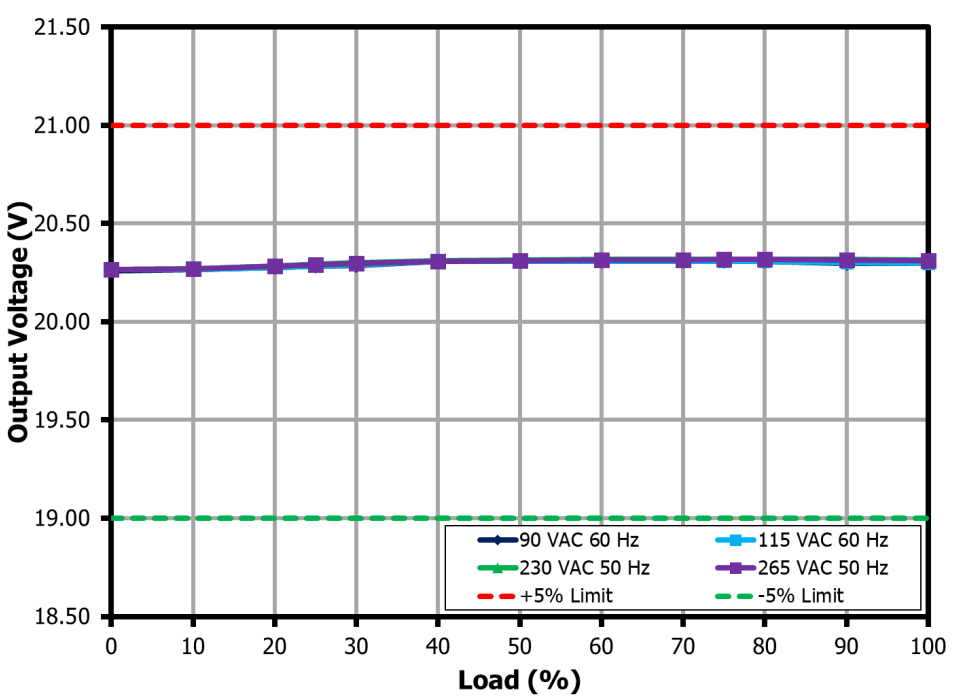


Figure 41 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

15.6.6 Output: 28 V / 5 A

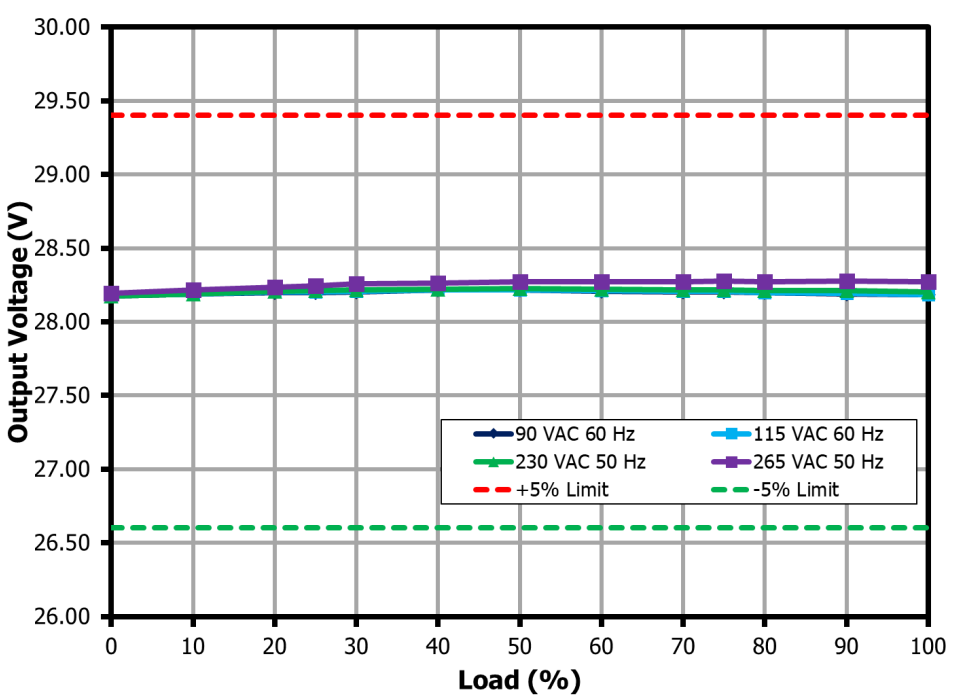


Figure 42 – Output Voltage vs. Output Load for 28 V Output, Room Temperature.

15.7 Efficiency vs Load (On Board)

15.7.1 Output: 5 V / 3 A

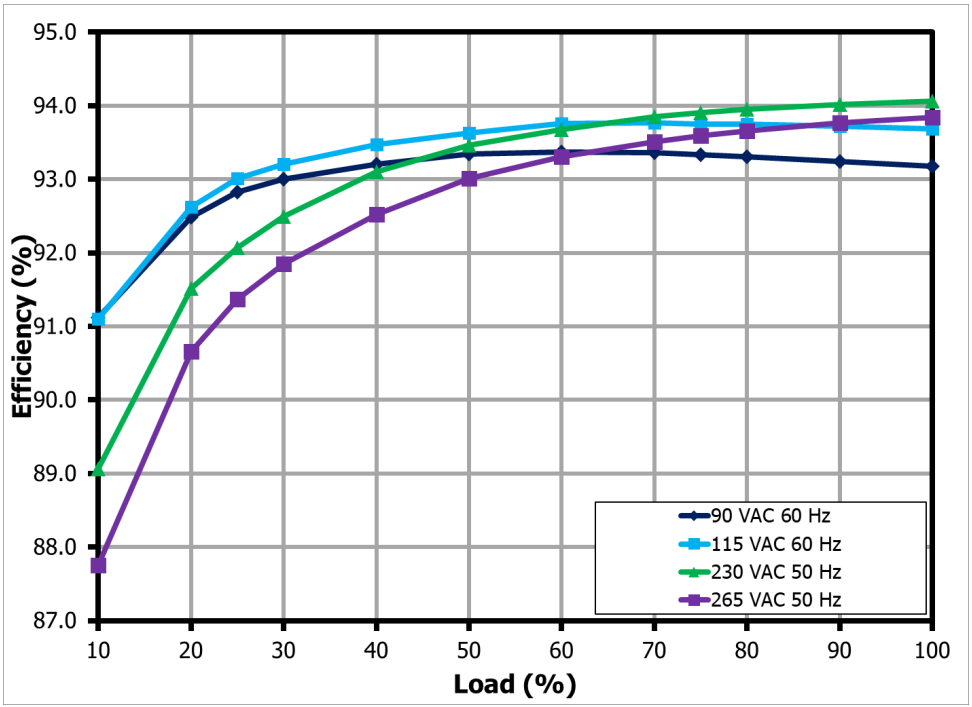


Figure 43 – Efficiency vs. Output Load for 5 V Output, Room Temperature.

15.7.2 Output: 9 V / 3 A

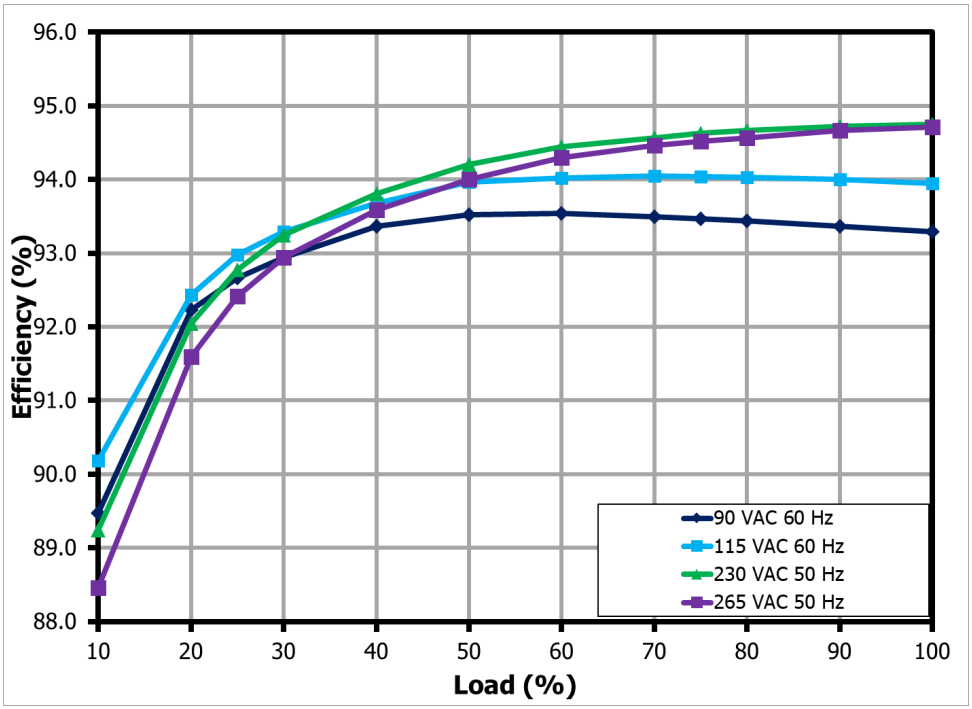


Figure 44 – Efficiency vs. Output Load for 9 V Output, Room Temperature.

15.7.3 Output: 12 V / 5 A

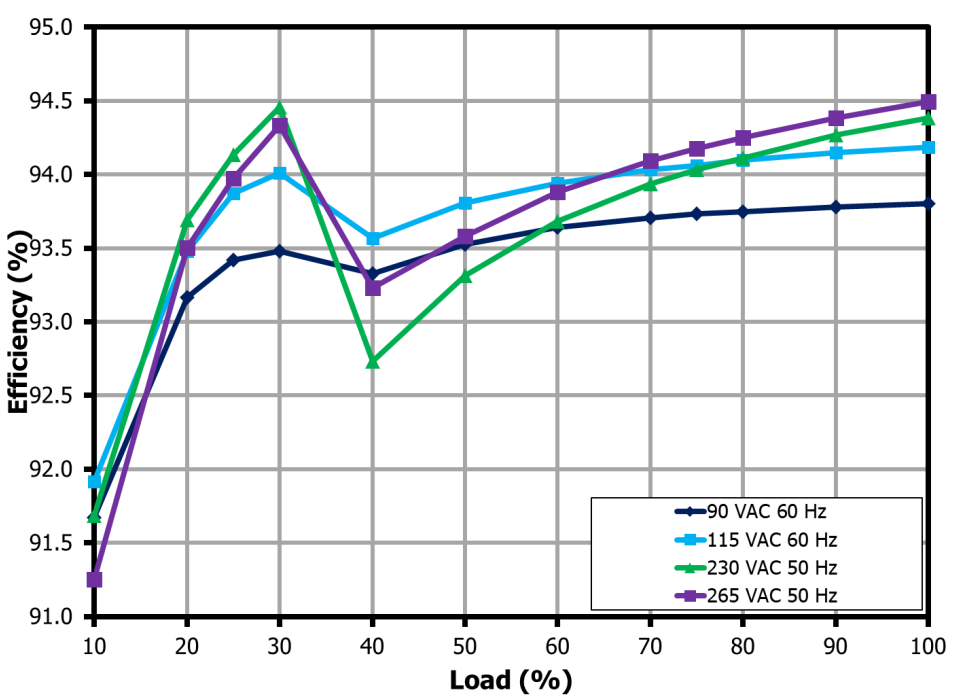


Figure 45 – Efficiency vs. Output Load for 12 V Output, Room Temperature.

15.7.4 Output: 15 V / 5 A

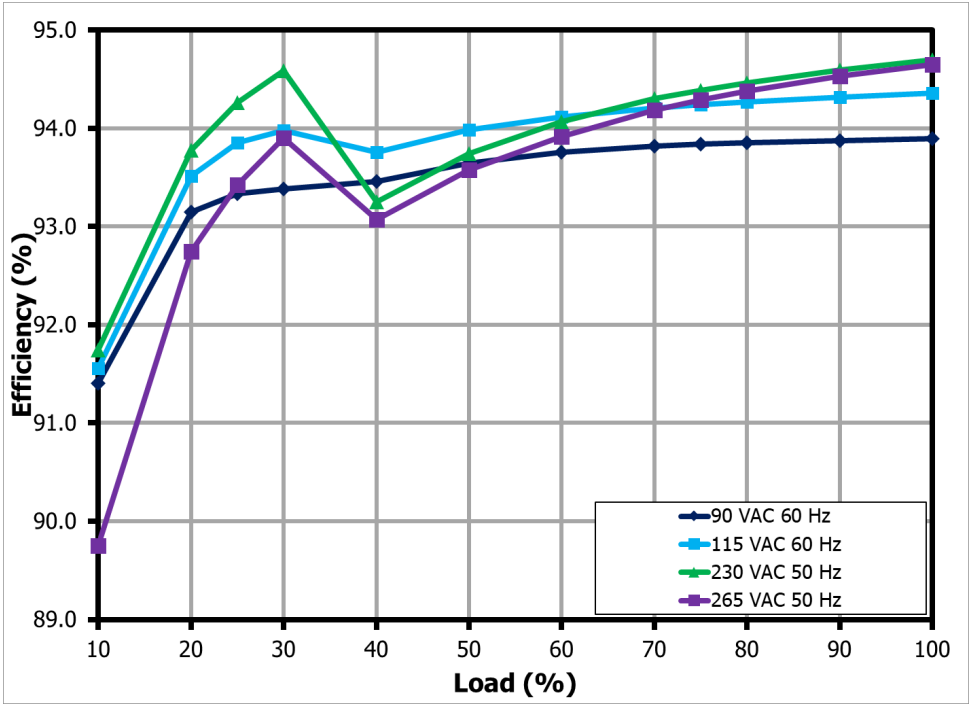


Figure 46 – Efficiency vs. Output Load for 15 V Output, Room Temperature.

15.7.5 Output: 20 V / 5 A

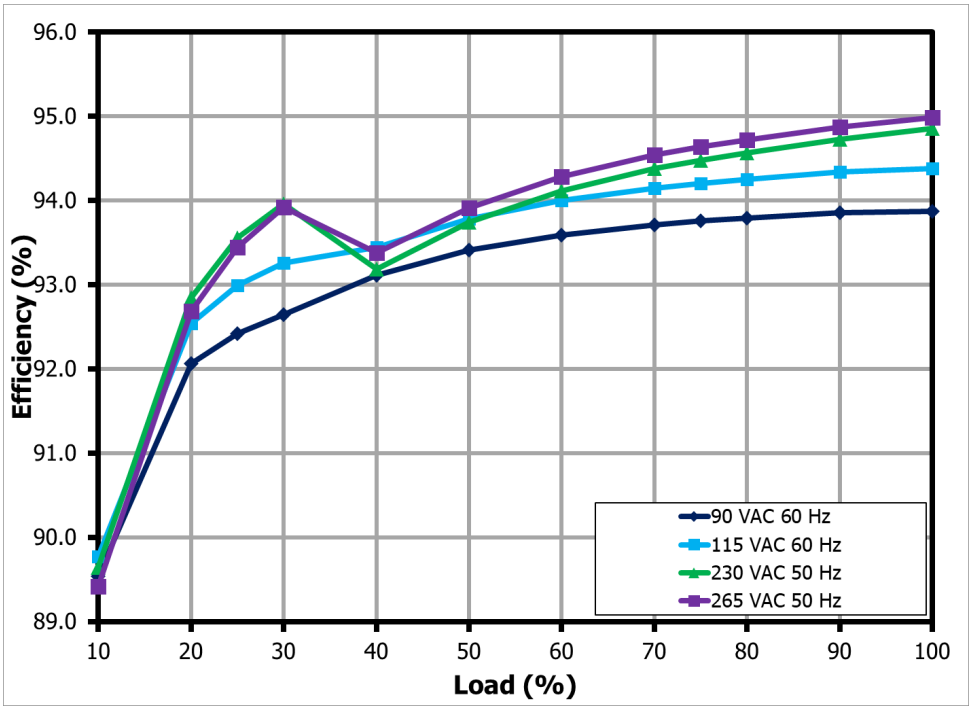


Figure 47 – Efficiency vs. Output Load for 20 V Output, Room Temperature.

15.7.6 Output: 28 V / 5 A

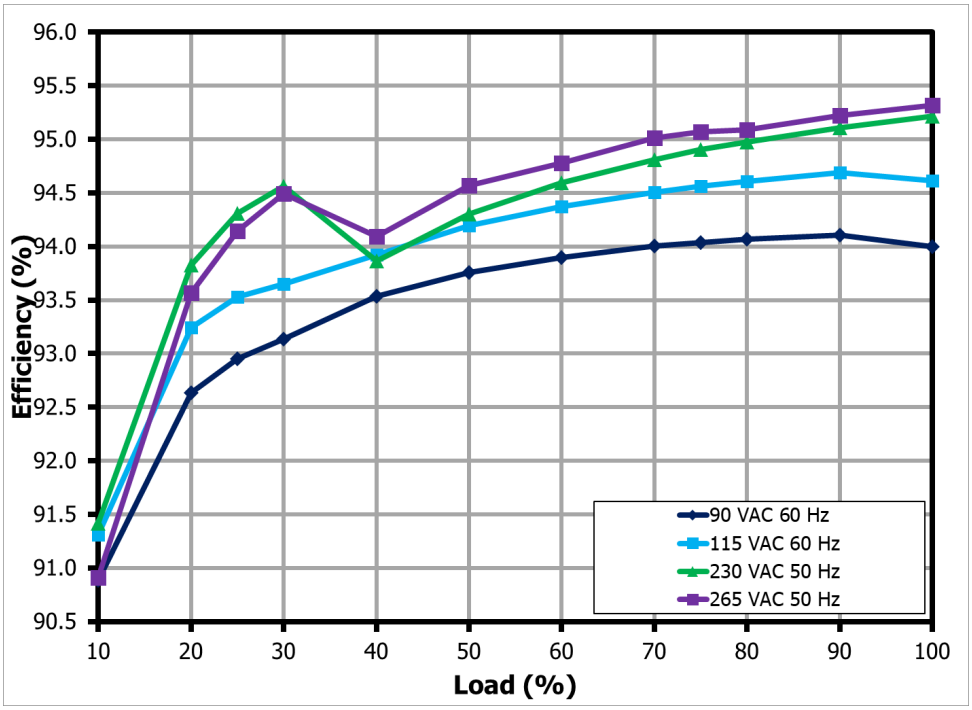


Figure 48 – Efficiency vs. Output Load for 28 V Output, Room Temperature.

15.8 Efficiency Comparison with Diode Bridge Rectifier

The active bridge assembly was removed and replaced with a GBU8K diode bridge rectifier. The difference in full-load efficiency at the lowest input voltage is 0.63% and 0.16% at the highest input voltage.

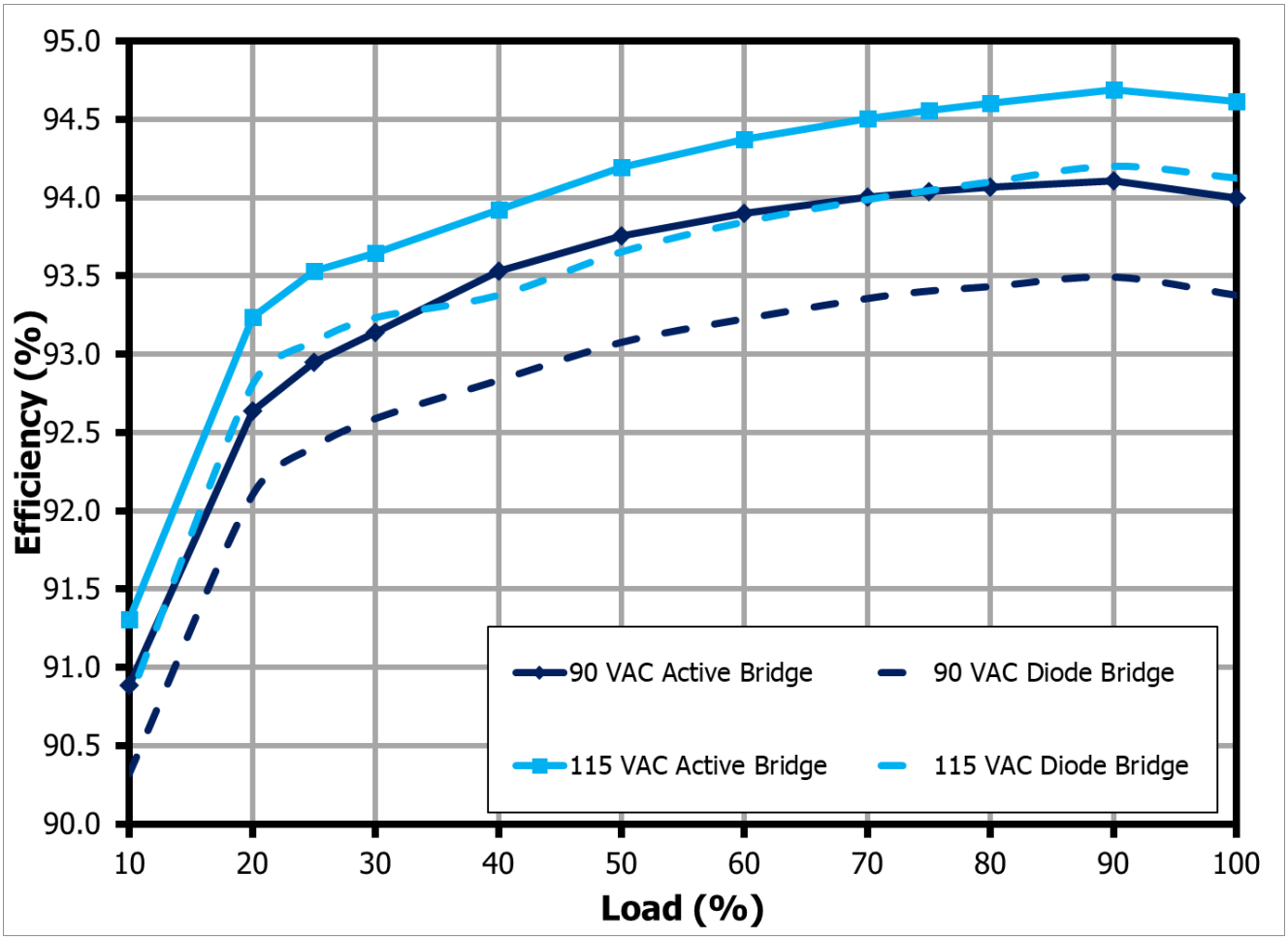


Figure 49 – Active Bridge and Diode Bridge Comparison, Efficiency vs. Output Load for 28 V Output, Low Line.

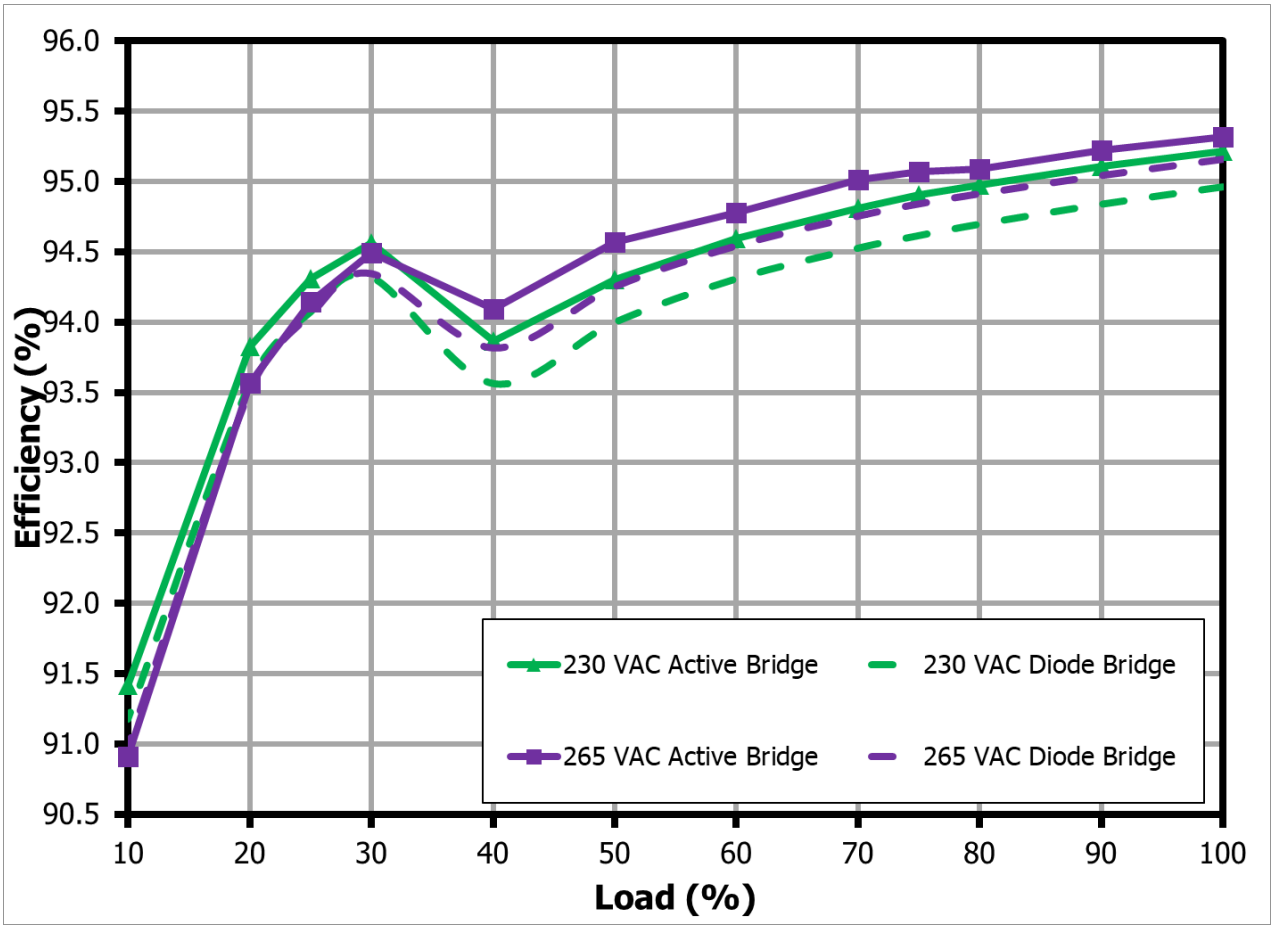


Figure 50 – Active Bridge and Diode Bridge Comparison, Efficiency vs. Output Load for 28 V Output, High Line.

16 Thermal Performance

Thermal performance is measured at ambient temperature. Thermal performance is tested inside an acrylic box with natural convection. The unit was left running for 1 hour in each test condition to let the component temperatures stabilize before taking the measurements.

16.1 Thermal Test Scan - Open Frame Unit

DUT (open frame) is placed inside an acrylic housing to reduce the effect of airflow. Component's case temperature is measured using an IR camera.

Figure 51 – Thermal Image at 90 VAC, 28 V 5 A (Left: Bottom view, Right: Top View).

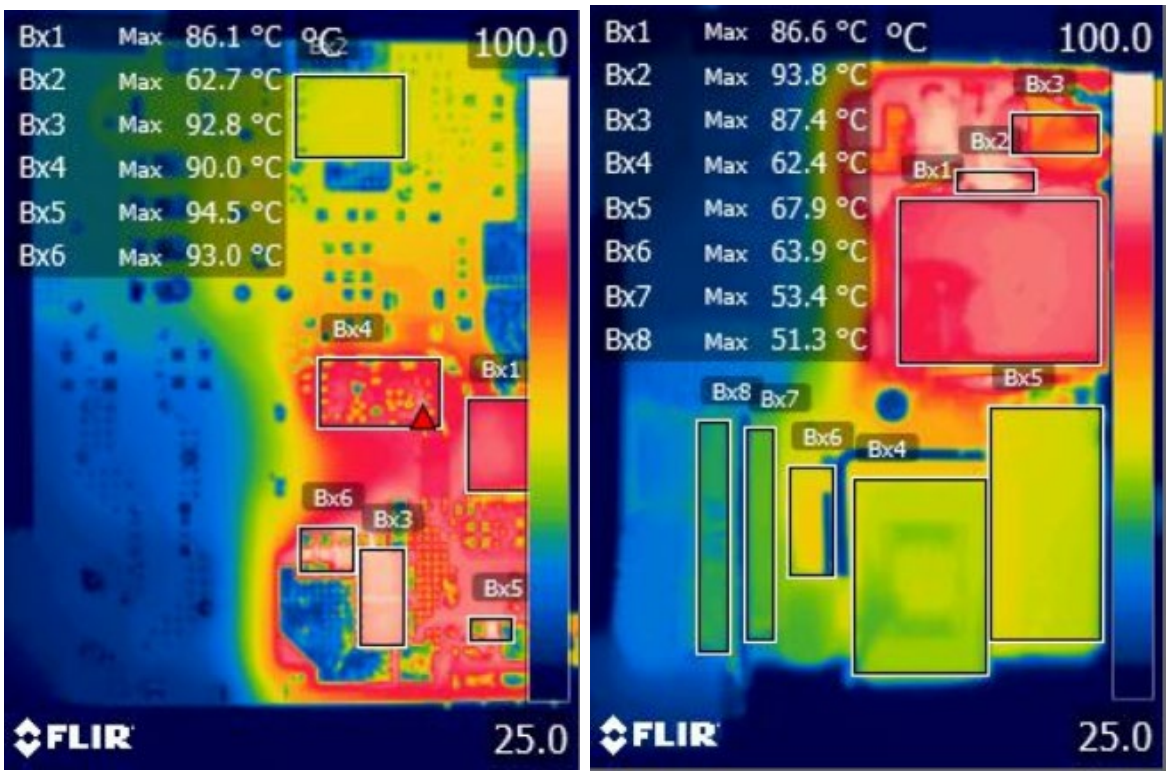


Figure 52 – Thermal Image at 90 VAC, 28 V 5 A (Left: Bottom view, Right: Top View).

Part			Temperature (°C)	
Ref Des	**Description**	**Thermal Image**	**90 VAC**	**265 VAC**
U102	InnoSwitch5-Pro	Bottom, Bx1	95.6	86.1
U100	HiperPFS-5	Bottom, Bx2	80.5	62.7
Q100, Q101	SR FETs	Bottom, Bx3	96.2	92.8
Q102, Q103	Primary Bias Components	Bottom, Bx4	99.1	90
R124	Rsense	Bottom, Bx5	98.2	94.5
C116, R119 R120, D102	Secondary Snubber	Bottom, Bx6	94.8	93
T101	Flyback Core	Top, Bx1	92.1	86.6
T101	Flyback Winding	Top, Bx2	99.2	93.8
C113	Output Capacitors	Top, Bx3	90.6	87.4
C114	PFC Choke	Top, Bx4	79.7	62.4
C104	Bulk Capacitor	Top, Bx5	84.6	67.9
D101	Boost Diode	Top, Bx6	85	63.9
BR200	Diode Bridge	Top, Bx7	83.4	53.4
Q200, Q201	Active Bridge FETs	Top, Bx8	79.2	51.3

17 Waveforms

Note: Measurements taken at room temperature

17.1 Start-up Waveforms

17.1.1 Output Voltage and Current

Note: Output voltages captured on the board at output connector

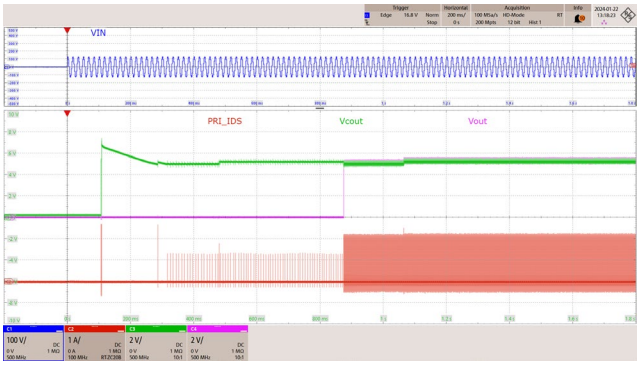


Figure 53 – Output Voltage at Start-up.
90 VAC, 5 V, 3 A Load.
C1: V_{IN}, 100 V / div.
C2: Primary I_{DS}, 1 A / div.
C3: V_{COUT}, 2 V / div.
C4: V_{OUT}, 2 V / div.
Time: 200 ms / div.

Figure 54 – Output Voltage at Start-up.
265 VAC, 5 V, 3 A Load.
C1: V_{IN}, 100 V / div.
C2: Primary I_{DS}, 1 A / div.
C3: V_{COUT}, 2 V / div.
C4: V_{OUT}, 2 V / div.
Time: 200 ms / div.

17.1.2 InnoSwitch5-Pro Drain Voltage and Current at Start-up

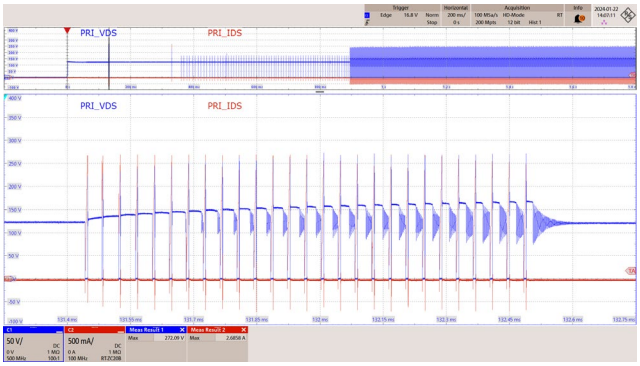


Figure 55 – InnoSwitch5-Pro Drain Voltage and Current at Start-up.
90 VAC, 5 V, 3 A Load.
C1: Primary V_{DS}, 50 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 150 µs / div.
Maximum Primary V_{DS} = 272 V.

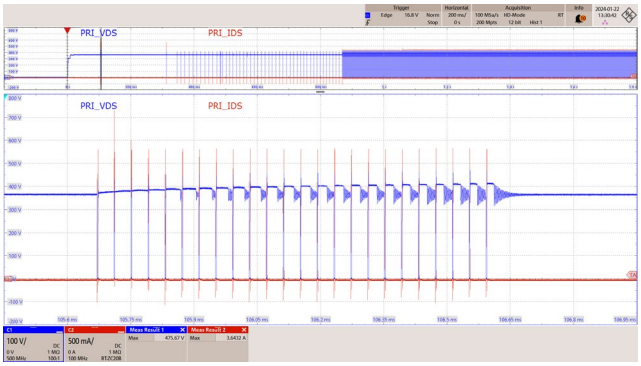


Figure 56 – InnoSwitch5-Pro Drain Voltage and Current at Start-up.
265 VAC, 5 V, 3 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 150 µs / div.
Maximum Primary V_{DS} = 475 V.

17.1.3 SR FET Drain and Gate Voltage at Start-up

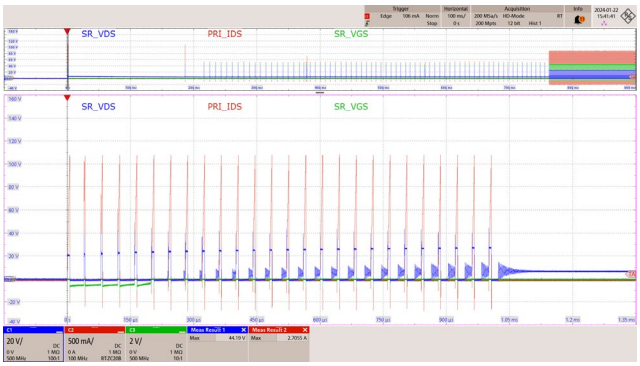


Figure 57 – SR FET Drain and Gate Voltage at Start-up.
90 VAC, 5 V, 3 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 150 µs / div.
Maximum SR V_{DS} = 44 V.

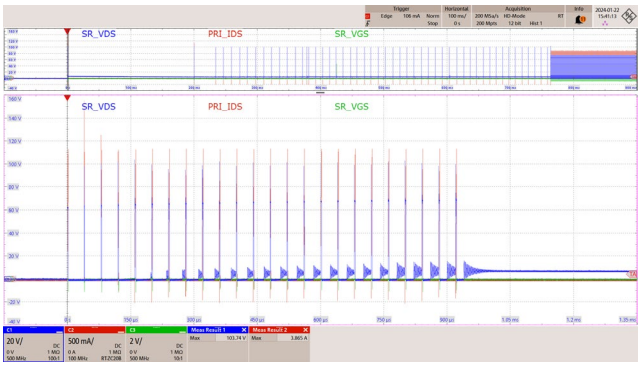


Figure 58 – SR FET Drain and Gate Voltage at Start-up.
265 VAC, 5 V, 3 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 150 µs / div.
Maximum SR V_{DS} = 104 V.

17.1.4 HiperPFS-5 Drain Voltage and Current at Start-up

At start-up, PFC is disabled.

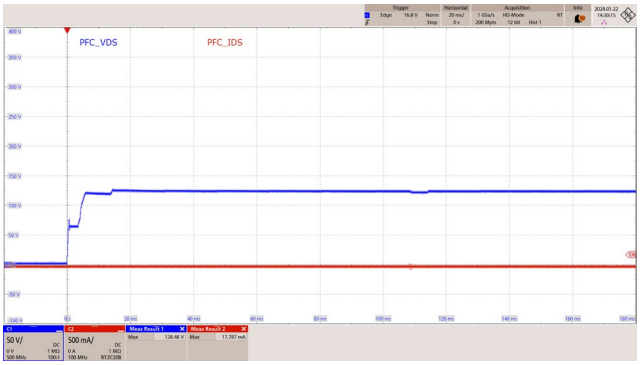


Figure 59 – HiperPFS-5 Drain Voltage and Current.
90 VAC, 5 V, 3 A Load.
C1: PFC V_{DS}, 50 V / div.
C2: PFC I_{DS}, 500 mA / div.
Time: 20 ms / div.

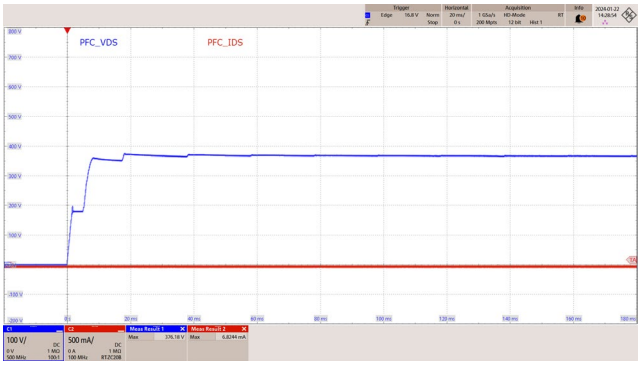


Figure 60 – HiperPFS-5 Drain Voltage and Current.
265 VAC, 5 V, 3 A Load.
C1: PFC V_{DS}, 100 V / div.
C2: PFC I_{DS}, 500 mA / div.
Time: 20 ms / div.

17.2 Load Transient Response

Note: Output voltage waveforms are captured at the end of the PC board. Load setting is as follows: 0% - 100% load current step, 2.5 Hz, 50% duty cycle, slew rate of 150 mA / µs.

17.2.1 Output: 5 V / 3 A

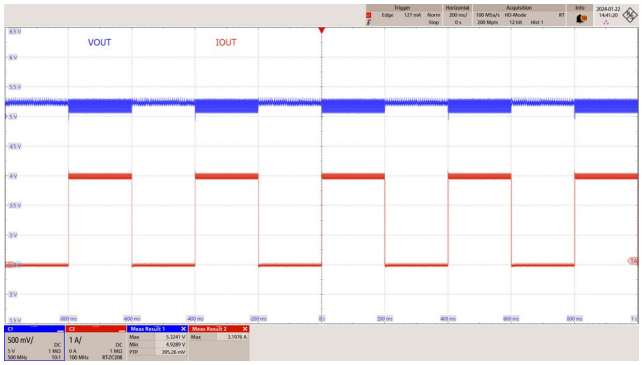


Figure 61 – Transient Response.
90 VAC, 5 V, 0% – 100% Load Step.
V_{MIN}: 4.929 V, V_{MAX}: 5.324 V.
C1: V_{OUT}, 500 mV / div.
C2: I_{OUT}, 1 A / div.
Time: 200 ms / div.

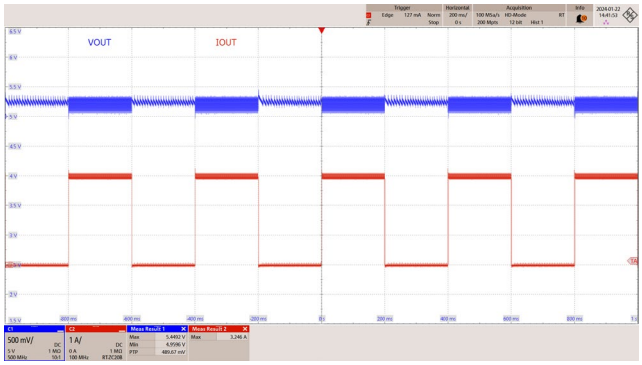


Figure 62 – Transient Response.
265 VAC, 5 V, 0% – 100% Load Step.
V_{MIN}: 4.960 V, V_{MAX}: 5.449 V.
C1: V_{OUT}, 500 mV / div.
C2: I_{OUT}, 1 A / div.
Time: 200 ms / div.

17.2.2 Output: 9 V / 3 A

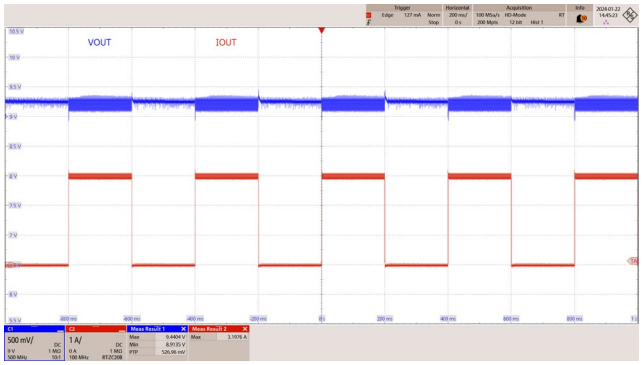


Figure 63 – Transient Response.
90 VAC, 9 V, 0% – 100% Load Step.
V_{MIN}: 8.914 V, V_{MAX}: 9.44 V.
C1: V_{OUT}, 500 mV / div.
C2: I_{OUT}, 1 A / div.
Time: 200 ms / div.

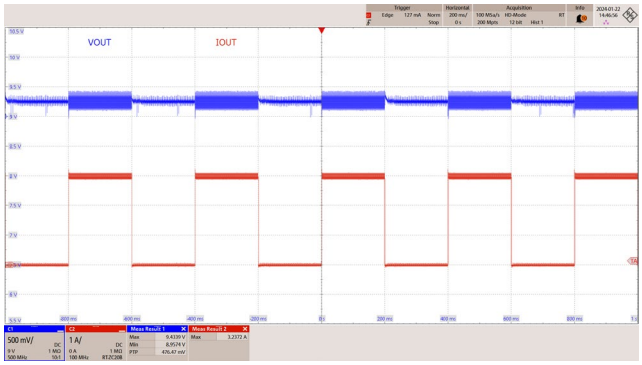


Figure 64 – Transient Response.
265 VAC, 9 V, 0% – 100% Load Step.
V_{MIN}: 8.957 V, V_{MAX}: 9.434V.
C1: V_{OUT}, 500 mV / div.
C2: I_{OUT}, 1 A / div.
Time: 200 ms / div.

17.2.3 Output: 12 V / 5 A

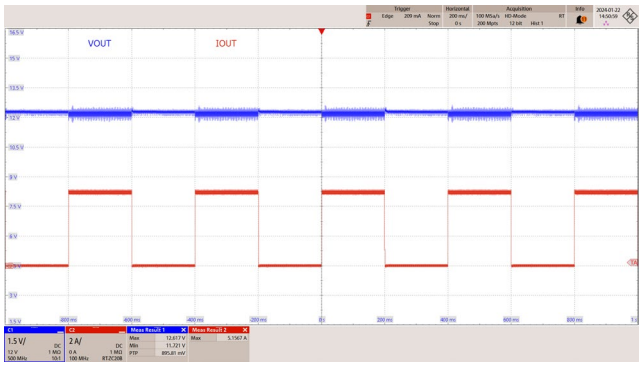


Figure 65 – Transient Response.
90 VAC, 12 V, 0% – 100% Load Step.
V_{MIN}: 11.721 V, V_{MAX}: 12.617 V.
C1: V_{OUT}, 1.5 V / div.
C2: I_{OUT}, 2 A / div.
Time: 200 ms / div.

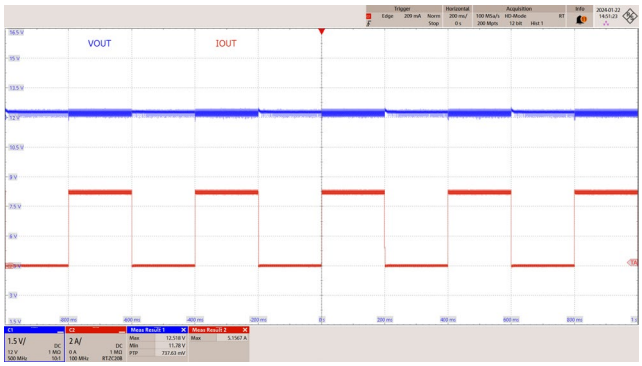


Figure 66 – Transient Response.
265 VAC, 12 V, 0% – 100% Load Step.
V_{MIN}: 11.78 V, V_{MAX}: 12.518 V.
C1: V_{OUT}, 1.5 V / div.
C2: I_{OUT}, 2 A / div.
Time: 200 ms / div.

17.2.4 Output: 15 V / 5 A

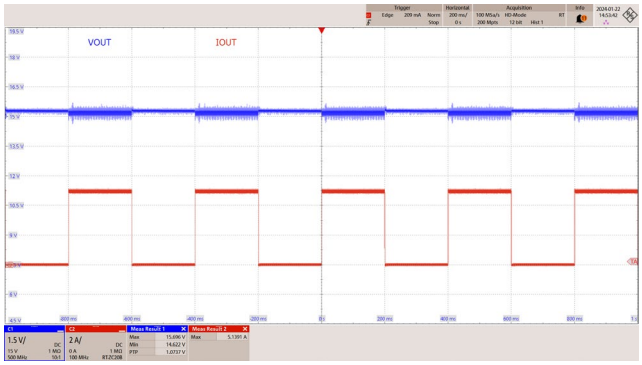


Figure 67 – Transient Response.
90 VAC, 15 V, 0% – 100% Load Step.
V_{MIN}: 14.622 V, V_{MAX}: 15.696 V.
C1: V_{OUT}, 1.5 V / div.
C2: I_{OUT}, 2 A / div.
Time: 200 ms / div.

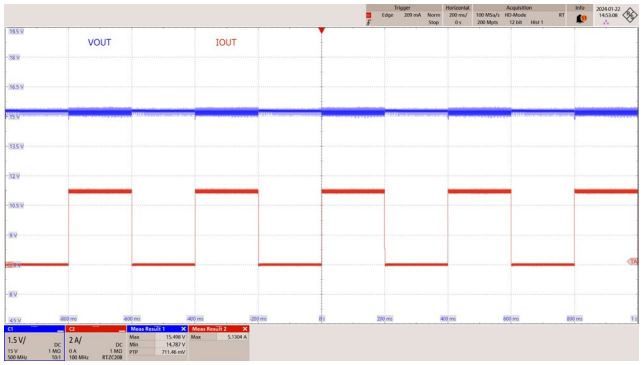


Figure 68 – Transient Response.
265 VAC, 15 V, 0% – 100% Load Step.
V_{MIN}: 14.787 V, V_{MAX}: 15.498 V.
C1: V_{OUT}, 1.5 V / div.
C2: I_{OUT}, 2 A / div.
Time: 200 ms / div.

17.2.5 Output: 20 V / 5 A

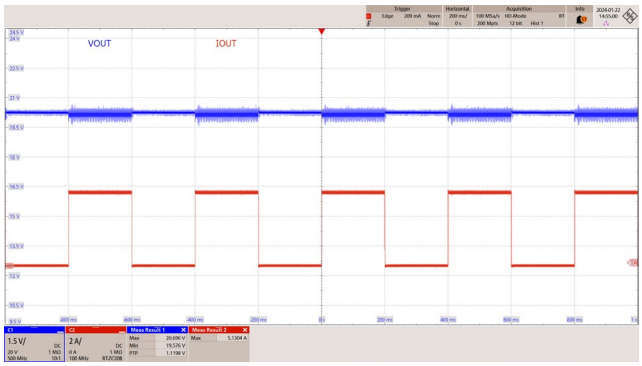


Figure 69 – Transient Response.
90 VAC, 20 V, 0% – 100% Load Step.
V_{MIN}: 19.576 V, V_{MAX}: 20.696 V.
C1: V_{OUT}, 1.5 V / div.
C2: I_{OUT}, 2 A / div.
Time: 200 ms / div.

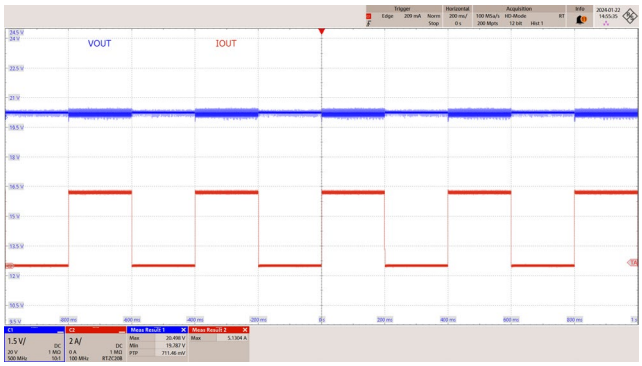


Figure 70 – Transient Response.
265 VAC, 20 V, 0% – 100% Load Step.
V_{MIN}: 19.787 V, V_{MAX}: 20.498 V.
C1: V_{OUT}, 1.5 V / div.
C2: I_{OUT}, 2 A / div.
Time: 200 ms / div.

17.2.6 Output: 28 V / 5 A

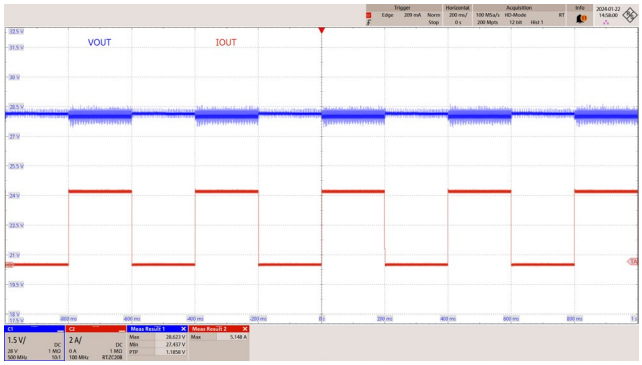


Figure 71 – Transient Response.
90 VAC, 28 V, 0% – 100% Load Step.
V_{MIN}: 27.437 V, V_{MAX}: 28.623 V.
C1: V_{OUT}, 1.5 V / div.
C2: I_{OUT}, 2 A / div.
Time: 200 ms / div.

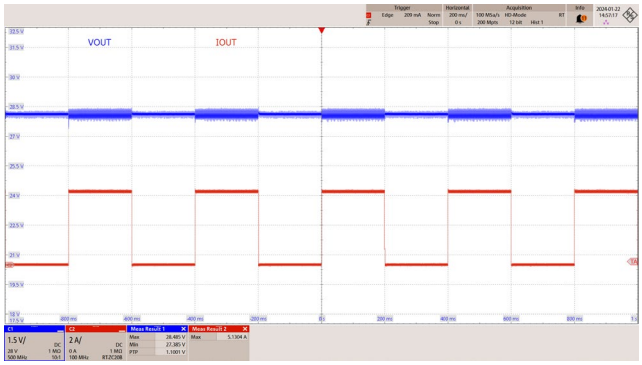


Figure 72 – Transient Response.
265 VAC, 28 V, 0% – 100% Load Step.
V_{MIN}: 27.385 V, V_{MAX}: 28.485 V.
C1: V_{OUT}, 1.5 V / div.
C2: I_{OUT}, 2 A / div.
Time: 200 ms / div.

17.3 InnoSwitch5-Pro Drain Voltage and Current (Steady-State)

17.3.1 Output: 5 V / 3 A

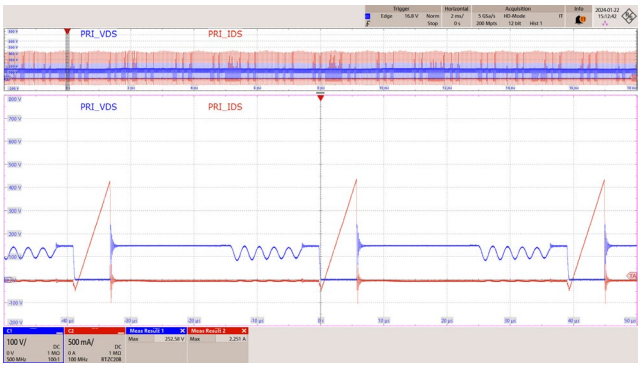


Figure 73 – InnoSwitch5-Pro Drain Voltage and Current.
90 VAC, 5 V, 3 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 253 V.

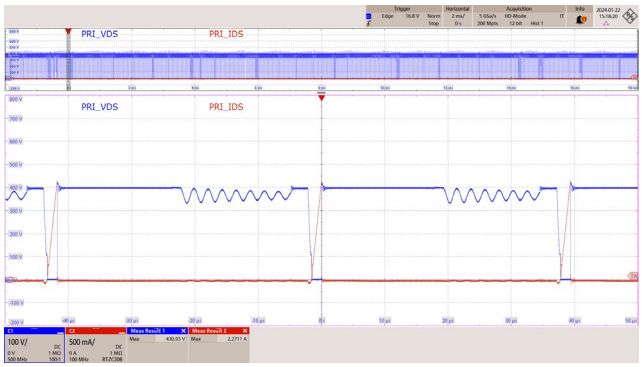


Figure 74 – InnoSwitch5-Pro Drain Voltage and Current.
265 VAC, 5 V, 3 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 431 V.

17.3.2 Output: 9 V / 3 A

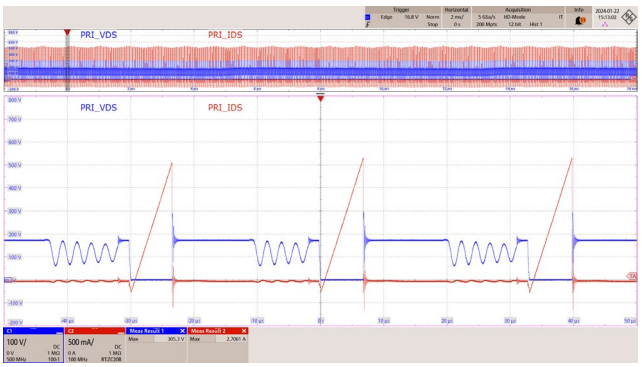


Figure 75 – InnoSwitch5-Pro Drain Voltage and Current.
90 VAC, 9 V, 3 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 305 V.

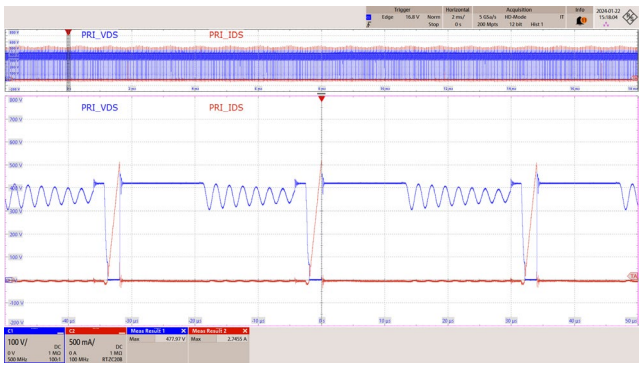


Figure 76 – InnoSwitch5-Pro Drain Voltage and Current.
265 VAC, 9 V, 3 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 478 V.

17.3.3 Output: 12 V / 5 A

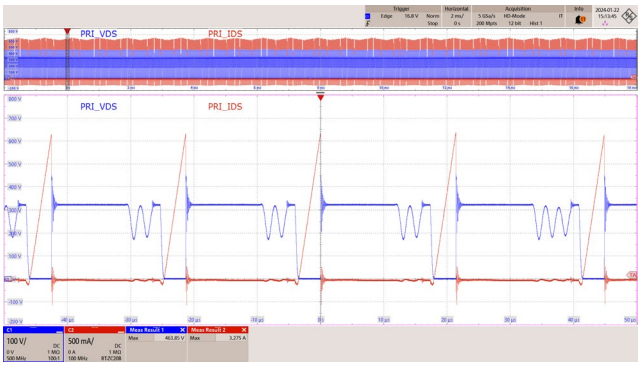


Figure 77 – InnoSwitch5-Pro Drain Voltage and Current.
90 VAC, 12 V, 5 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 464 V.

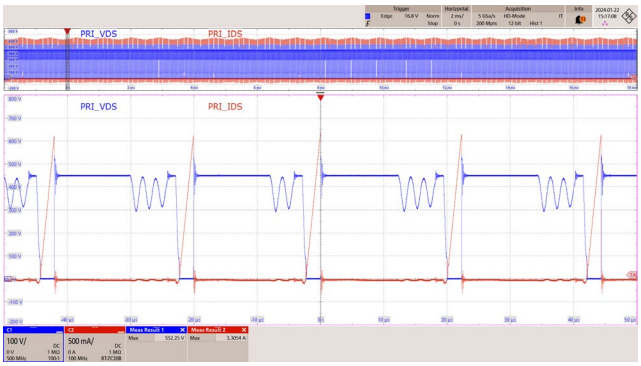


Figure 78 – InnoSwitch5-Pro Drain Voltage and Current.
265 VAC, 12 V, 5 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 552 V.

17.3.4 Output: 15 V / 5 A

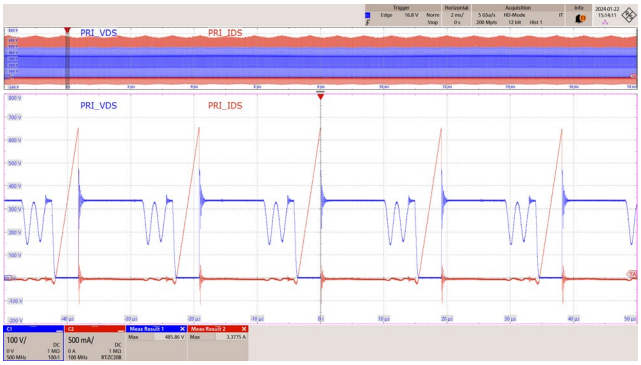


Figure 79 – InnoSwitch5-Pro Drain Voltage and Current.
90 VAC, 15 V, 5 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 486 V.

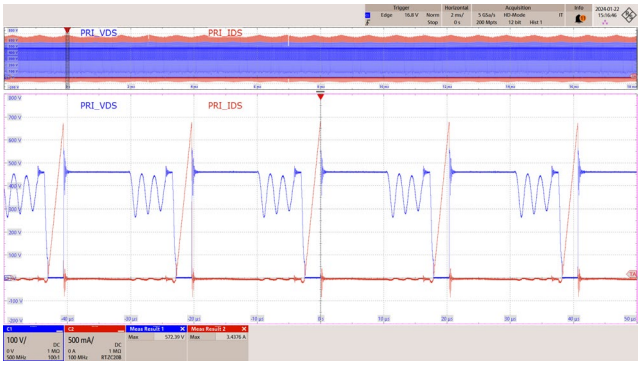


Figure 80 – InnoSwitch5-Pro Drain Voltage and Current.
265 VAC, 15 V, 5 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 572 V.

17.3.5 Output: 20 V / 5 A

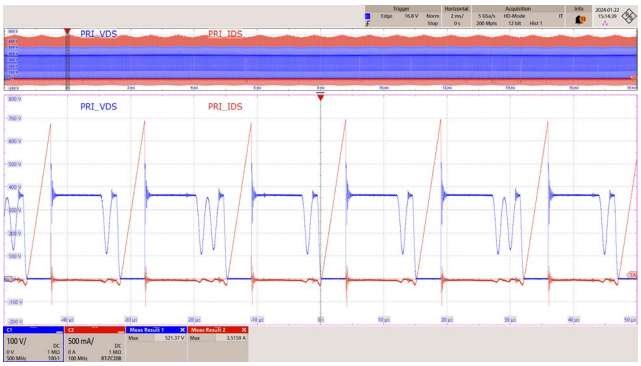


Figure 81 – InnoSwitch5-Pro Drain Voltage and Current.
90 VAC, 20 V, 5 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 521 V.

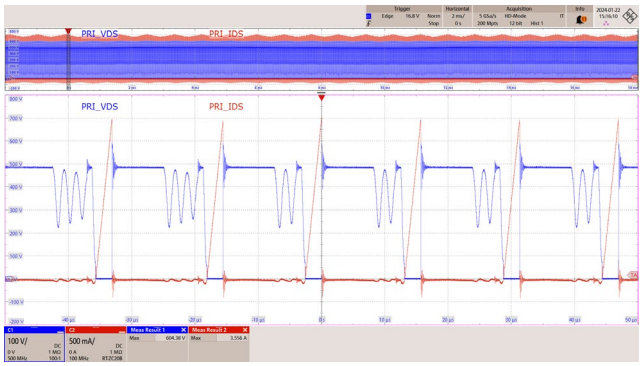


Figure 82 – InnoSwitch5-Pro Drain Voltage and Current.
265 VAC, 20 V, 5 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 604 V.

17.3.6 Output: 28 V / 5 A

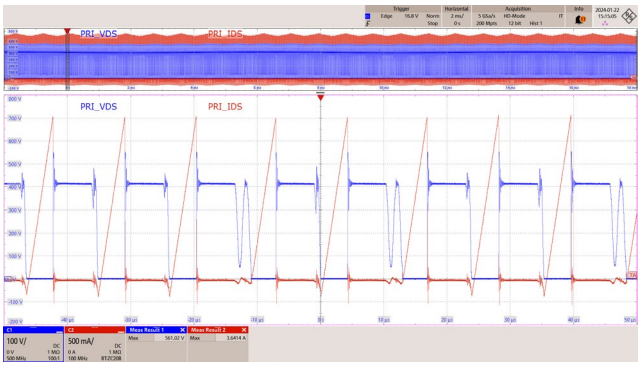


Figure 83 – InnoSwitch5-Pro Drain Voltage and Current.
90 VAC, 28 V, 5 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 561 V.

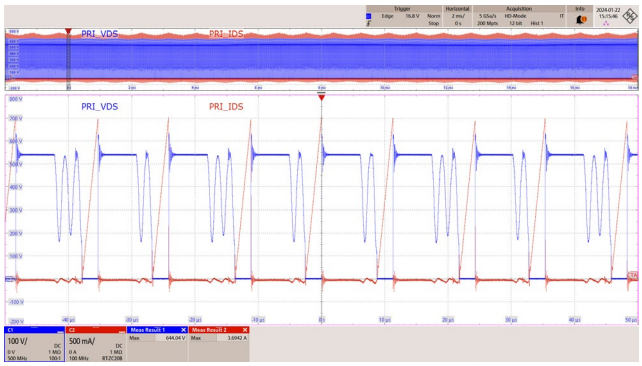


Figure 84 – InnoSwitch5-Pro Drain Voltage and Current.
265 VAC, 28 V, 5 A Load.
C1: Primary V_{DS}, 100 V / div.
C2: Primary I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum Primary V_{DS} = 644 V.

17.4 SR FET Drain and Gate Voltage (Steady-State)

17.4.1 Output: 5 V / 3 A

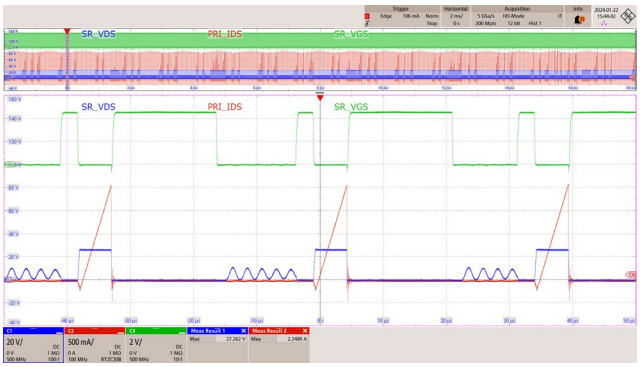


Figure 85 – SR FET Drain and Gate Voltage.
90 VAC, 5 V, 3 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 27 V.

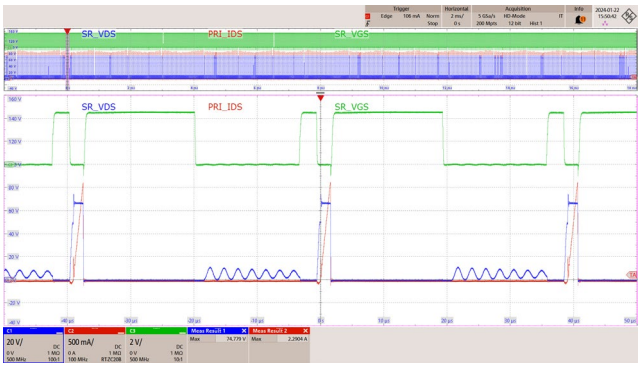


Figure 86 – SR FET Drain and Gate Voltage.
265 VAC, 5 V, 3 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 75 V.

17.4.2 Output: 9 V / 3 A

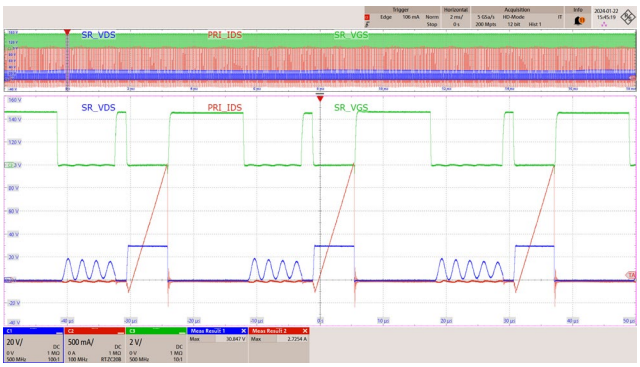


Figure 87 – SR FET Drain and Gate Voltage.
90 VAC, 9 V, 3 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 31 V.

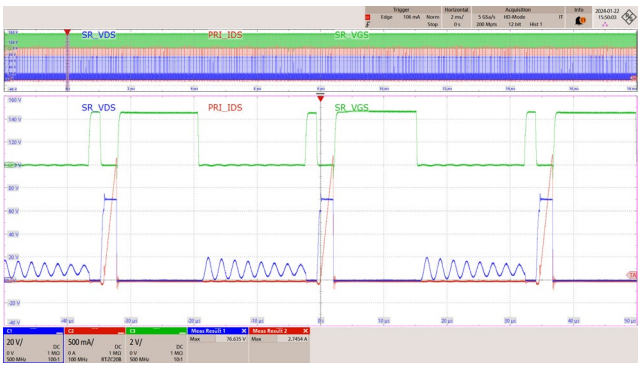


Figure 88 – SR FET Drain and Gate Voltage.
265 VAC, 9 V, 3 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 77 V.

17.4.3 Output: 12 V / 5 A

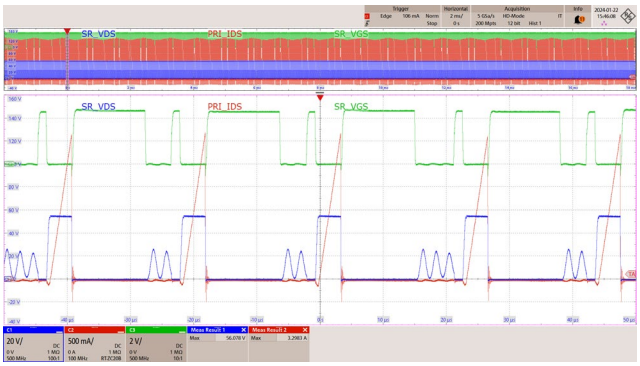


Figure 89 – SR FET Drain and Gate Voltage.
90 VAC, 12 V, 5 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 56 V.

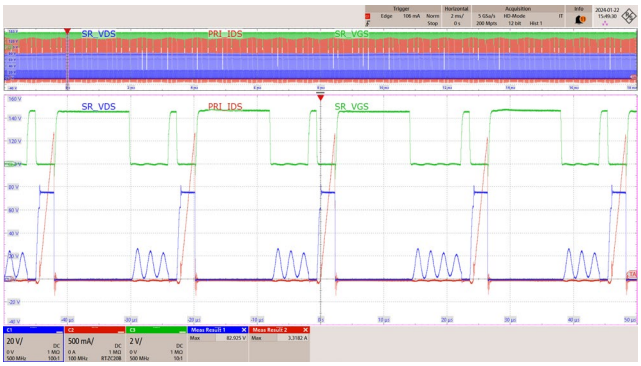


Figure 90 – SR FET Drain and Gate Voltage.
265 VAC, 12 V, 5 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 83 V.

17.4.4 Output: 15 V / 5 A

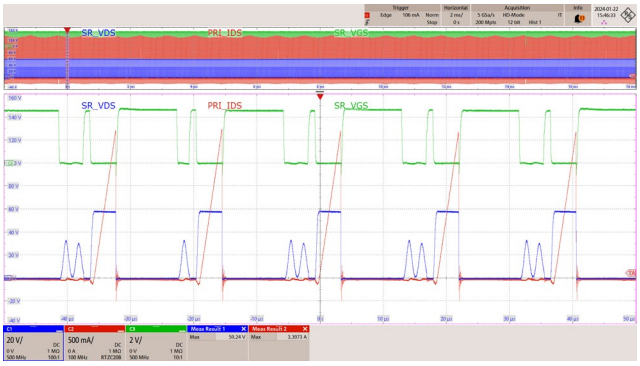


Figure 91 – SR FET Drain and Gate Voltage.
90 VAC, 15 V, 5 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 59 V.

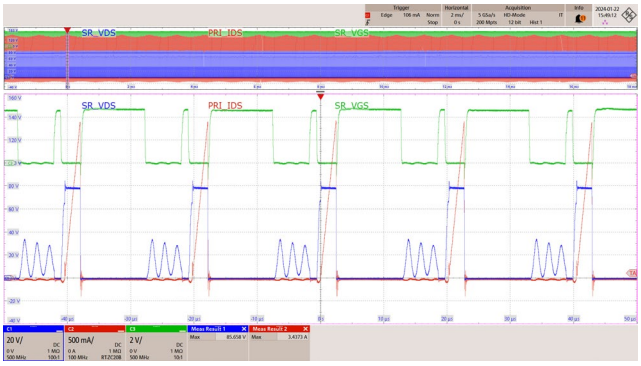


Figure 92 – SR FET Drain and Gate Voltage.
265 VAC, 15 V, 5 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 86 V.

17.4.5 Output: 20 V / 5 A

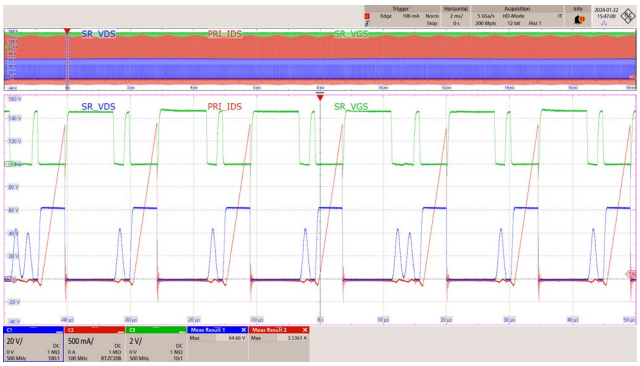


Figure 93 – SR FET Drain and Gate Voltage.
90 VAC, 20 V, 5 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 65 V.

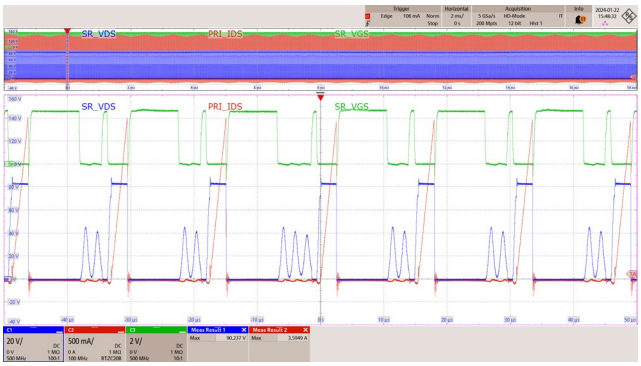


Figure 94 – SR FET Drain and Gate Voltage.
265 VAC, 20 V, 5 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 90 V.

17.4.6 Output: 28 V / 5 A

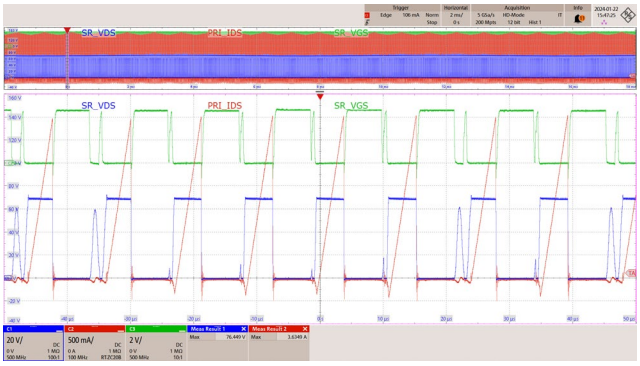


Figure 95 – SR FET Drain and Gate Voltage.
90 VAC, 28 V, 5 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 76 V.

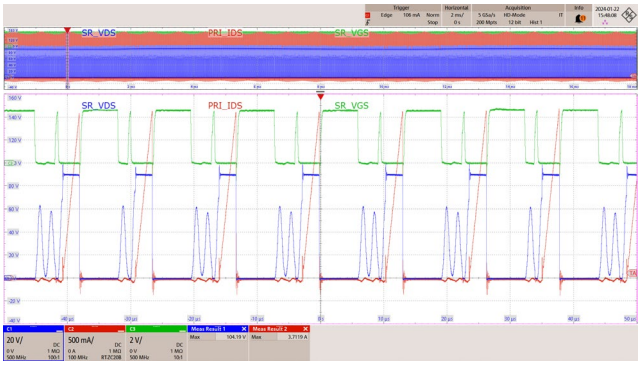


Figure 96 – SR FET Drain and Gate Voltage.
265 VAC, 28 V, 5 A Load.
C1: SR V_{DS}, 20 V / div.
C2: Primary I_{DS}, 500 mA / div.
C13: SR V_{GS}, 2 V / div.
Time (Zoom): 10 µs / div.
Maximum SR V_{DS} = 104 V.

17.5 HiperPFS-5 Drain Voltage and Current (Steady-State)

PFC is disabled at 9 V and 5 V Output.

17.5.1 Output: 12 V / 5 A

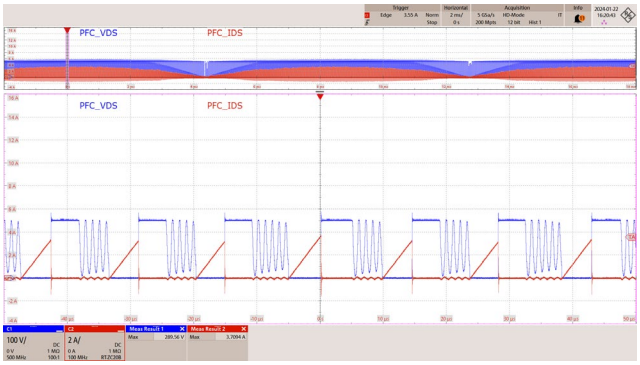


Figure 97 – HiperPFS-5 Drain Voltage and Current.
90 VAC, 12 V, 5 A Load.
C1: PFC V_{DS}, 100 V / div.
C2: PFC I_{DS}, 2 A / div.
Time (Zoom): 10 µs / div.
Maximum PFC VDS = 290 V.

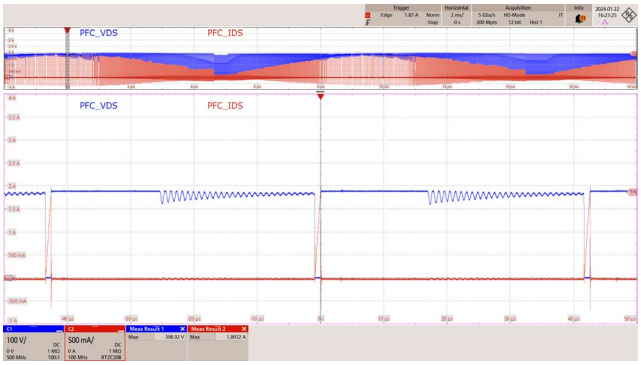


Figure 98 – HiperPFS-5 Drain Voltage and Current.
265 VAC, 12 V, 5 A Load.
C1: PFC V_{DS}, 100 V / div.
C2: PFC I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum PFC VDS = 399 V.

17.5.2 Output: 15 V / 5 A

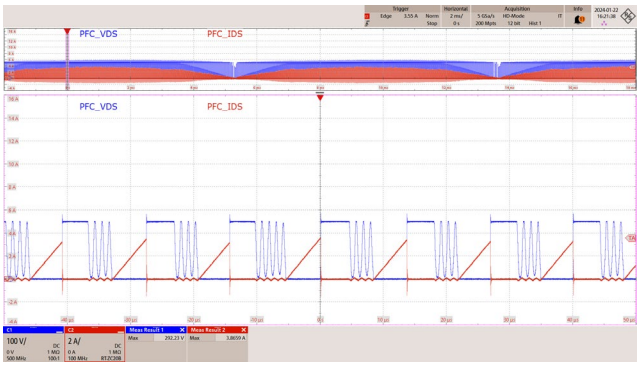


Figure 99 – HiperPFS-5 Drain Voltage and Current.
90 VAC, 15 V, 5 A Load.
C1: PFC V_{DS}, 100 V / div.
C2: PFC I_{DS}, 2 A / div.
Time (Zoom): 10 µs / div.
Maximum PFC VDS = 292 V.

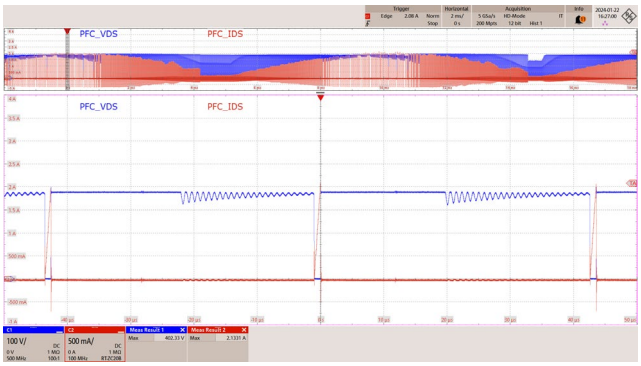


Figure 100 – HiperPFS-5 Drain Voltage and Current.
265 VAC, 15 V, 5 A Load.
C1: PFC V_{DS}, 100 V / div.
C2: PFC I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum PFC VDS = 402 V.

17.5.3 Output: 20 V / 5 A

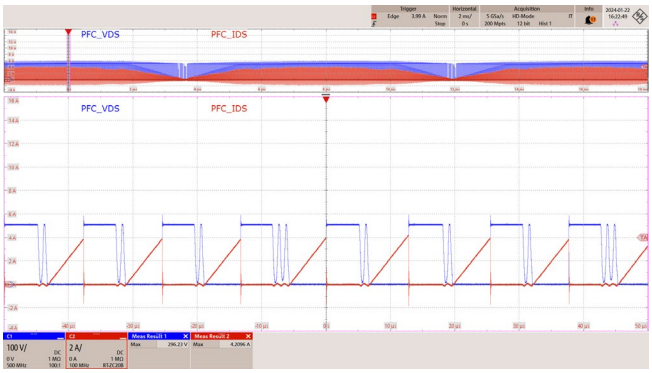


Figure 101 – HiperPFS-5 Drain Voltage and Current.
90 VAC, 20 V, 5 A Load.
C1: PFC V_{DS}, 100 V / div.
C2: PFC I_{DS}, 2 A / div.
Time (Zoom): 10 µs / div.
Maximum PFC VDS = 296 V.

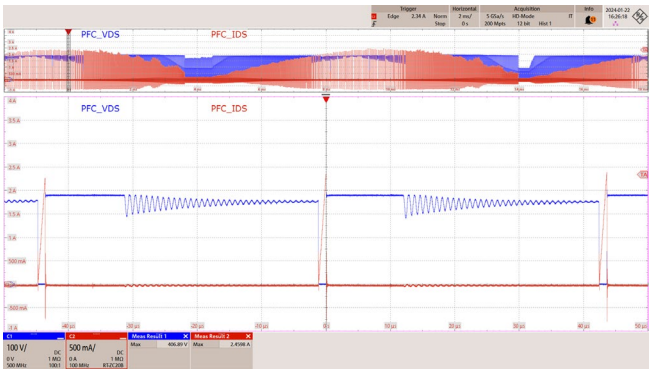


Figure 102 – HiperPFS-5 Drain Voltage and Current.
265 VAC, 20 V, 5 A Load.
C1: PFC V_{DS}, 100 V / div.
C2: PFC I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum PFC VDS = 407 V.

17.5.4 Output: 28 V / 5 A

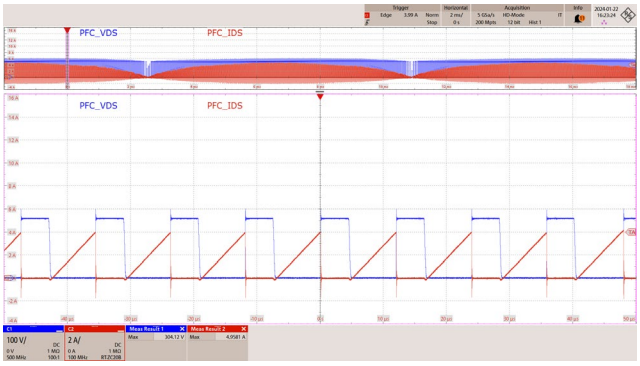


Figure 103 – HiperPFS-5 Drain Voltage and Current.
90 VAC, 20 V, 5 A Load.
C1: PFC V_{DS}, 100 V / div.
C2: PFC I_{DS}, 2 A / div.
Time (Zoom): 10 µs / div.
Maximum PFC VDS = 304 V.

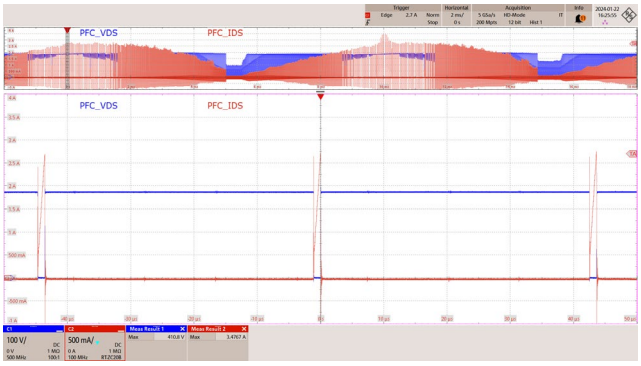


Figure 104 – HiperPFS-5 Drain Voltage and Current.
265 VAC, 20 V, 5 A Load.
C1: PFC V_{DS}, 100 V / div.
C2: PFC I_{DS}, 500 mA / div.
Time (Zoom): 10 µs / div.
Maximum PFC VDS = 411 V.

18 Output Ripple Measurements

18.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

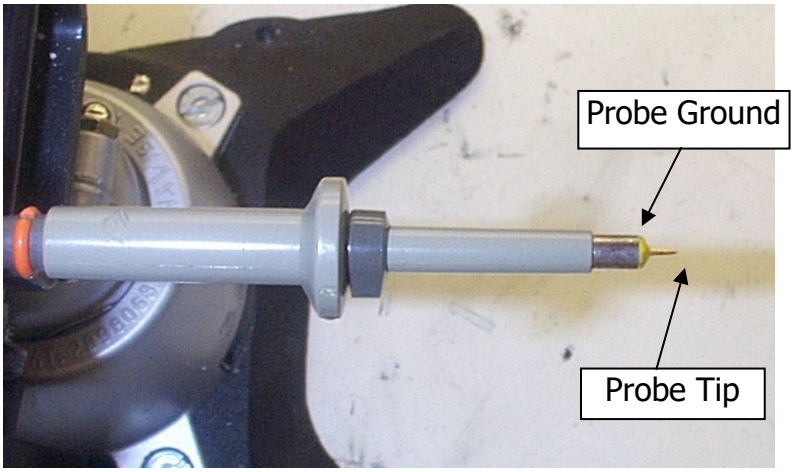


Figure 105 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

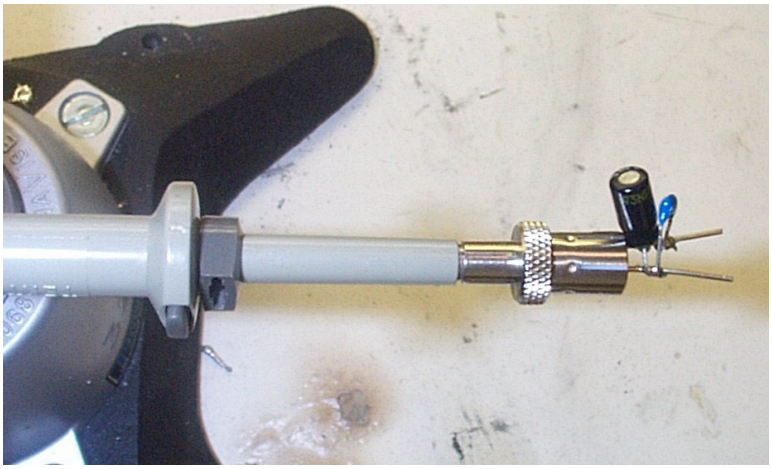


Figure 106 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added).

18.2 Output Voltage Ripple vs. Load

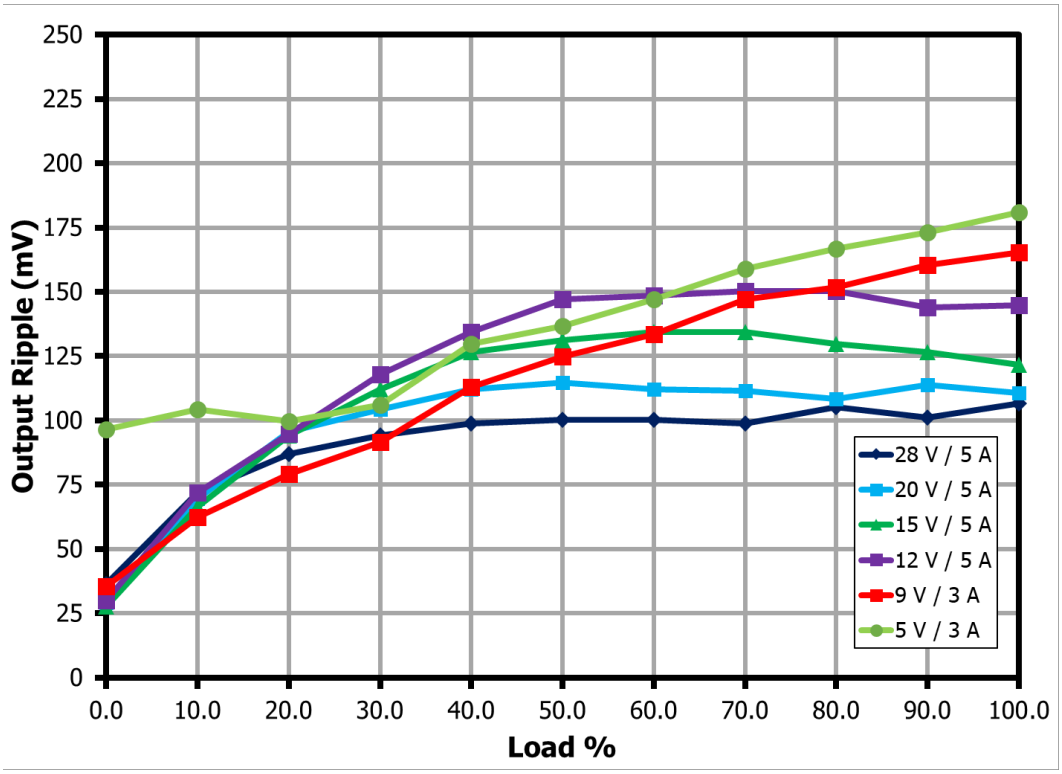


Figure 107 – Output Voltage Ripple vs. Load, 90 VAC.

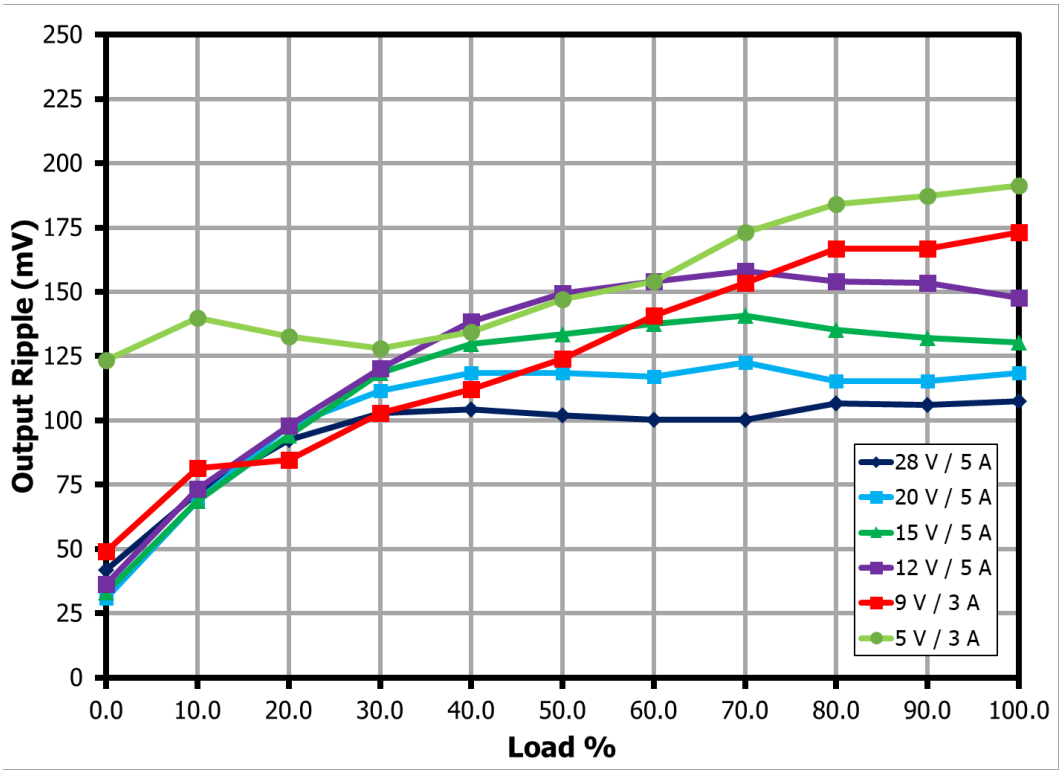


Figure 108 – Output Voltage Ripple vs. Load, 265 VAC.

18.3 Output Voltage Ripple Waveforms

Note 1: Output voltage ripple waveforms are captured at the end of the cable.
2: Measurements taken at room temperature (approximately 25 °C)

18.3.1 Output: 5 V / 3 A

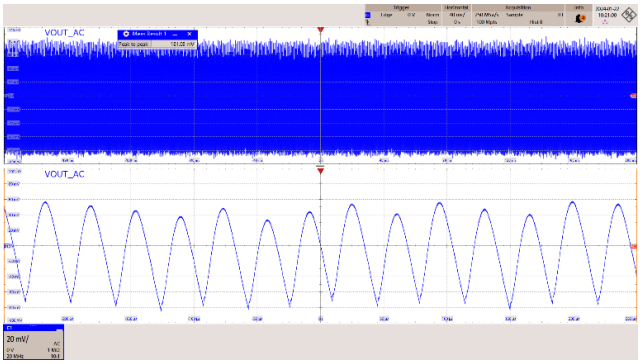


Figure 109 – Output Voltage Ripple.
90 VAC, 5 V, 3 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 181 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

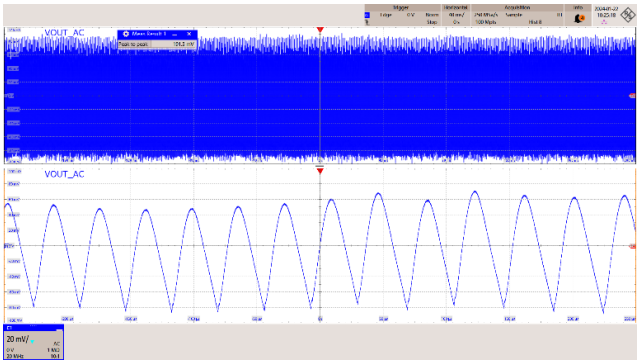


Figure 110 – Output Voltage Ripple.
265 VAC, 5 V, 3 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 191 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

18.3.2 Output: 9 V / 3 A

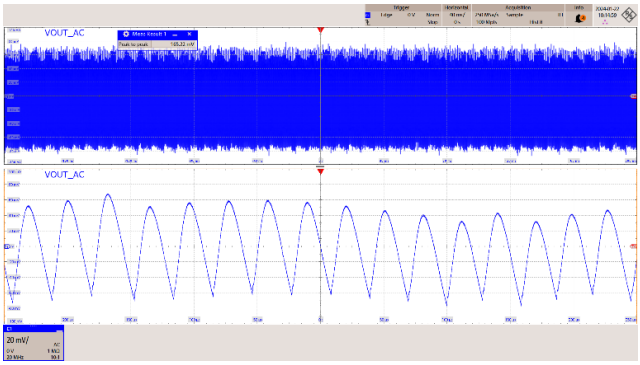


Figure 111 – Output Voltage Ripple.
90 VAC, 9 V, 3 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 165 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

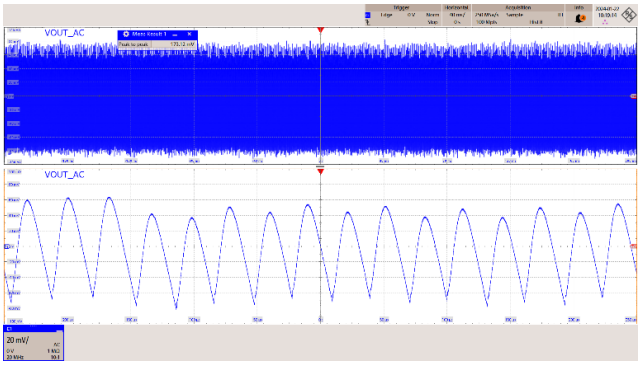


Figure 112 – Output Voltage Ripple.
265 VAC, 5 V, 3 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 173 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

18.3.3 Output: 12 V / 5 A

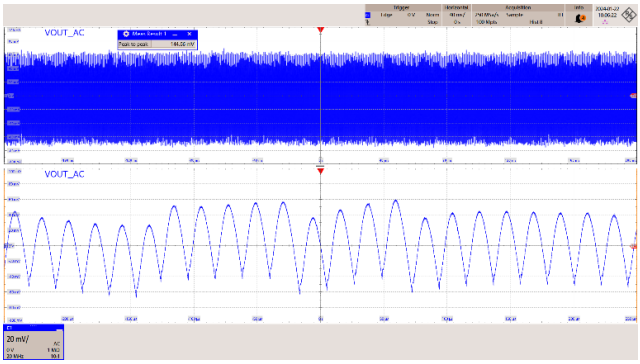


Figure 113 – Output Voltage Ripple.
90 VAC, 12 V, 5 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 145 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

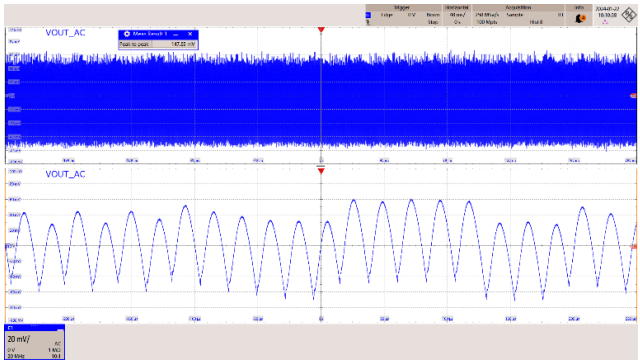


Figure 114 – Output Voltage Ripple.
265 VAC, 12 V, 5 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 148 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

18.3.4 Output: 15 V / 5 A

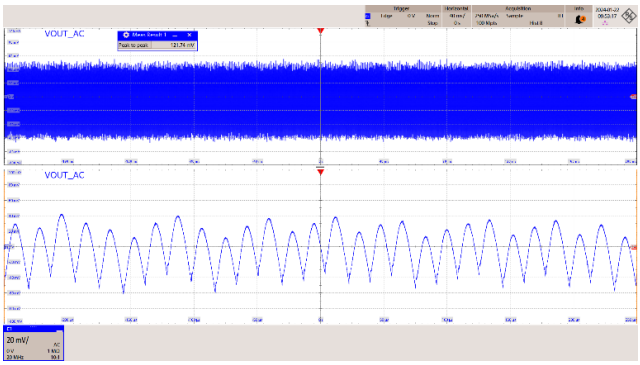


Figure 115 – Output Voltage Ripple.
90 VAC, 15 V, 5 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 122 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

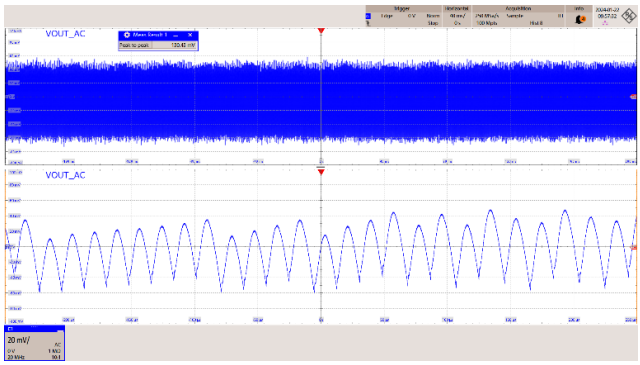


Figure 116 – Output Voltage Ripple.
265 VAC, 15 V, 5 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 130 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

18.3.5 Output: 20 V / 5 A

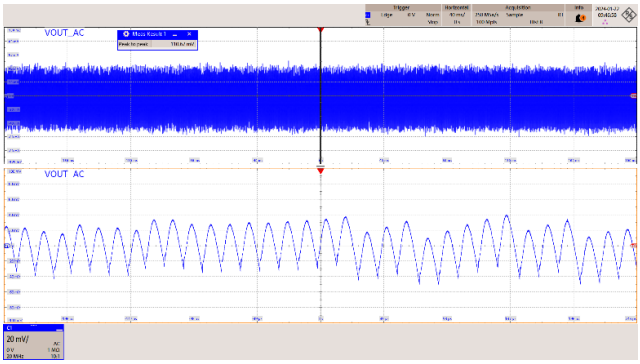


Figure 117 – Output Voltage Ripple.
90 VAC, 20 V, 5 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 111 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

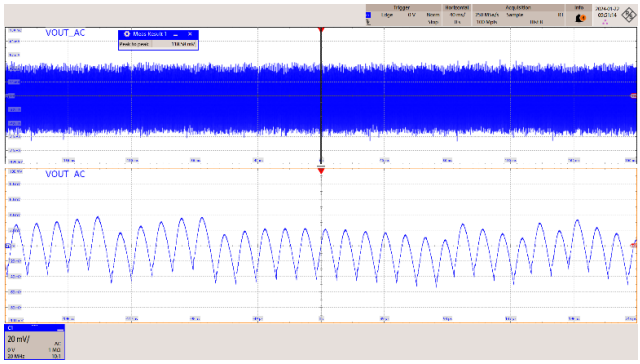


Figure 118 – Output Voltage Ripple.
265 VAC, 20 V, 5 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 119 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

18.3.6 Output: 28 V / 5 A

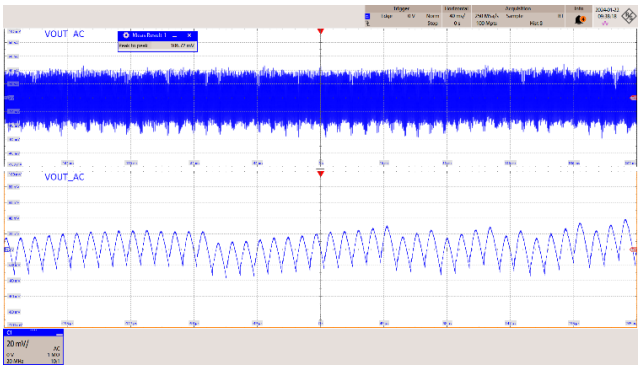


Figure 119 – Output Voltage Ripple.
90 VAC, 28 V, 5 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 107 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

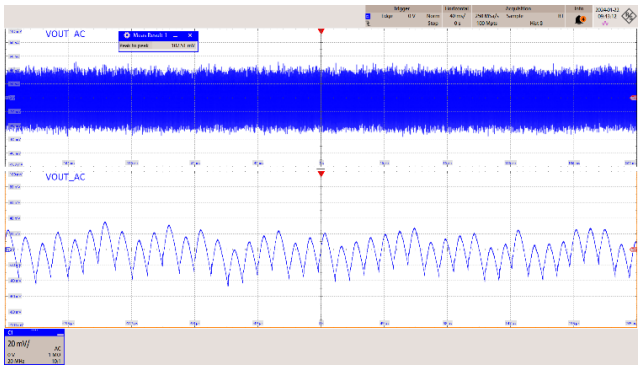


Figure 120 – Output Voltage Ripple.
265 VAC, 28 V, 5 A Load.
C1: V_{OUT}, 20 mV / div.
V_{RIPPLE}: 108 mV_{PK-PK}.
Time (Zoom): 50 µs / div.

19 Conducted EMI (QPK / AV)

19.1 Floating Output

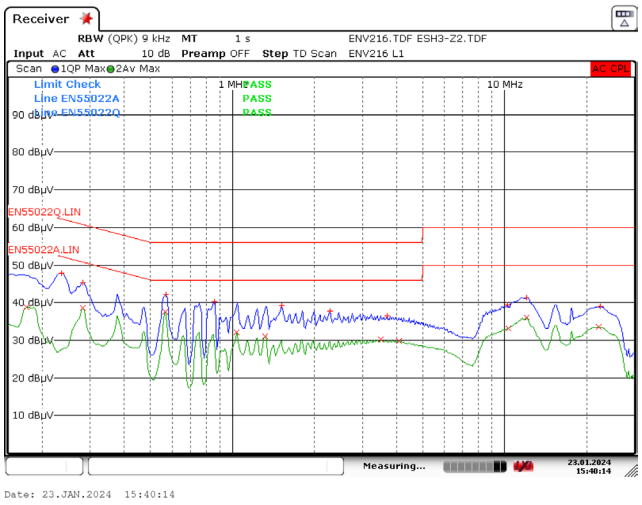


Figure 121 – Conducted EMI, Floating Output, Line. 115 VAC, 28 V, 5 A Load. Passed with 8 dB Margin.

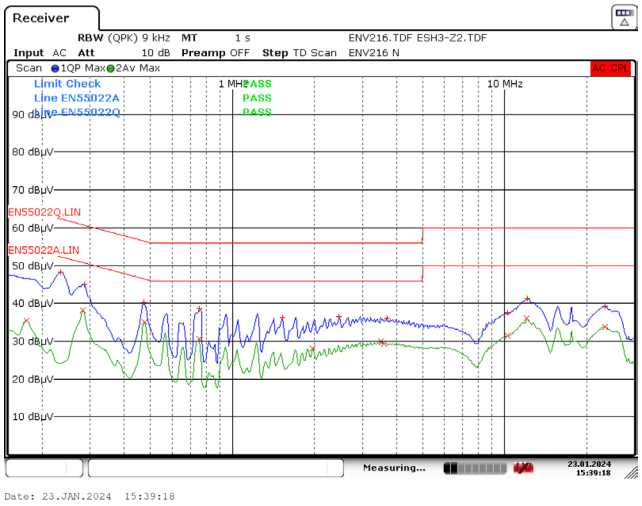


Figure 122 – Conducted EMI, Floating Output, Neutral. 115 VAC, 28 V, 5 A Load. Passed with 11 dB Margin.

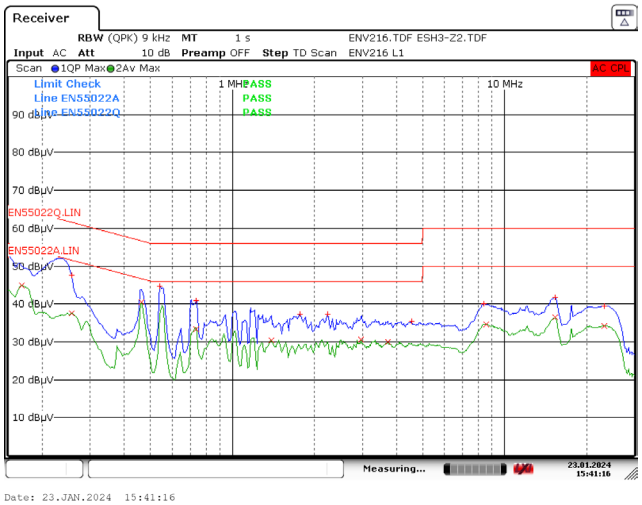


Figure 123 – Conducted EMI, Floating Output, Line. 230 VAC, 28 V, 5 A Load. Passed with 6 dB Margin.

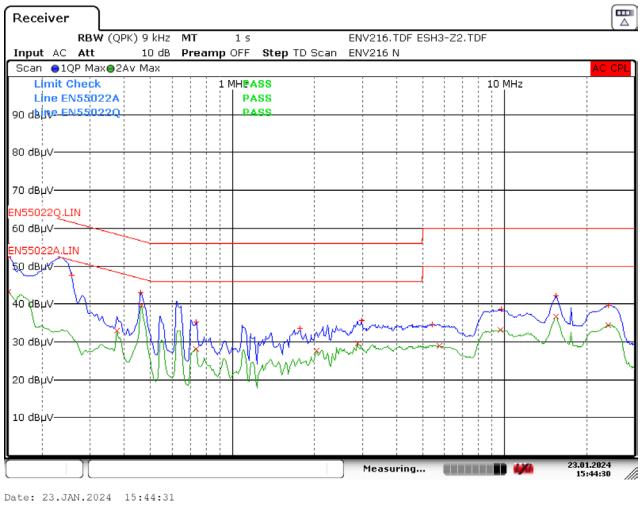


Figure 124 – Conducted EMI, Floating Output, Neutral. 230 VAC, 28 V, 5 A Load. Passed with 7 dB Margin.

19.2 Output Grounded

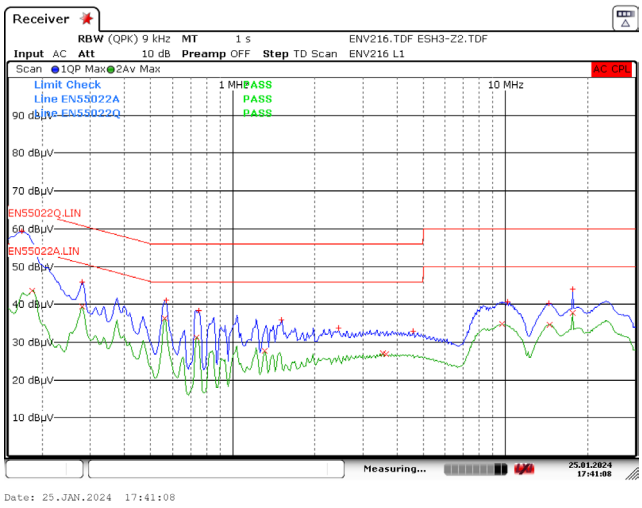


Figure 125 – Conducted EMI, Output Grounded, Line. 115 VAC, 28 V, 5 A Load. Passed with 7 dB Margin.

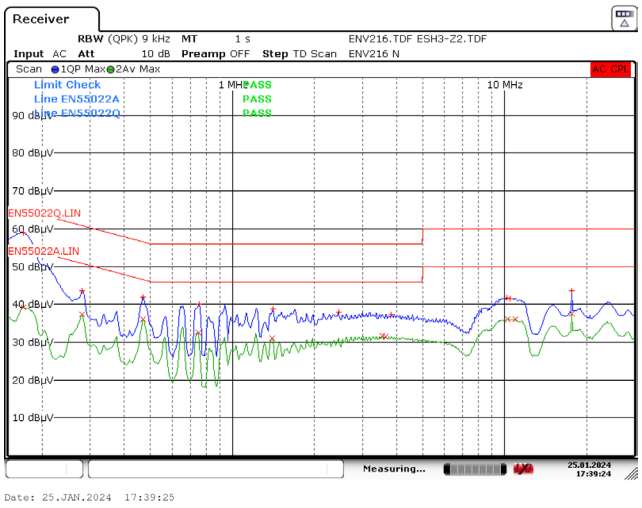


Figure 126 – Conducted EMI, Output Grounded, Neutral. 115 VAC, 28 V, 5 A Load. Passed with 6 dB Margin.

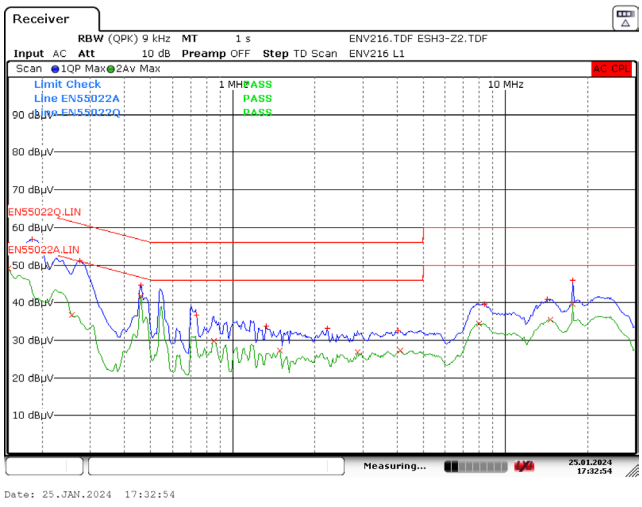


Figure 127 – Conducted EMI, Output Grounded, Line. 230 VAC, 28 V, 5 A Load. Passed with 5 dB Margin.

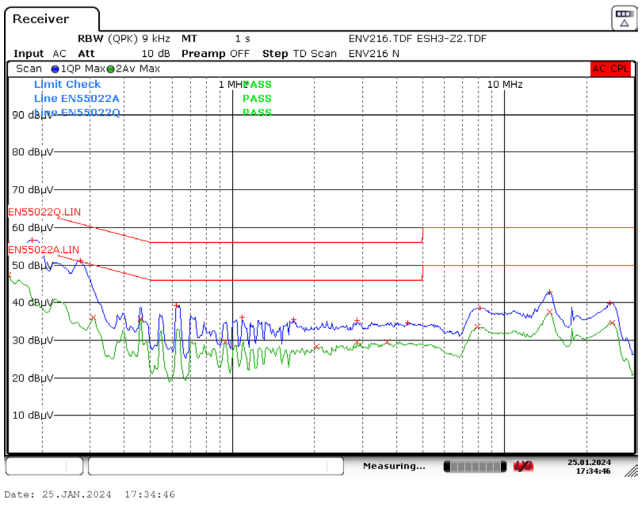


Figure 128 – Conducted EMI, Output Grounded, Neutral. 230 VAC, 28 V, 5 A Load. Passed with 7 dB Margin.

20 Surge Test

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition. A test failure was defined as a temporary loss of function which is self-recoverable.

20.1 Combination Wave Surge at 230 VAC, Differential Mode

Test Voltage (V)	Input Voltage (VAC)	Coupling	Injection Phase (°)	Remarks	Test Result 28 V / 5A (Pass/Fail)
1000	230	L to N	0	No Damage / No AR	Pass
-1000	230	L to N	0	No Damage / No AR	Pass
1000	230	L to N	90	No Damage / No AR	Pass
-1000	230	L to N	90	No Damage / No AR	Pass
1000	230	L to N	270	No Damage / No AR	Pass
-1000	230	L to N	270	No Damage / No AR	Pass

20.2 Combination Wave Surge at 230 VAC, Common Mode

Test Voltage (V)	Input Voltage (VAC)	Coupling	Injection Phase (°)	Remarks	Test Result 28 V / 5 A (Pass/Fail)
2000	230	L to PE	0	No Damage / No AR	Pass
-2000	230	L to PE	0	No Damage / No AR	Pass
2000	230	L to PE	90	No Damage / No AR	Pass
-2000	230	L to PE	90	No Damage / No AR	Pass
2000	230	L to PE	270	No Damage / No AR	Pass
-2000	230	L to PE	270	No Damage / No AR	Pass
2000	230	N to PE	0	No Damage / No AR	Pass
-2000	230	N to PE	0	No Damage / No AR	Pass
2000	230	N to PE	90	No Damage / No AR	Pass
-2000	230	N to PE	90	No Damage / No AR	Pass
2000	230	N to PE	270	No Damage / No AR	Pass
-2000	230	N to PE	270	No Damage / No AR	Pass
2000	230	L, N to PE	0	No Damage / No AR	Pass
-2000	230	L, N to PE	0	No Damage / No AR	Pass
2000	230	L, N to PE	90	No Damage / No AR	Pass
-2000	230	L, N to PE	90	No Damage / No AR	Pass
2000	230	L, N to PE	270	No Damage / No AR	Pass
-2000	230	L, N to PE	270	No Damage / No AR	Pass

20.3 Ring Wave Surge at 230 VAC, Differential Mode

Test Voltage (V)	Input Voltage (VAC)	Coupling	Injection Phase (°)	Remarks	Test Result 28 V / 5 A (Pass/Fail)
1000	230	L to N	0	No Damage / No AR	Pass
-1000	230	L to N	0	No Damage / No AR	Pass
1000	230	L to N	90	No Damage / No AR	Pass
-1000	230	L to N	90	No Damage / No AR	Pass
1000	230	L to N	270	No Damage / No AR	Pass
-1000	230	L to N	270	No Damage / No AR	Pass

20.4 Ring Wave Surge at 230 VAC, Common Mode

Test Voltage (V)	Input Voltage (VAC)	Coupling	Injection Phase (°)	Remarks	Test Result 28 V / 5 A (Pass/Fail)
2000	230	L to PE	0	No Damage / No AR	Pass
-2000	230	L to PE	0	No Damage / No AR	Pass
2000	230	L to PE	90	No Damage / No AR	Pass
-2000	230	L to PE	90	No Damage / No AR	Pass
2000	230	L to PE	270	No Damage / No AR	Pass
-2000	230	L to PE	270	No Damage / No AR	Pass
2000	230	N to PE	0	No Damage / No AR	Pass
-2000	230	N to PE	0	No Damage / No AR	Pass
2000	230	N to PE	90	No Damage / No AR	Pass
-2000	230	N to PE	90	No Damage / No AR	Pass
2000	230	N to PE	270	No Damage / No AR	Pass
-2000	230	N to PE	270	No Damage / No AR	Pass
2000	230	L, N to PE	0	No Damage / No AR	Pass
-2000	230	L, N to PE	0	No Damage / No AR	Pass
2000	230	L, N to PE	90	No Damage / No AR	Pass
-2000	230	L, N to PE	90	No Damage / No AR	Pass
2000	230	L, N to PE	270	No Damage / No AR	Pass
-2000	230	L, N to PE	270	No Damage / No AR	Pass

21 ESD Test

The unit was tested with ±8.0 kV to ±16.5 kV air discharge and ±8.0 kV to ±8.8 kV contact discharge with 10 strikes for each condition. Discharge points were added on the board to test VOUT and GND ESD performance. A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

21.1 Air Discharge

Test Voltage (kV)	No. of Strikes	Discharge Location	Remarks	Test Result 28 V / 5A (Pass/Fail)
+8	10	+ Output Terminal on Board	No Damage	Pass
	10	- Output Terminal on Board	No Damage	Pass
-8	10	+ Output Terminal on Board	No Damage	Pass
	10	- Output Terminal on Board	No Damage	Pass
+10	10	+ Output Terminal on Board	No Damage	Pass*
	10	- Output Terminal on Board	No Damage	Pass*
-10	10	+ Output Terminal on Board	No Damage	Pass
	10	- Output Terminal on Board	No Damage	Pass
+12	10	+ Output Terminal on Board	No Damage	Pass*
	10	- Output Terminal on Board	No Damage	Pass*
-12	10	+ Output Terminal on Board	No Damage	Pass
	10	- Output Terminal on Board	No Damage	Pass
+14	10	+ Output Terminal on Board	No Damage	Pass*
	10	- Output Terminal on Board	No Damage	Pass*
-14	10	+ Output Terminal on Board	No Damage	Pass
	10	- Output Terminal on Board	No Damage	Pass
+16.5	10	+ Output Terminal on Board	No Damage	Pass*
	10	- Output Terminal on Board	No Damage	Pass*
-16.5	10	+ Output Terminal on Board	No Damage	Pass
	10	- Output Terminal on Board	No Damage	Pass

21.2 Contact Discharge

Test Voltage (kV)	No. of Strikes	Discharge Location	Remarks	Test Result 28 V / 5A (Pass/Fail)
+8	10	+ Output Terminal on Board	No Damage	Pass
	10	- Output Terminal on Board	No Damage	Pass
-8	10	+ Output Terminal on Board	No Damage	Pass
	10	- Output Terminal on Board	No Damage	Pass
+8.8	10	+ Output Terminal on Board	No Damage	Pass
	10	- Output Terminal on Board	No Damage	Pass*
-8.8	10	+ Output Terminal on Board	No Damage	Pass
	10	- Output Terminal on Board	No Damage	Pass

Note: * The power supply may undergo Auto-Restart when ESD is applied.

22 Revision History

Date	Author	Revision	Description & Changes	Reviewed
14-Feb-2426-Apr-24	RN, RRI	1.0	Initial Release.	Apps & Mktg
01-Apr-24	RN, SC	1.1	Updated Schematics and Heat Sink Assembly Sections.	Apps & Mktg
26-Apr-24	RN	1.2	Updated BOM and Input and PFC Section Schematic.	Apps & Mktg

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