2SP0430V2A0C-FF1800R12IE5
SCALE™-2

power integrations™

Advanced Information

Gate Driver for 1200 V PrimePACK™ 3+ Power Modules
Supporting 2-level Applications

Product Highlights

Highly Integrated, Compact Footprint

- Ready-to-use gate driver solution for PrimePACK™ 3+ IGBT power modules with 1200 V blocking voltage
- Dual channel gate driver
- Optical I/O interface
- Secondary side power supply with reinforced insolation
- ±30 A peak output gate current
- 2 W output power per channel at maximum ambient temperature
- -40 °C to 85 °C operating ambient temperature

Protection and Safety Features

- Reinforced insulation between primary and secondary side
- Undervoltage lock-out (UVLO) protection for primary side (low voltage side) and secondary-side (high voltage side)
- Short-circuit protection
- Dynamic Advanced Active Clamping (DA^{2}C)
- Applied double sided conformal coating

Full Safety and Regulatory Compliance

- 100% production partial discharge and HIPOT test
- Clearance and creepage distances between primary and secondary sides meet requirements for reinforced isolation.

Applications

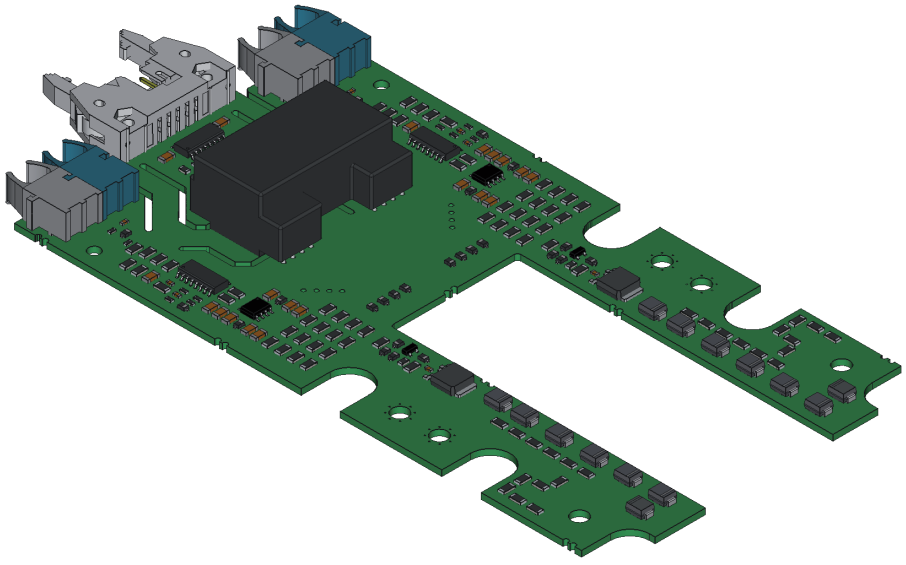
- Wind and PV power
- Traction inverter
- Industrial drives
- Other industrial applications

Applications

The plug-and-play 2SP0430V2 gate driver family is optimized for operation of 1200 V and 1700 V PrimePACK™ 3+ power modules in 2-level and 3 level applications.

The gate driver features fiber optic interface and built-in DC/DC power supply with reinforced isolation.

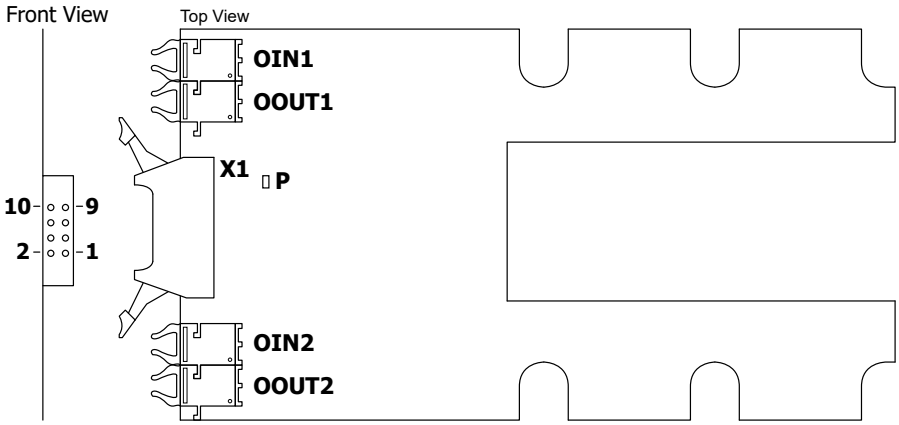
Power Integrations' Dynamic Advanced Active Clamping allows an extended DC-link voltage range in IGBT off-state for up to 60 s in PV and regenerating applications (e.g. traction).



Product Details

Part Number	Power Module	Voltage Class	Current Class	Package	Power Device Supplier
2SP0430V2A0C-FF1800R12IE5	FF1800R12IE5	1200 V	1800 A	PrimePACK™ 3+	Infineon

Interface Description



Connector X1

To external power supply (DIC-10 connector).

VDC (Pin 1, 3)

These pins are the primary-side 15 V supply voltage connection for the integrated DC/DC converter. It is mandatory to use the same supply for VDC and VCC.

VCC (Pin 7, 9)

These pins are the primary-side 15 V supply voltage connection for the primary-side electronic. It is mandatory to use the same supply for VDC and VCC.

GND (Pin 2, 4, 5, 6, 8, 10)

These pins are the connection for the primary-side ground potential. All primary-side signals refer to these pins.

Optical Interface OIN1

This is the optical receiver (Broadcom HFBR-2522ETZ) for the command input signals of channel 1.

Optical Interface OOUT1

This is the optical transmitter (Broadcom AFBR-1529Z) for the status output signals of channel 1.

Optical Interface OIN2

This is the optical receiver (Broadcom HFBR-2522ETZ) for the command input signals of channel 2.

Optical Interface OOUT2

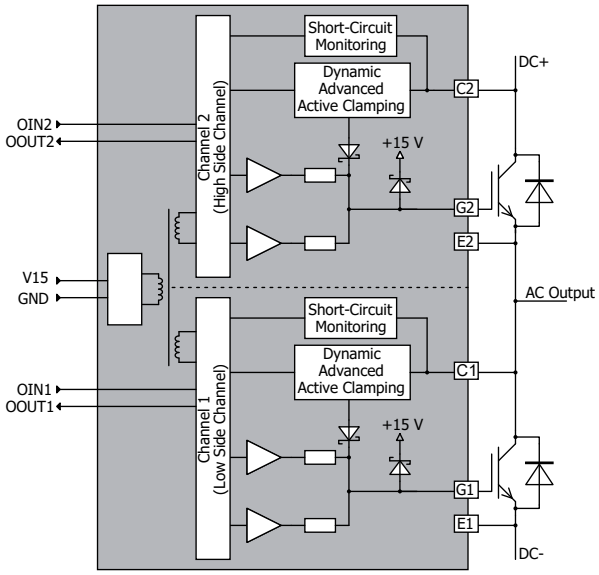
This is the optical transmitter (Broadcom AFBR-1529Z) for the status output signals of channel 2.

Optical Indicator

P

White optical indicator for monitoring the voltage V_{VCC}. During the absence of V_{VCC} the indicator is OFF.

Functional Description



The 2SP0430V2 is a dual channel plug-and-play gate driver for PrimePACK™ 3+ power modules. The gate driver is available in different variants, which all provide reinforced isolation for all primary-side signals:

- 2SP0430V2A0C for PrimePACK™ 3+ power modules features an isolation rating between primary-side and secondary-side of 5000 V_{RMS}.

As plug-and-play gate driver the 2SP0430V2 characteristics match the requirements of the individual power modules.

The operation of the channel 1 (low-side switch) and channel 2 (high-side switch) of the gate driver is independent from each other. Any dead time insertion, to avoid synchronous or overlapping switching of the driven power switches, has to be generated in the external system controller.

Note:
Synchronous or overlapping switching of top and bottom switches within a half-bridge leg may damage or destroy the driven power switche(s) and in conjunction as secondary failure the attached gate driver.

Power Supplies

The 2SP0430V2 provides two power supply inputs. For both a typical supply voltage level of 15 V is required. The first input VDC supplies the integrated DC/DC converter, which generates the isolated voltage for the secondary-side gate driver channels. The positive rail of the gate driver channels has the voltage level V_{VISOx} and the negative rail the voltage level V_{COMx}. Both are referenced to the emitter potential at terminal E1 or E2 of the driven power semiconductor.

The second input VCC supplies the primary-side electronic of the gate driver. It is mandatory to provide the supply for VDC and VCC from the same source.

Under Voltage Monitoring

The supply voltages are closely monitored. In case of an under voltage condition (UVLO) a failure signal will be provided on the status output of the gate driver. In case of an UVLO on the secondary-side, the fiber optic status signal OOUTx of the respective channel and the corresponding power semiconductor will be turned-off.

Optical Input (OIN)

This is the edge-triggered command input signal to drive attached power semiconductor. A light signal at the input OIN will turn-on the gate of the power semiconductor. Accordingly, no light signal will turn-off the gate.

Gate driver signal is transferred from OIN to the gate with a propagation delay of $t_{P(LH)}$ for the turn-on and $t_{P(HL)}$ for the turn-off commands.

Optical Output (OOUT)

During normal operation (i.e. the gate driver is supplied with power at nominal voltage, and there is no fault anywhere), the status feedback is given by a light on signal at the optical link. A failure condition is signaled by a light off signal.

Each edge of the control signal is acknowledged by the gate driver with a short pulse (the light is off for a period of tack). Because this can be observed by the external controller, this method allows simple and continuous monitoring of the driver and fiber-optic link. Figure 1 shows the control and response signals of a given driver in normal operation.

In case of a detected short-circuit of the driven power module the corresponding status feedback light SOx is set to OFF for a duration of t_{Fault} after a delay of $t_{D,Fault}$ referred to the edge of the received light signal on INx. The gate is turned off after the time $t_{P(HL),Fault}$ and blocked for t_{blk}. Figure 2 illustrates the timing of the fiber optic interface in fault (here short circuit) operating conditions.

In case of a detected under voltage lock-out condition (UVLO) on the secondary-side the corresponding status feedback light SOx is set to OFF as long as the UVLO condition is present. During fault condition no gate signal are transmitted to the respective gate driver channel.

Screw Terminals

The gate driver is mounted on top of the power module and fixed by screws. Details are given in the Section Mounting Instruction.

Gate Voltage

2SP0430V2 possesses a voltage regulator for the positive (turn-on) rail of the gate voltage. Internal current sources are regulating actively the positive gate-emitter voltage independently of actual load conditions within the maximum specified ratings. Therefore, the on-state gate-emitter voltage of the power semiconductor equals in steady state the positive supply voltage V_{VISO}.

The off-state gate-emitter voltage $V_{GE(off)}$ equals in steady state the voltage V_{COM}. This voltage is load dependent. It has its lowest value under no load conditions and is increasing slightly (i.e. getting less negative) with increasing load.

In the event of an under voltage lock-out condition the gate driver changes the control of the positive rail towards control of the negative rail V_{COM}. By this potential parasitic turn-on events of the power semiconductor are avoided.

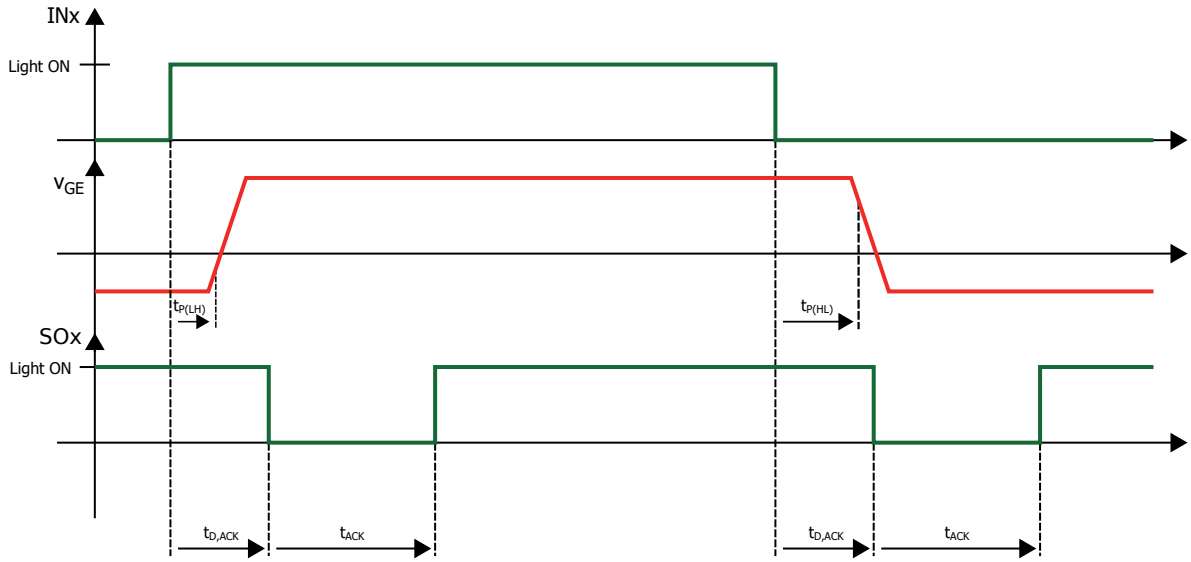


Figure 1 Driver Behavior and Status Feedback in Normal Operation

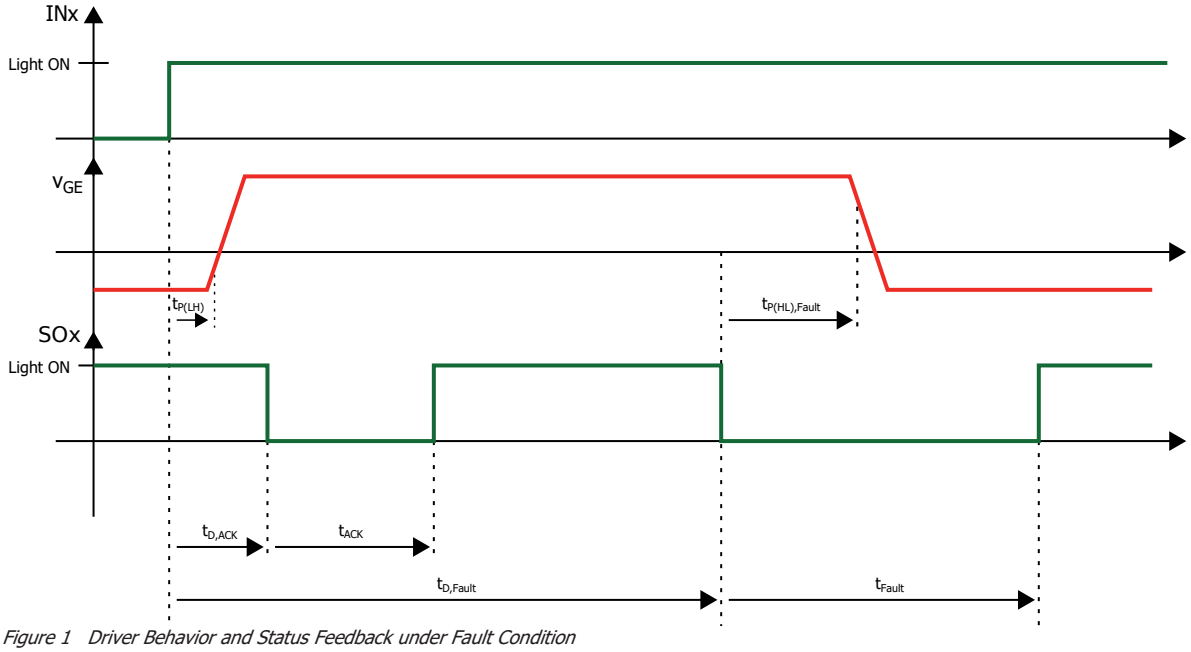


Figure 1 Driver Behavior and Status Feedback under Fault Condition

Short-Circuit Protection

The gate driver uses the semiconductor desaturation effect to detect short-circuits. The desaturation is monitored by using a resistor sensing network. The collector-emitter voltage is checked after the response time tres at turn-on to detect a short circuit. If the voltage is higher than the programmed threshold voltage $V_{CE(stat)}$, the driver detects a short-circuit condition. The monitored semiconductor is switched off immediately and a fault signal is transmitted to the status output after a delay t_{SOx}.

The fault feedback is automatically reset after the blocking time t_{blk}. The semiconductor is turned-on again as soon as the next light on signal is applied to the respective inputs after the fault status has disappeared.

It should be noted that the response time t_{res} is dependent on the DC-link voltage. It remains constant over a wide range of the higher DC-link voltage range and increases at lower DC-link voltages.

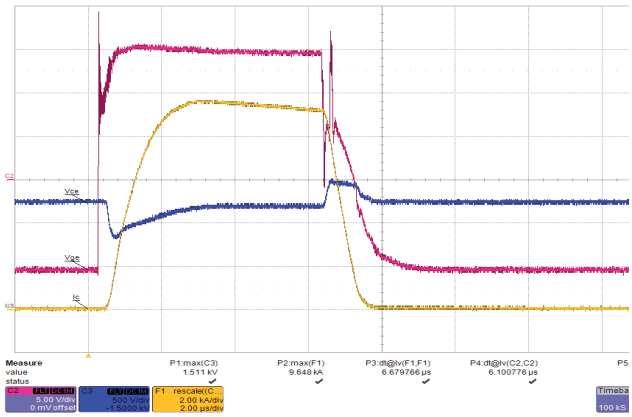


Figure 2 Short-Ciruict Turn-Off.

⚠ Note:
The desaturation function is for short-circuit detection only and cannot provide overcurrent protection. However, overcurrent detection has a lower time priority and can be easily provided by the application.

Gate Clamping

In the event of a short-circuit condition the gate voltage is increased due to the high dv_{CE}/dt between the collector and emitter terminals of the driven power semiconductor. This dv_{CE}/dt is driving a current through the Miller-capacitance (capacitance between the gate and collector) and charges the gate capacitance, which eventually leads to a gate-emitter voltage larger than the nominal gate-emitter turn-on voltage. In consequence, the short-circuit current is increased due to the transconductance of the power semiconductor.

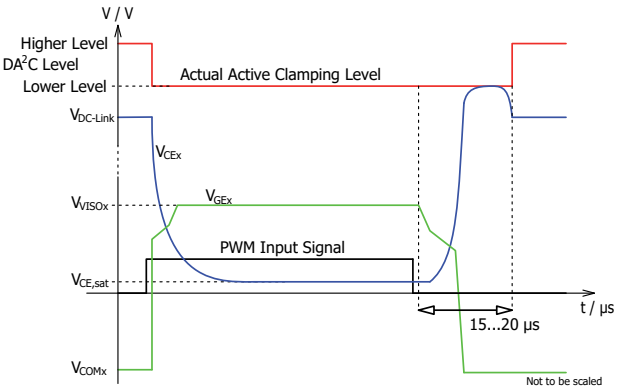
To ensure that the gate-emitter voltage stays close to the nominal turn-on voltage the gate driver features a gate-clamping circuitry. The gate clamping provides a voltage similar to V_{ISO} to the gate, i.e. 15 V. As the effective short-circuit current is a function of the gate-emitter voltage the short-circuit current is limited. This is shown in Figure 3 where the gate-emitter voltage and in consequence the short-circuit current is kept at a flat plateau. As a result the energy dissipated in the power semiconductor during the short-circuit event is reduced, leading to a junction temperature within the short-circuit safe operating area (SCSOA) limits and enables a safe turn-off of the device.

Dynamic Advanced Active Clamping (DA²C)

Active clamping is a technique designed to partially turn on the IGBT in case the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic active clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor (TVS) diodes to the IGBT gate. The 2SP0430V2 gate driver contains Power Integrations' Dynamic Advanced Active Clamping (DA²C) based on this principle:

When active clamping is activated, the turn-off MOSFET of the gate driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature – called Advanced Active Clamping – is mainly integrated in the secondary-side ASIC of the gate driver.

Additional TVS diodes have been added in series to the TVS diodes required to withstand the maximum DC-link voltage under switching operation. These TVS diodes are short-circuited during the IGBT on state as well as for about 15…20 µs after the turn-off command to guarantee efficient active clamping. After this delay, these additional TVS diodes are activated and allow the DC-link voltage to be increased to a higher value during the IGBT off-state. This feature – together with Advanced Active Clamping – is called Dynamic Advanced Active Clamping (DA²C). Note that the time during which the voltage can be applied above the value for switching operation should be limited to short periods (< 60 s).



Optical Indicator

The gate driver as one optical indicator. The white LED P monitors the voltage V_{VCC}.

Absolute Maximum Ratings

Parameters	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Max	Unit
Absolute Maximum Ratings[1]					
Primary-side supply voltage	V_{VDC}	VDC and VCC must be applied in parallel to GND	0	16	V
	V_{VCC}		0	16	
Primary-side supply current	I_{VDC}	Average supply current at full load		530	mA
Gate output power per channel	P_{Gx}			2	W
Gate output current per channel	I_G			30	A
Test voltage primary-side to secondary-side	$V_{iso,ps}$	50 Hz, 60 s		5000	V_{RMS}
Test voltage secondary-side to secondary-side	$V_{iso,ss}$	50 Hz, 60 s		4000	V_{RMS}
Operating voltage primary-side to secondary-side	V_{op}	Transient only		1700	V_{pk}
		Permanently applied		1250	V_{DC}
DC-link voltage	$V_{DC-Link}$	Switching operation		850	V_{pk}
		Off-state, limited to 60 s		1100	V_{DC}
Storage temperature[3]	T_{st}		-40	50	°C
Operating ambient temperature	T_A		-40	85	°C
Surface temperature[4]	T			125	°C
Relative humidity	H_r	No condensation		93	%
Altitude of operation[5]	A_{op}			2000	m

Recommended Operating Conditions

Parameters	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Typ	Max	Unit
Power Supply						
Primary-Side Supply Voltage	V_{VDC}	VDC to GND	14.5	15	15.5	V
	V_{VCC}	VCC to GND	14.5	15	15.5	V

Notes:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85°C.
3. The component surface temperature, which may strongly vary depending on the actual operating conditions, must be limited to the given value for coated gate driver versions to ensure long-term reliability of the coating material.
4. Operation above this level requires a voltage derating to ensure proper isolation coordination.

Characteristics - 2SP0430V2A0C-FF1800R12IE5

Parameters	Symbol	Conditions T_A = 25 °C		Min	Typ	Max	Unit
Power Supply							
Supply current	I_{VDC}	V_{VDC} = V_{VCC} = 15 V, without load			96		mA
		V_{VDC} = V_{VCC} = 15 V, f_{SW} = 10 kHz, P_{Gx} = 2W, 50 % duty cycle			420		
	I_{VCC}	V_{VDC} = V_{VCC} = 15 V, f_{SW} = 0…10 kHz			27		
Power supply monitoring threshold (secondary side)	$UVLO_{VISOx}$	Referenced to respective terminal E1 or E2	Clear fault (resume operation)	11.6	12.6	13.6	V
			Set fault (suspend operation)	11.0	12.0	13.0	
			Hysteresis	0.35			
	$UVLO_{COMx}$		Clear fault (resume operation)		-5.15		
			Set fault (suspend operation)		-4.85		
			Hysteresis		0.3		
Output voltage (secondary side)	V_{VISOx}	V_{VDC} = V_{VCC} = 15 V, Referenced to V_{COMx}, without load			25.2		V
		V_{VDC} = V_{VCC} = 15 V, Referenced to V_{COMx}, f_{SW} = 10 kHz, P_{Gx} = 2 W, 50 % duty cycle			24.7		
Coupling capacitance	C_{io}	Primary-side to secondary-side, total per channel			10		pF
Timing Characteristics							
Turn-on delay[6]	$t_{P(LH)}$	OIN to 50% of $V_{GE(on)}$, no load attached (optical cable length 1 m)			165		ns
Turn-off delay[6]	$t_{P(HL)}$	OIN to 50% of $V_{GE(off)}$, no load attached (optical cable length 1 m)			165		
Transmission delay of fault state[7]	t_{OOUT}	Optical cable length 1 m			70		
Delay to clear fault state[8]	tblk	Measured on the external controller side (optical cable length 1 m)			10		µs
Acknowledge delay time[9]	td(ack)	Optical cable length 1 m			160		ns
Acknowledge pulse width	tack	Measured on the external controller side (optical cable length 1 m)		400	600	1050	ns

Notes:

6. Measured from the transition of the turn-on or turn-off command at the optical transmitter of the external controller to the direct output of the gate drive unit (excluding the delay of the gate resitors).
7. Measured from the driver secondary-side (ASIC output) to the optical receiver on the external controller.
8. The fault status is stretched by the given value after the fault condition has been turned-off.
9. Measured from the transition of the turn-on or turn-off command at the optical transmitter of the external controller to the transition of the acknowledge signal at the optical receiver of the external controller.

Parameters	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Gate Output						
Gate turn-on voltage	$V_{GE(on)}$	V_{V15} = 15 V, without load, referenced to respective terminal Ex		15		V
		V_{V15} = 15 V, P_{Gx} = $P_{G,max}$ referenced to respective terminal Ex		15		
Gate turn-off voltage	$V_{GE(off)}$	V_{V15} = 15 V, without load, referenced to respective terminal Ex		-10.2		V
		V_{V15} = 15 V, P_{Gx} = $P_{G,max}$ referenced to respective terminal Ex		-9.7		
Short-Circuit Protection						
Static V_{CE}-monitoring threshold	$V_{CE(stat)}$			tbd		V
Response time	t_{res}	DC-link voltage = 850 V		tbd		µs
		DC-link voltage = 600 V		tbd		
		DC-link voltage = 500 V		tbd		
Delay to power semiconductor turn-off after short-circuit detection	$t_{pd,SC}$			0.2		µs
Electrical Isolation						
Test voltage[10]	$V_{iso,ps}$	Primary side to secondary side	5			kV_{RMS}
	$V_{iso,ss}$	Secondary side to secondary side	4			
Partial discharge extinction voltage[11]	$P_{D,ps}$	Primary side to secondary side	1.77			kV_{pk}
	$P_{D,ss}$	Secondary side to secondary side	1.7			
Creepage distance	CPG_{P-S}	Primary side to secondary side	30			mm
	CPG_{S-S}	Secondary side to secondary side	7			
Clearance distance	CLR_{P-S}	Primary side to secondary side	12.6			mm
	CLR_{S-S}	Secondary side to secondary side	7			
Mounting						
Terminal connection torque		Screw M4	1.8		2.1	Nm
Terminal diameter[12]	d_{M3}	Screw holes S1 and S2			8.8	mm
	d_{M4}	Module Terminals Gx, Ex and Cx			9.8	
Bending[13]	l_{bend}	According to IPC			0.75	%
Gate Output - 2SP0430V2A0C-FF1800R12IE5						
Turn-on gate resistor	$R_{G(on)}$			0.85		Ω
Turn-off gate resistor	$R_{G(off)}$			3.375		Ω
Auxiliary gate capacitor	C_{GE}			N.A.		nF

Notes:

10. The transformer of every production sample has undergone 100% testing at the given value for 1s.
11. Partial discharge measurement is performed on each transformer. The measurements are performed in accordance with IEC 60270 and IEC 60664-1 for basic insulation requirements.
12. This refers to the double value of the maximum radius from hole center to the next metallic part (d_{M3}) resp. to the end of the metallic pad (d_{M4}).
13. Refer to section *Mounting Instruction* for absolute values of allowed bending distances.

Mounting Instructions

The gate driver is mounted on top of the target power module with six screws to the gate, emitter, and collector terminals (Figure 3). The mounting force is given with M_{M4}. The given value refers to the mechanical property of the gate driver only. M_{M4} must not exceed the values given in the respective datasheet of the target power module. Hence, actual mounting torque may be smaller than M_{M4}.

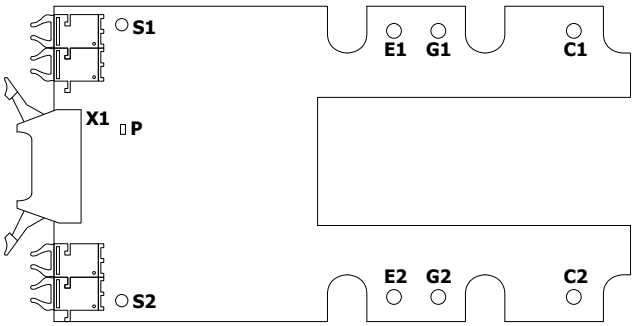


Figure 3 Screw Terminals.

To maintain the electrical isolation distances, the screw header including any washer must not exceed the available metallic terminal pad of the gate driver. For the terminals G1, E1, C1, G2, E2, and C2 the corresponding distances are given with d_{M4}.

To avoid mechanical stress of the gate driver during and after the mounting process any bending or warping force imposed to the gate driver must not lead to a vaulting or twisting of the housing of more than l_{bend} per axis according to Figure 4:

- Axis 1 and 2: max. 0.9 mm bending
- Axis 3: max. 0.7 mm bending
- Axis 4 and 5: max. 1.2 mm bending

The 2SP0430V2 possesses two fixation points S1 and S2 (Figure 3) for stand-offs to mitigate any bending force during assembly and operation. The stand-off could be mounted on the heatsink or the frame of the inverter system. The maximum diameter of the screw header and washer for the stand-offs are limited by d_{M3}.

Note:

The stand-offs have to be made of insulating material to avoid any conducting path from the gate driver to the heatsink or inverter frame.

In Figure 5 the minimum required space in front of the power module for mounting the 2SP0430V is given with A = 88.8 mm. This distance includes also the space for connector X1 with mounted cable. Further dimensions are given in section Product Dimensions.

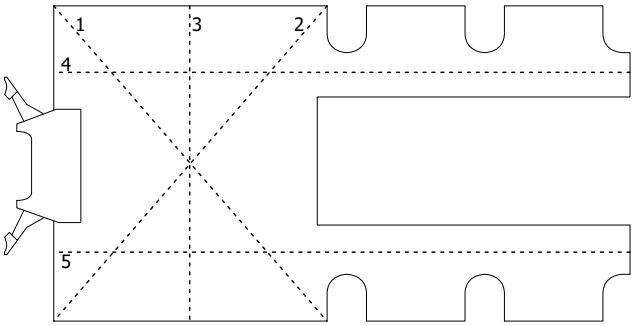


Figure 4 Screw Terminals.

To ensure proper cooling by natural or forced convection minimum clearance of 50 mm of the gate driver top side is required as shown in Figure 5. This includes also that the AC and/or DC bus bars are not covering parts or the entire gate driver top side (red circled area in Figure 5).

Cables

The cable from gate driver connector X1 to the system level controller is not part of the 2SP0430V gate driver and has to be provided by the designer of the system. It is recommended to route the cable with minimum parasitic coupling from the controller to the gate driver. Parasitic coupling in particular to any potential of the secondary-side of the gate driver (i.e. high voltage side) and the AC and/or DC bus bar has to be avoided. Otherwise, increased common-mode currents may circulate, which may cause interferences with command, measurement and/or status feedback signals. Furthermore, usage of pair-wise twisted cables is recommended.

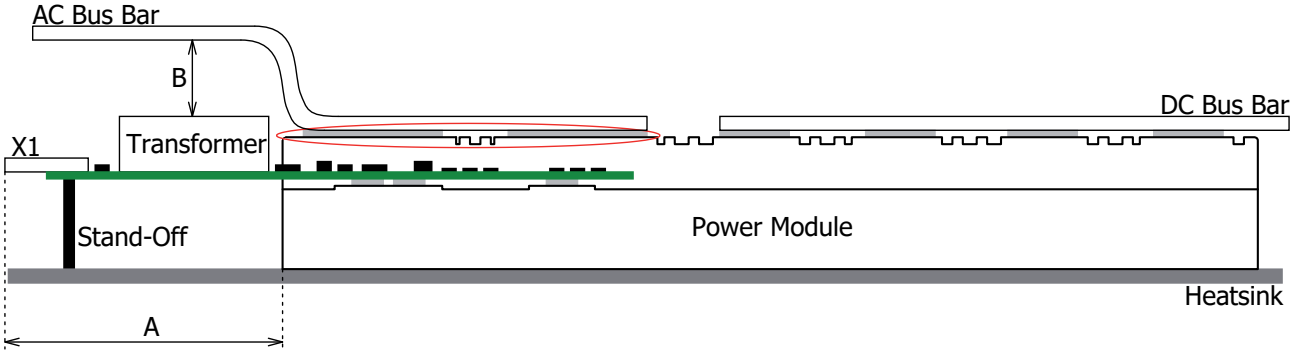


Figure 5 2SP0430V Mounted on PrimePACK™3+ Power Module showing Relevant Distances to the Surrounding..

Application Guidelines

The following guidelines are meant to optimize the overall system performance when using 2SP0430V gate drivers in various applications.

Power Supply

The gate driver has to be supplied by a fixed voltage of typically 15V at VDC and VCC. It is mandatory that one supply is used for both terminals.

DC-Link Design

The mechanical and electrical design of the DC-link of the target application determines during turn-off events of the driven power semiconductor the over voltages ΔV_{CE} according to equation (1). Here, L_σ describes the overall DC-link stray inductance (i.e. sum stray inductance of DC-capacitors, DC-link bus bar and power module) and di_C/dt the collector current change.

$$\Delta V = L_\sigma \cdot \frac{di_C}{dt} \qquad (1)$$

If the over voltage ΔV_{CE} plus the applied DC-link voltage V_{DC} exceed the breakdown voltage of the driven power module (refer to the reverse bias safe operating area RBSOA), the power module may be damaged. In case of excessive turn-off over voltages, one or more of the following application parameters have to be decreased:

- DC-link voltage V_{DC}
- Stray inductance L_σ
- Collector current i_C

Therefore, during the installation and testing of the target application the actual over voltages ΔV_{CE} at different conditions have to be measured.

Note: 2SP0430V gate driver will actively limit any over voltage during turn-off events under normal and over current conditions to safe levels using the implemented Dynamic Advanced Active Clamping scheme. However, it is not recommened that the clamping feature is active during normal switching conditions. It may lead to an over load of the implemented clamping devices. Furthermore, it might lead to an under voltage lock-out (UVLO) condition on the secondary-side power supply of the gate driver.

Paralleling of Power Modules

Paralleling of PrimePACK™ 3+ power modules with 2SP0430V gate driver is in principle possible if the following basic rules are obeyed to ensure minimum load current imbalances and general proper system operation.

The load current sharing between paralleled power modules depends on several factors:

- Deviation of the power modules parameters like IGBT saturation voltage V_{CEsat}, diode forward voltage V_F, rise and fall times t_r and t_f, turn-on and turn-off delay times $t_{d(on)}$ and $t_{d(off)}$. They are influencing the current sharing in the conducting (static) and switching (dynamic) phase.
- Deviation in the cooling of the power modules. The before mentioned parameters are mostly temperature dependent. Inhomogeneous cooling of paralleled power modules influences therefore the static and dynamic current sharing.
- Deviation of the gate loop impedance. It leads to static and dynamic current imbalances.
- Deviation of the apparent DC-link stray inductance and resistance per paralleled power module. It leads to static and dynamic current imbalances.

Power module parameter deviations can be addressed by screening of power modules as offered by some manufacturers. The deviation in cooling can be compensated to a fair degree by the inherent positive temperature coefficient of the power modules. In case one power module takes over more current than the other power modules, it will heat-up more than the others. As a result the saturation voltage is increased, which leads to a reduction of the current in the power module. The system is self-regulated to a certain extent.

Deviations of the gate loop impedances are minimized by design, process and assembly control of 2SP0430V. Part of the gate loop impedance is also the terminal screw connection of the gate driver towards the power module. Here the recommended (i.e. maximum) mounting torque must be obeyed to minimize its influence.

Deviation of the apparent DC-link stray inductance and resistance between paralleled power modules refers to the mechanical arrangement of the power modules and DC-link.

Depending on the actual application conditions is might be required to add inductors in the AC output phases of each paralleled power module to symmetrize load current imbalance.

Note: Do not operate paralleled power modules without connected gate driver. This may lead to half-bridge short-circuits within the power modules and will eventually destroy them.

Multilevel Topologies

2SP0430V gate driver are designed for 2-level and 3-level topologies. For 3-level topologies:

- Cascaded multilevel topologies on system level like for instance Modular Multilevel Converter (MMC) operating with 2-level topologies within one cell are supported without any restriction (implying that required isolation requirements are fulfilled).
- For 3-level systems the turn-off sequence has to be obeyed by the system controller to avoid overvoltage events, which might lead to an RBSOA (reverse biased safe operating area) violation of the power module. However, 2SP0430V2 gate driver have Power Integrations' Dynamic Advanced Active Clamping (DA^2C) implemented, which enables the gate driver to protect the power modules against over voltage conditions arising by wrong turn-off sequences. The suitability of DA^2C has to be checked within the target application.

Note: During short-circuit and/or under voltage events, the gate driver will immediately switch-off the respective power module. No control on the turn-off sequence is given. Therefore, the suitability of 2SP0430V has to be checked on application level for this kind of topology.

Conformal Coating

The electronic components of the gate driver are protected by a layer of acrylic conformal coating with a typical thickness of 50 µm using ELPEGUARD SL 1307 FLZ/2 from Lackwerke Peters on both sides of the PCB. This coating layer increases the product reliability when exposed to contaminated environments.

Note: Standing water (e.g. condensate water) on top of the coating layer is not allowed as this water will diffuse over time through the layer. Eventually it will form a thin film of conducting nature between PCB surface and coating layer, which will cause leakage currents. Such currents may lead to a disturbance of the performance of the gate driver.

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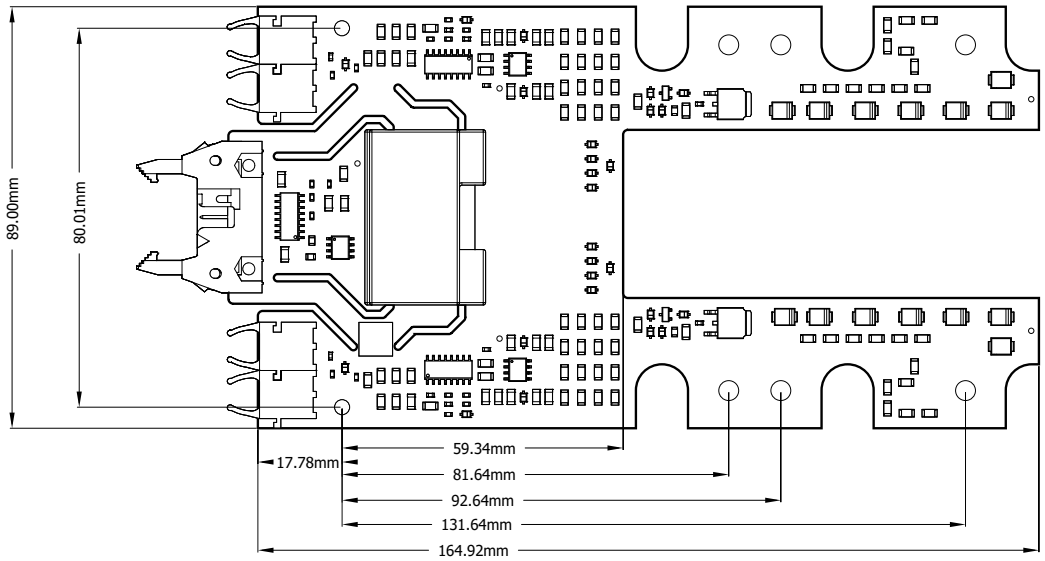
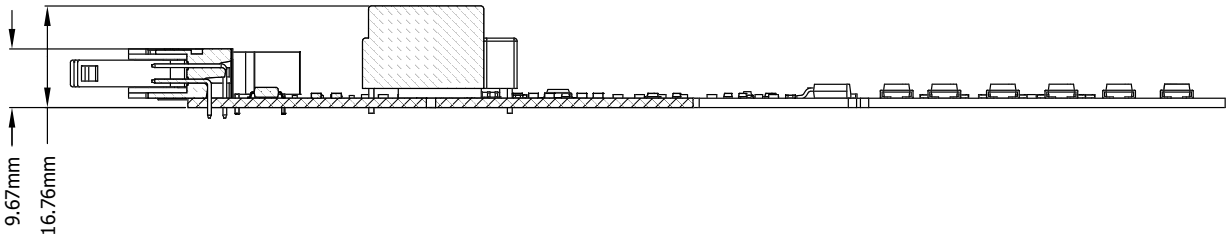
Product Dimensions

Top View



Side View



Transportation and Storage Conditions

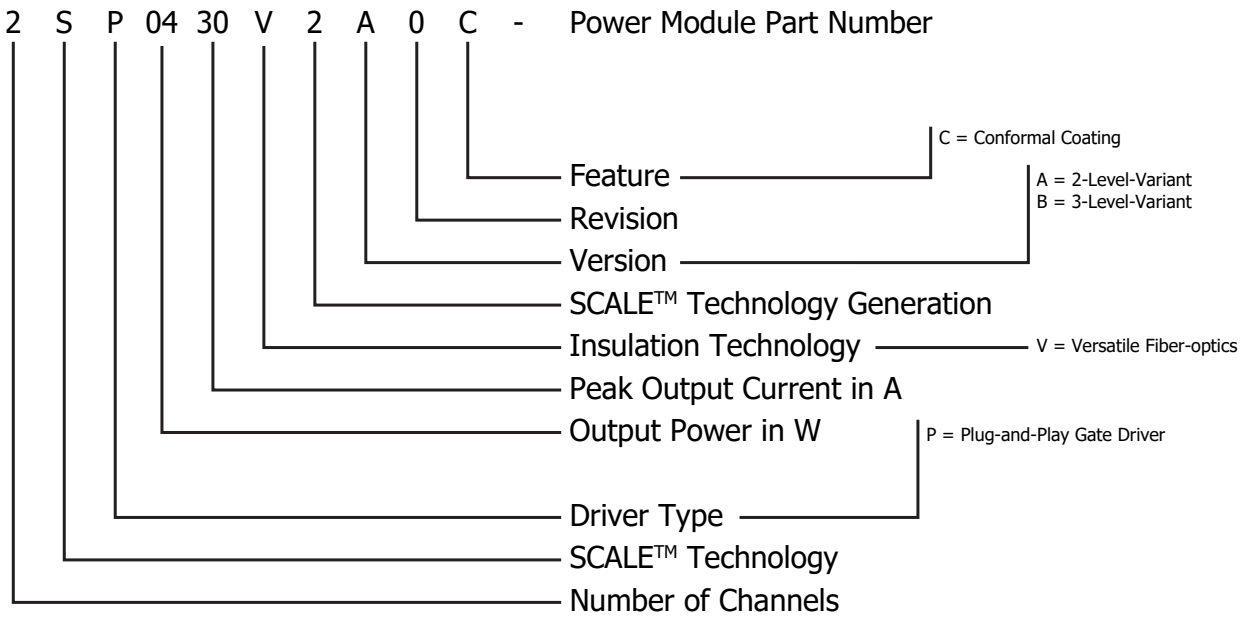
For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

We hereby confirm that the product supplied does not contain any of the restricted substances according Article 4 of the RoHS Directive 2011/65/EU in excess of the maximum concentration values tolerated by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.

Part Ordering Information



Revision	Notes	Date
A	Target Datasheet	09/20

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Safety Notice

The data contained in this datasheet is intended exclusively for technically trained staff. Handling all high-voltage equipment involves risk to life. Strict compliance with the respective safety regulations is mandatory.

Any handling of electronic devices is subject to general specifications for protecting electrostatic-sensitive devices according to international standard IEC 60747-1, Chapter IX or European standard EN 100015 (i.e. the workplace, tools, etc. must comply with these standards). Otherwise, this product may be damaged.

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