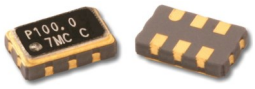
PLETRONICS HC5544DEV-100.0M
HCSL Clock Oscillator



HC55DV
3.2 x 5.0 x 1.35 mm
LCC Ceramic Package

Features

- Pletronics' HC55D Series is a Quartz crystal controlled Precision Square Wave Oscillator
- HCSL Output
- Enable/Disable Function on pad 1
- Fast Rise & Fall Time / Low Jitter
- 3.3V nominal Supply Voltage
- 100 MHz Frequency

Applications

Driving A/Ds, D/As, FPGAs
Fibre Channel
Ethernet, GbE, SynchE
Medical
Storage Area Networking
COTS
Telecom
PON

COMPLIANT FOR PCIe GENERATIONS 1,2,3, AND 4

Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Frequency	-	100	-	MHz	
Frequency Stability vs. Temperature	-25	-	+25	ppm	For all supply voltages, load changes, aging for 1 year at 25°C ± 2°C, shock, vibration and temperatures
Operating Temperature Range	-40	-	+85	°C	Extended Range
Supply Voltage [1] V_{CC}	2.97	3.30	3.63	V	
Supply Current I_{CC}	-	22	33	mA	
Output Waveform		HCSL			
Output High Level V_{OH}	550	-	850	mV	See load circuit
Output Low Level V_{OL}	-150	-	150	mV	See load circuit
Output T_{RISE} and T_{FALL}	-	0.3	0.5	ns	Vth is 20% and 80% of waveform
Startup Time	-	-	2	ms	Time for output to reach specified frequency
Duty Cycle	45	-	55	%	50% of V_{CC} (See Load Circuit)
$V_{DISABLE}$	-	-	30	%Vcc	Referenced to ground
V_{ENABLE}	70	-			
Enable Time	-	-	2	ms	Time for output to reach a logic high state
Disable Time	-	-	200	ns	Time for output to reach a high Z state
Output Leakage $V_{OUT} = V_{CC}$ $V_{OUT} = 0V$	-10 -10	-	+10 +10	µA	Pad 1 low, device disabled
Standby Current	-	-	10	µA	
Jitter	-	0.2	-	ps	12 kHz to 20 MHz from the output frequency at 100 MHz
Phase Noise 10 Hz 100 Hz 1 kHz 10 kHz 100 kHz	-	-67 -101 -128 -142 -145	-	dBc/Hz	25°C ± 2°C at 100 MHz
Storage Temperature Range	-55	-	+125	°C	

Notes: Specifications with Pad 1 E/D open circuit
[1] Place an appropriate power supply bypass capacitor next to device for correct operation

COMPLIANCE STATEMENT

SUMMARY OF RESULTS FROM INDEPENDENT TEST LAB

Specification	
Specification name:	PCIE-BASE-REV4.0-CC-REFCLK
Specification title:	Common-clock Refclk Evaluation for PCIe® v4.0 BASE (v1.0)
Specification owner:	JitterLabs
Device Under Test	
Sample product number:	HC5544DEV-100.0M
Sample description:	HCSL Crystal Oscillator
Sample manufacturer:	Pletronics
Sample submitted by:	Pletronics
Test Report	
Test Report number:	JL18011700
Test date:	Jan 17, 2018
Test frequency:	100 000 000 Hz
Test supply voltage:	3.300 V
Test temperature:	25 °C

PCIE-BASE-REV4.0-CC-REFCLK, v1

Specification title:	Common-clock Refclk Evaluation for PCIe® v4.0 BASE (v1.0)
Standard body:	PCI-SIG® association
Standard name:	PCIe® v4.0 GEN 1/2/3/4 [1]
Specification owner:	JitterLabs
Warning margin:	5% for all tests, except Tssc_freq_dev (0.5%).

GEN-1:	100% passing
GEN-2:	100% passing
GEN-3:	100% passing
GEN-4:	100% passing

Overall result

Gary Giust, PhD
CEO, JitterLabs

Approved by

JitterLabs
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1 (408) 627-6454

Contact

PLEASE CONTACT PLETRONICS FOR FULL REPORT

Part Number

Series Model	Frequency Stability		Operating Temperature Range	Supply Voltage V_{CC}	Frequency in MHz	Optional T&R Packaging code
HC55	**44**	**D**	**E**	**V**	**- 100.0M**	**-XX**
	45 = ± 50 ppm (STD) **44** = ± 25 ppm **20** = ± 20 ppm		**Blank** = -10 to +70°C (STD) **C** = -20 to +70°C **E** = -40 to +85°C	**V** = 3.3V±10%	13 - 220 MHz	**T250** = 250 per Reel **T500** = 500 per Reel **T1K** = 1000 per Reel (Std for 1K pcs)

Device Marking

P*FFF.F*H
- ***YMDx***

P = Pletronics
FFF.F = Frequency in MHz
H =HCSL Output
YMD = Date Code, All other marking is internal codes

Note: Specifications such as frequency stability, supply voltage and operating temperature range, etc. are not identified from marking. External packaging labels and packing list will correctly identify the ordered Pletronics part number.

Codes for Date Code YMD (Year Month Day)

Code	5	6	7	8	9	Code	A	B	C	D	E	F	G	H	J	K	L	M
Year	2015	2016	2017	2018	2019	Month	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC

Code	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	G
Day	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Code	H	J	K	L	M	N	P	R	T	U	V	W	X	Y	Z	
Day	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Package Labeling

Tape and Reel available for quantities of 250 to 1000 per reel, cut tape for < 250. 16mm tape, 8mm pitch.

P/N Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Courier New
Bar code is 39-Full ASCII

RoHs Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Arial

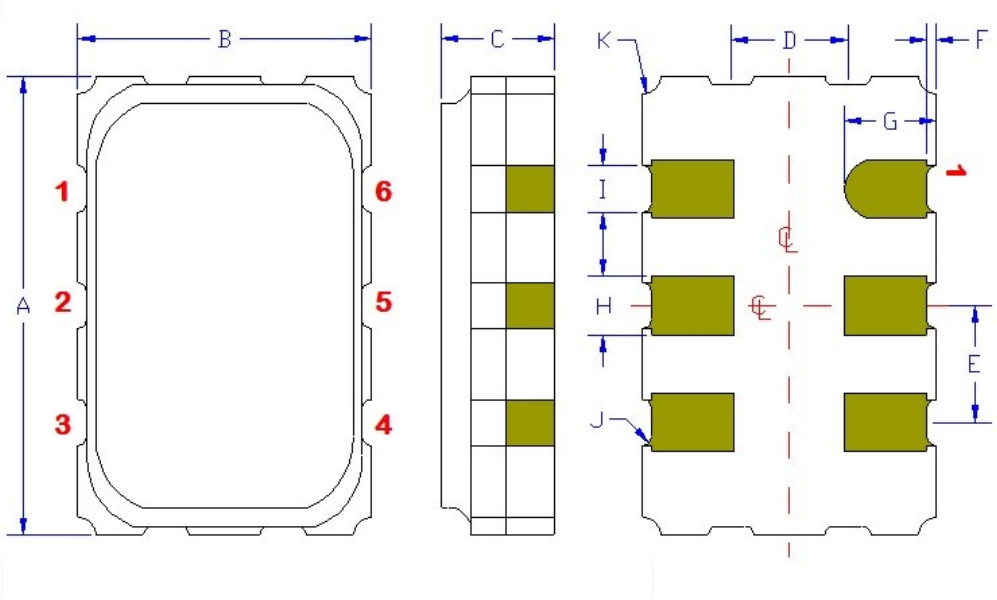
RoHS Compliant
2nd LvL Interconnect
Category=e4
Max Safe Temp=260C for 10s 2X Max

Pletronics Inc. certifies this device is in accordance with the RoHS 2 (2011/65/EU) and WEEE (2002/96/EC) directives.

Pletronics Inc. guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
Weight of the Device: 0.17 grams
Moisture Sensitivity Level: 1 As defined in J-STD-020D
Second Level Interconnect code: e4

Mechanical Dimensions

	Inches	mm
A	0.197 ± 0.006	5.00 ± 0.15
B	0.125 ± 0.006	3.20 ± 0.15
C	0.063 max	1.35 max
D[1]	0.050	1.27
E[1]	0.050	1.27
F[1]	0.004	0.10
G[1]	0.039	1.00
H[1]	0.025	0.63
I[1]	0.020	0.50
J[1]	0.004R	0.10R
K[1]	0.008R	0.20R



[1] Typical dimensions

(Not to Scale)

Contacts (pads): Gold 11.8 to 39.4 µinches (0.3 to 1.0 µm) over Nickel 50 to 350 µinches (1.27 to 8.89 µm)

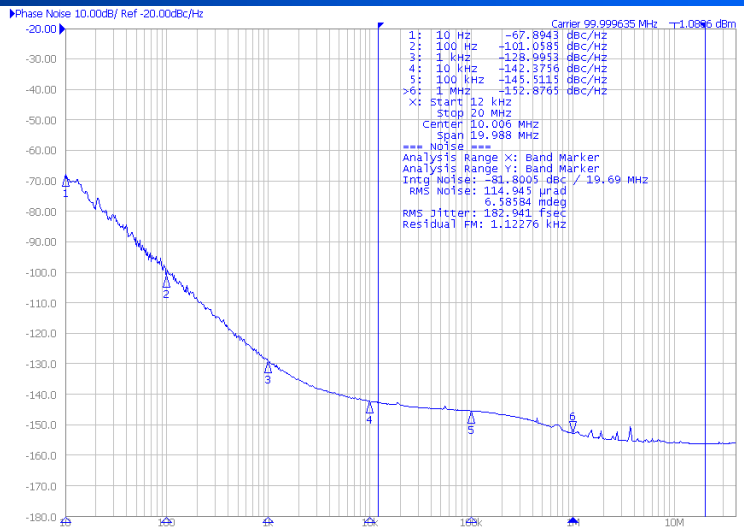
Layout

Pad	Function	Note
1	Output Enable/Disable	The oscillator shall operate when this pad is not connected. The output will be inhibited (high impedance state) when this pad is logic low. Recommend connecting this pad to V_{CC} if the oscillator is to be always on.
2	No connect	There is no internal connection to this pad. Recommend connecting to pad 1 to permit E/D input on either pad for layout.
3	Ground (GND)	
4	Output	Both outputs must be terminated and biased for proper operation. The ideal termination is 100 ohms between the outputs
5	Output*	
6	V_{CC} Supply Voltage	Connect an appropriate power supply bypass capacitor as close as possible to pad 4

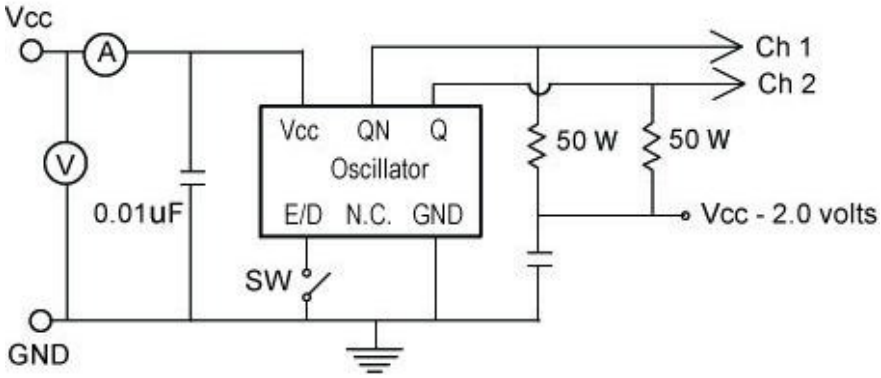
For Optimum Jitter Performance, Pletronics recommends:

- A ground plane under the device
- Do not route large transient signals (both current and voltage) under the device
- Do not place near a large magnetic field such as a high frequency switching power supply
- Do not place near piezoelectric buzzers or mechanical fans

Typical Phase Noise



Electrical Test /Load Circuit



Environmental / ESD Ratings

Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	JESD22-B104
Vibration	JESD22-B103
Solderability	IPC J-STD-002
Thermal Shock	MIL-STD-883 Method 1011, Condition A

ESD Rating

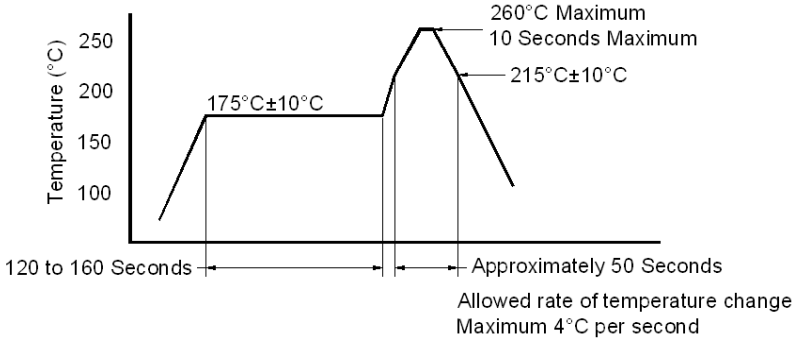
Model	Min. Voltage	Condition
Human Body Model	2000V	JESD22-A114
Charged Device Model	500V	JESD 22-C101
Machine Model	200V	JESD22-A115

Thermal Characteristics:
The maximum die or junction temperature is 155°C
The thermal resistance junction to board is 30 to 50°C/Watt depending on the solder pads, ground plane and construction of the PCB.

Absolute Maximum Ratings

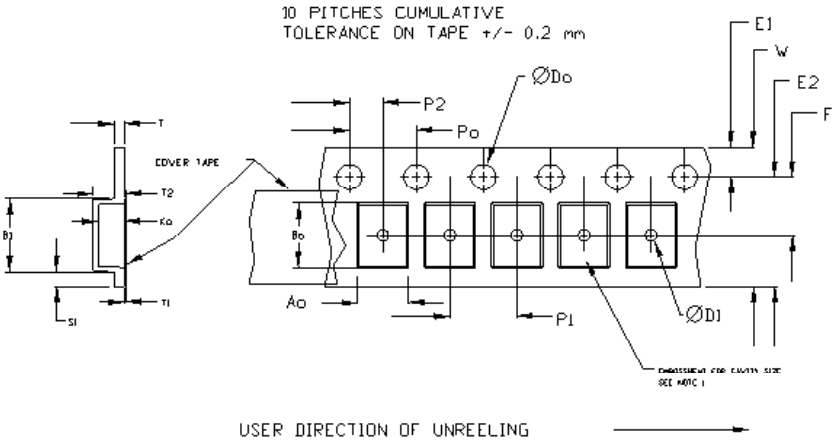
Parameter	Unit
V_{CC} Supply Voltage	-0.5V to +5.0V
Vi Input Voltage	-0.5V to V_{CC} + 0.5V
Vo Output Voltage	-0.5V to V_{CC} + 0.5V

Reflow Cycle



The part may be reflowed 2 times without degradation (typical for lead free processing).

Tape and Reel

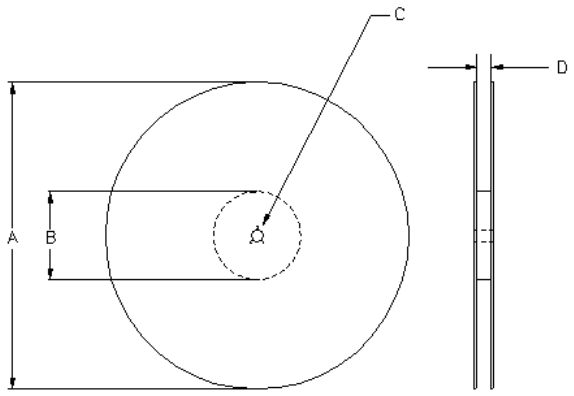


Tape Constant Dimensions Table 1								
Tape Size	Do	D1 min	E1	Po	P2	S1 min	T max	T1 max
8mm	1.5 +0.1 -0.0	1.0	1.75 ±0.1	4.0 ±0.1	2.0 ±0.05	0.6	0.6	0.1
12mm		1.5						
16mm		1.5			2.0 ±0.1			
24mm		1.5						

Tape Variable Dimensions Table 2							
Tape Size	B1 max	E2 min	F	P1	T2 max	W max	Ao, Bo & Ko
16mm	12.1	14.25	7.5 ±0.1	8.0 ±0.1	8.0	16.3	Note 1

Dimensions in mm Drawing Not to scale

Note 1: Embossed cavity to conform to EIA– 481-B



Reel Dimensions (may vary) Table 3						
	A		B		C	D
Reel Size	Inches	mm	Inches	mm	mm	mm
7	7.0	177.8	2.50	63.5	13.0 +0.5 -0.2	Tape size +0.4 +2.0 -0.0
10	10.0	254.0	4.00	101.6		
13	13.0	330.2	3.75	95.3		

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