

User's Guide For Evaluation Board NN31002A-EVB

Power Supply in Package (PSiP)

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1 Introduction

This user's guide contains background information for the

NN31002A : 4A Synchronous DC-DC Step Down Regulator(1ch),Power Supply in Package (PSiP) which integrates a Controller IC that employs a hysteretic control system, two Power MOSFETs, an Inductor and Capacitors into a single QFN package.

as well as support documentation for the NN31002A Evaluation Board (NN31002A-EVB). Also included are the appearance , the pin function , the test set-up , the schematic , the bill of materials and the board layout for the Evaluation Board.

1.1 Overview

NN31002A is a synchronous DC-DC Step Down Regulator (1-ch) Power Supply in Package (PSiP), which integrates a Controller IC that employs a hysteretic control system, two Power MOSFETs, an Inductor and Capacitors into a single 8.5 x 7.5 x 4.7 mm QFN package. The easiness of mounting PSiP onto Printed Circuit Board (PCB), a very small footprint and a highly reduced number of external components, offers very compact and simplified solutions for applications requiring point-of-load design. The number of external components have been reduced to only input / output capacitor, slow start capacitor and feedback resistors. Furthermore, for applications requiring an output voltage of 1.0V / 3.3V, the external feedback resistors can be eliminated, resulting into even a smaller footprint.

The PSiP achieves efficiencies of greater than 94% with very good power dissipation capabilities.

Table 1. NN31002A-EVB Input Voltage / Output Current

| EVB | INPUT VOLTAGE RANGE | OUTPUT CURRENT RANGE |
|--------------|----------------------------------|----------------------|
| NN31002A-EVB | VIN = 4.5 V to 28 V VEN = 5 V | 0 A to 4 A |

1.2 Recommended Operating Conditions

Table 2. NN31002A-EVB Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|----------------------|---------------------|-------|-----|------------------------|------|-------|
| Supply Voltage range | AV _{IN} | 4.5 | 12 | 28 | V | — |
| | PV _{IN} | 4.5 | 12 | 28 | V | — |
| Input Voltage Range | V _{MODE} | − 0.3 | — | V _{REG} + 0.3 | V | *1 |
| | V _{FSEL} | − 0.3 | — | V _{REG} + 0.3 | V | *1 |
| | V _{PRTCNT} | − 0.3 | — | V _{REG} + 0.3 | V | *1 |
| | V _{EN} | − 0.3 | — | 5.0 | V | — |
| Output Voltage Range | V _{PGOOD} | − 0.3 | — | V _{REG} + 0.3 | V | *1 |
| | V _{LX} | − 0.3 | — | V _{IN} + 0.3 | V | *2 |

Notes : Voltage values, unless otherwise specified, are with respect to GND.

GND is voltage for AGND, PGND. AGND = PGND

V_{IN} is voltage for AVIN, PVIN. V_{IN} = AV_{IN} = PV_{IN}.

Do not apply external currents or voltages to any pin not specifically mentioned.

*1 : (V_{REG} + 0.3) V must not exceed 6 V.

*2 : (V_{IN} + 0.3) V must not exceed 30 V.

1.3 Block Diagram

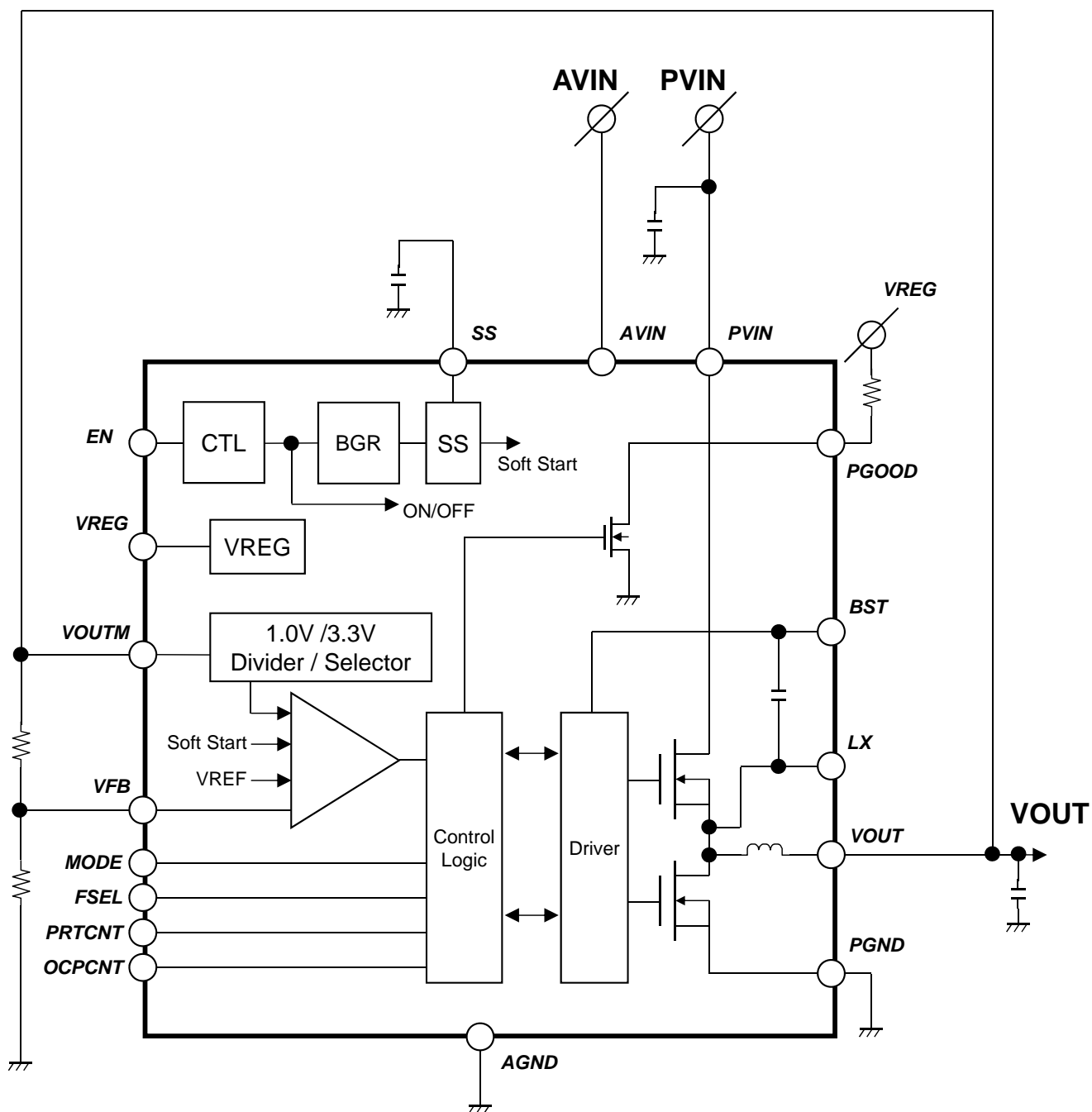


Figure 1. Block Diagram

1.4 Schematic of Evaluation Board

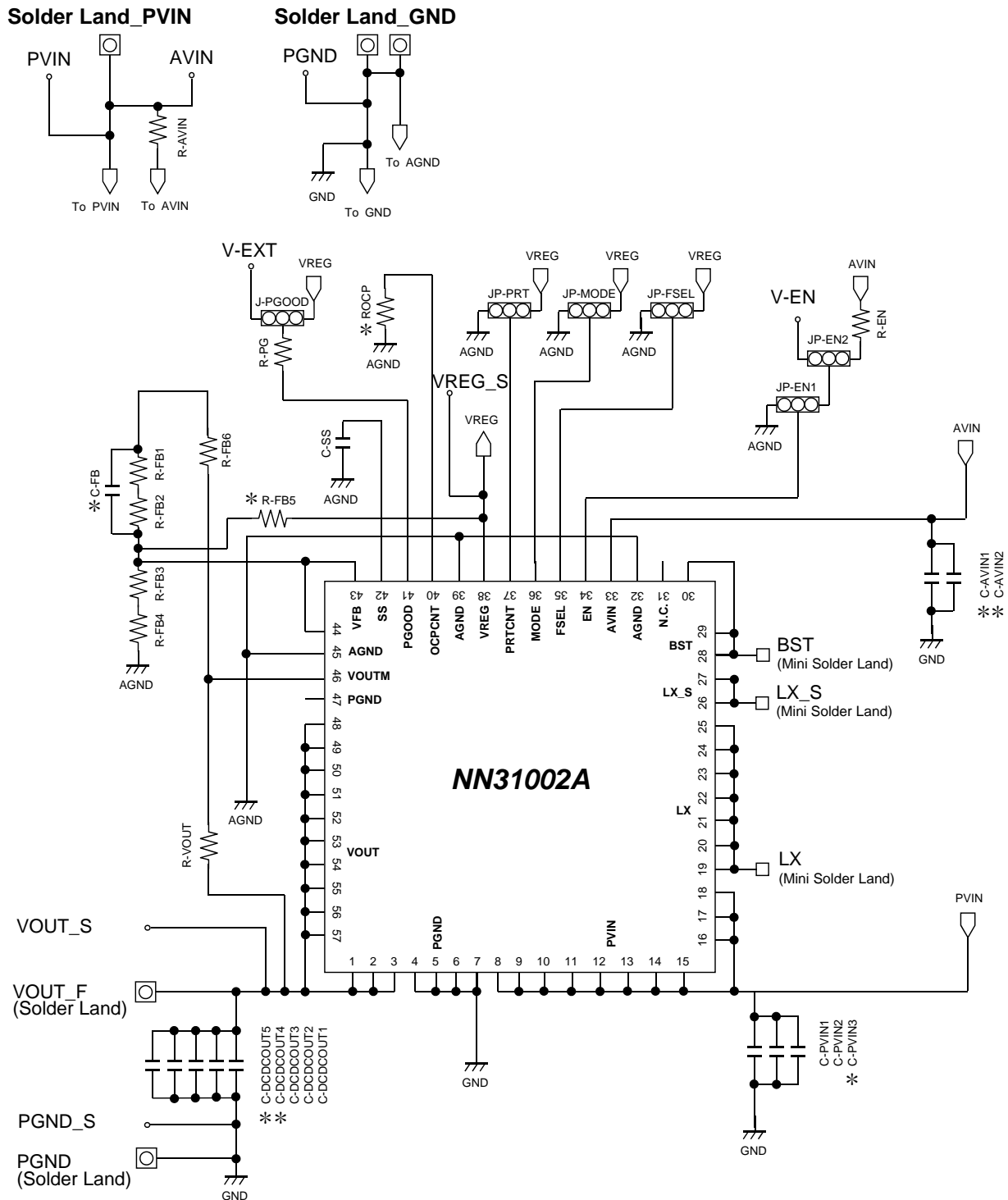


Figure 2. Evaluation Board Schematic

1.5 Start Process

- 1) Set jumper "JP-EN1" to **Low (GND)**.
- 2) Choose jumper setting "JP-EN2" for **EN pin voltage**. (V-EN or AVIN).
- 3) Choose jumper setting "J-PGOOD" for **PGOOD pull up power supply**. (V-EXT or VREG)
- 4) Choose jumper setting "JP-FSEL" for **frequency**. (400KHz , 600KHz or 800KHz)
- 5) Choose jumper setting "JP-MODE" for **DCDC mode**. (FCCM or SKIP)
- 6) Choose jumper setting "JP-PRT" for **Protection mode**.
 - [To VREG] : Latch Mode (OVD and SCP)
 - [To Open] : Latch Mode (OVD) / Auto Recovery Mode (SCP)
 - [To GND] : Auto Recovery Mode (OVD and SCP)
- 7) Supply VIN = 4.5V to 28V(typ:12V) , V-EXT = 3V(for example) , V-EN = 3V(for example) on Evaluation Board.
- 8) Set jumper "JP-EN1" Low to High , DCDC will **Wake up**.

2 Evaluation Board

2.1 Appearance

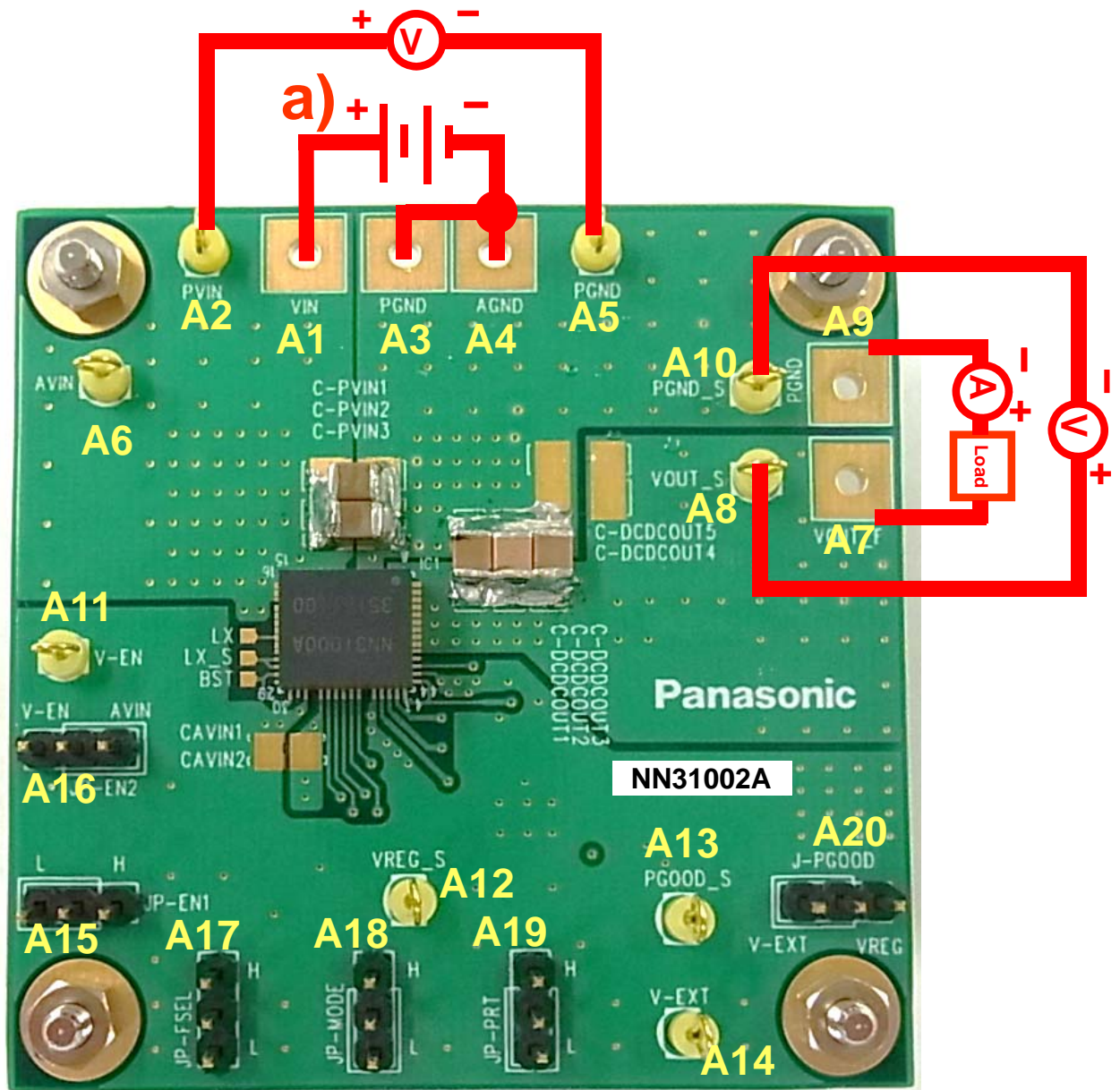


Figure 3. Appearance of Evaluation Board

a) VIN = Main Power supply (4.5V to 28.0V)

2.2 Pin Function (Sense / Force)

Table 3. Pin Function

| No. | NAME | Function | Sense / Force |
|-----|---------|---|---------------|
| A1 | VIN | Power Supply Pin | Force |
| A2 | PVIN | Power Supply Pin | Sense |
| A3 | PGND | GND | Force |
| A4 | AGND | GND | Force |
| A5 | PGND | GND | Sense |
| A6 | AVIN | Power Supply Pin | Sense |
| A7 | VOUT_F | DCDC Output Pin | Force |
| A8 | VOUT_S | DCDC Output Pin | Sense |
| A9 | PGND | GND | Force |
| A10 | PGND_S | GND | Sense |
| A11 | V-EN | Power Supply for Enable | Force |
| A12 | VREG_S | LDO Output Pin | Sense |
| A13 | PGOOD_S | Power Good Open Drain Pin | Sense |
| A14 | V-EXT | External PGOOD Pull Up Power Supply Pin | Force |
| A15 | JP-EN1 | Jumper for Enable/Disable | - |
| A16 | JP-EN2 | Jumper for Enable pull up Voltage | - |
| A17 | JP-FSEL | Jumper for DCDC frequency selection | - |
| A18 | JP-MODE | Jumper for DCDC mode selection | - |
| A19 | JP-PRT | Jumper for protect control selection | - |
| A20 | J-PGOOD | Jumper for PGOOD pull up power supply | - |

2.3 Jumpers Setup

EN pin, FSEL pin, MODE pin, PRTCNT pin and PGOOD pin are able to be controlled by JP-EN1, JP-EN2, JP-FSEL, JP-MODE, JP-PRT and J-PGOOD.

Figure 4. Appearance of JP-EN2, JP-EN1, JP-FSEL

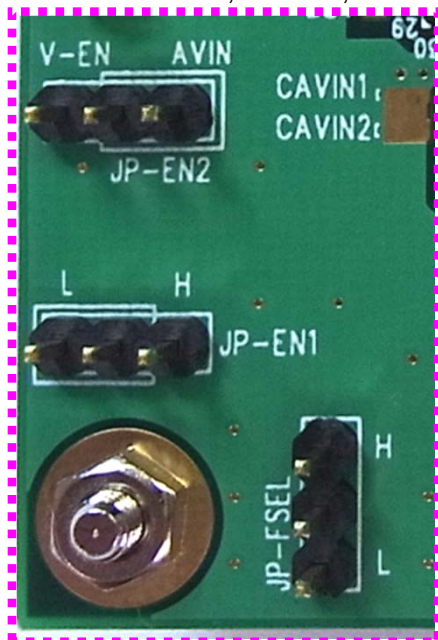


Figure 5. Appearance of JP-MODE, JP-PRT

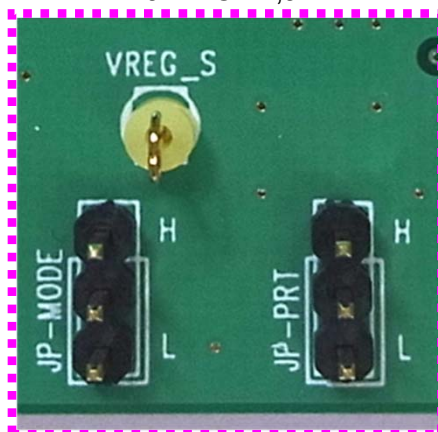


Figure 6. Appearance of J-PGOOD



Table 4. **JP-EN2** (Pull up Voltage of Enable pin)

| Jumper | Connect to V-EN | Short | Short | Connect to AVIN via R-EN |
|------------|-----------------|-------|-------|--------------------------|
| | | | | |
| Pull up to | | V-EN | | AVIN via R-EN |

Table 5. **JP-EN1** (Control Enable / Disable)

| Jumper | Connect to GND | Short | Short | Connect to High |
|--------|----------------|---------|-------|-----------------|
| | | | | |
| Status | | Disable | | Enable |

Table 6. **JP-FSEL** (Control SW Frequency)

| Jumper | Short | Connect to VREG | Open | Short | Connect to GND |
|-----------|-------|-----------------|------|-------|----------------|
| | | | | | |
| Frequency | | 800KHz | | | 400KHz |

Table 7. **JP-MODE** (Control Mode)

| Jumper | Short | Connect to VREG | Short | Connect to GND |
|--------|-------|-----------------|-------|----------------|
| | | | | |
| Mode | | FCCM | | SKIP |

Table 8. **JP-PRT** (Control SW of Protection Mode) OVD : Over Voltage Detection
SCP : Short Circuit Protection

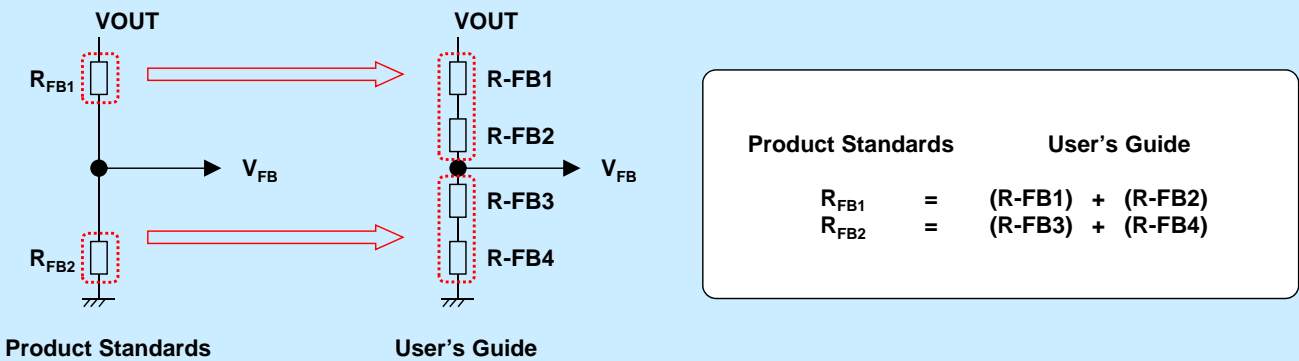
| Jumper | Short | Connect to VREG | Open | Short | Connect to GND |
|--------|-------|-----------------------------|---|-------|--|
| | | | | | |
| Mode | | Latch Mode (OVD and SCP) | OVD:Latch Mode SCP:Auto Recovery Mode | | Auto Recovery Mode (OVD and SCP) |

Table 9. **J-PGOOD** (Control of the Voltage PGOOD pin pull up to)

| Jumper | Connect to V-EXT | Short | Short | Connect to VREG |
|------------|------------------|-------|-------|-----------------|
| | | | | |
| Pull up to | | V-EXT | | VREG |

3 Output Voltage Set Point

The circuit in the Evaluation Board has been modified from the product standards in order to accommodate various output voltage settings.



To change the output voltage of the Evaluation Board, it is necessary to change the value of resister R-FB1~R-FB4.

The values of R-FB1~R-FB4 for a specific output value can be calculated using Equation (1).

For output voltage from 0.6V to 5.5V:

$$V_{out} = \left(\frac{(R-FB1 + R-FB2 + R-FB3 + R-FB4)}{(R-FB3 + R-FB4)} \right) \times 0.6 \quad \text{----- (1)}$$

Table 10 lists the R-FB1~R-FB4 values for some common output voltage.

Table 10. Output Voltages

| Output Voltage (V) | R-FB1(k ohm) | R-FB2(k ohm) | R-FB3(k ohm) | R-FB4(k ohm) |
|--------------------|--------------|--------------|--------------|--------------|
| 1.00 | 0 | 1.0 | 1.5 | 0 |
| 1.20 | 0 | 1.0 | 1.0 | 0 |
| 1.80 | 1.0 | 1.0 | 1.0 | 0 |
| 3.30 | 3.3 | 1.2 | 1.0 | 0 |
| 5.00 | 10.0 | 1.0 | 1.5 | 0 |

Output voltage range

0.6V to 5.5V

Minimum input and output voltage difference

$$V_{IN} \text{ (PVIN) } - V_{OUT} \text{ (DCDC OUT) } = 2.5V$$

4 Bill of Materials

Table 11 presents the bill of materials for the Evaluation Board.

Table 11. Evaluation Board Bill of Materials

| Reference Designator | QTY | Value | Description | Size *2 | Manufacturer | Part Number |
|----------------------|-----|--------|-----------------------------------|---------|--------------|--------------------|
| C-AVIN1 | - | - | - | - | - | - |
| C-AVIN2 | - | - | - | - | - | - |
| C-DCDCOUT1 | 1 | 22uF | Capacitor, Ceramic, 25V, X7R, 10% | 1210 | Murata | GRM32ER71E226KE15# |
| C-DCDCOUT2 | 1 | 22uF | Capacitor, Ceramic, 25V, X7R, 10% | 1210 | Murata | GRM32ER71E226KE15# |
| C-DCDCOUT3 | 1 | 22uF | Capacitor, Ceramic, 25V, X7R, 10% | 1210 | Murata | GRM32ER71E226KE15# |
| C-DCDCOUT4 | - | - | - | - | - | - |
| C-DCDCOUT5 | - | - | - | - | - | - |
| C-PVIN1 | 1 | 10uF | Capacitor, Ceramic, 50V, X7R, 20% | 1210 | TAIYO YUDEN | UMK325AB7106MM-T |
| C-PVIN2 | 1 | 10uF | Capacitor, Ceramic, 50V, X7R, 20% | 1210 | TAIYO YUDEN | UMK325AB7106MM-T |
| C-PVIN3 | - | - | - | - | - | - |
| C-SS | 1 | 4700pF | Capacitor, Ceramic, 50V, X7R, 10% | 0603 | Murata | GRM188R71H472KA01# |
| R-AVIN | 1 | 0 | Resistor, Chip, 0.1W | 0603 | Panasonic | ERJ3GEY0R00V |
| R-FB1 *1 | 1 | 0 | Resistor, Chip, 0.1W | 0603 | Panasonic | ERJ3GEY0R00V |
| R-FB2 *1 | 1 | 1.0k | Resistor, Chip, 0.1W, 1% | 0603 | Panasonic | ERJ3EKF1001V |
| R-FB3 *1 | 1 | 1.5k | Resistor, Chip, 0.1W, 1% | 0603 | Panasonic | ERJ3EKF1501V |
| R-FB4 *1 | 1 | 0 | Resistor, Chip, 0.1W | 0603 | Panasonic | ERJ3GEY0R00V |
| R-FB5 | - | - | - | - | - | - |
| R-FB6 | 1 | 0 | Resistor, Chip, 0.1W | 0603 | Panasonic | ERJ3GEY0R00V |
| R-VOUT | 1 | 0 | Resistor, Chip, 0.1W | 0603 | Panasonic | ERJ3GEY0R00V |
| R-PG | 1 | 100k | Resistor, Chip, 0.1W, 1% | 0603 | Panasonic | ERJ3EKF1003V |
| R-EN | 1 | 220k | Resistor, Chip, 0.1W, 1% | 0603 | Panasonic | ERJ3EKF2203V |
| ROCP | - | - | - | - | - | - |
| C-FB | - | - | - | - | - | - |

*1 : These resistors determine output voltage.

The setting in the above table sets the output voltage for 1.0V.

To change the output voltage, it is necessary to change these resistors following Equation (1) in the section 3.

*2 : These values comply with EIA standards.

5 Board Layout

The board layout for the evaluation board is shown in Figure 7 through Figure 12.

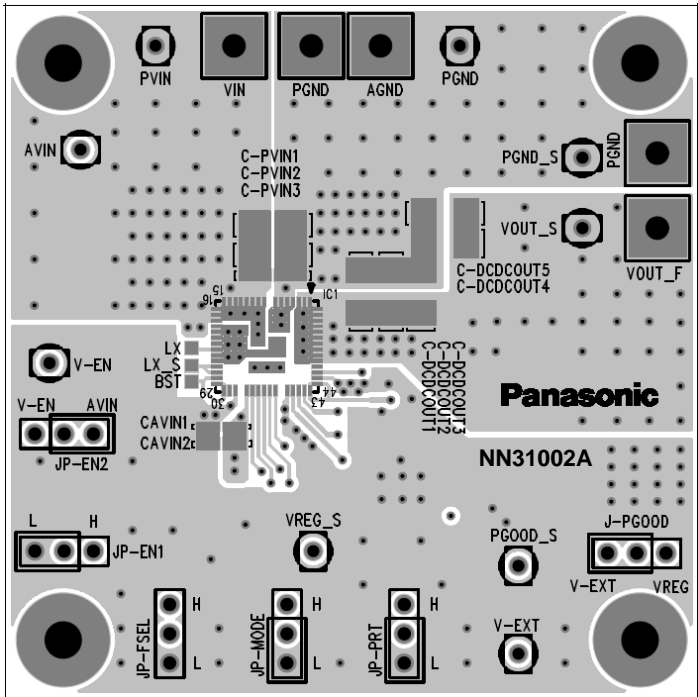


Figure 7. Top Layer with silk screen (Top View)

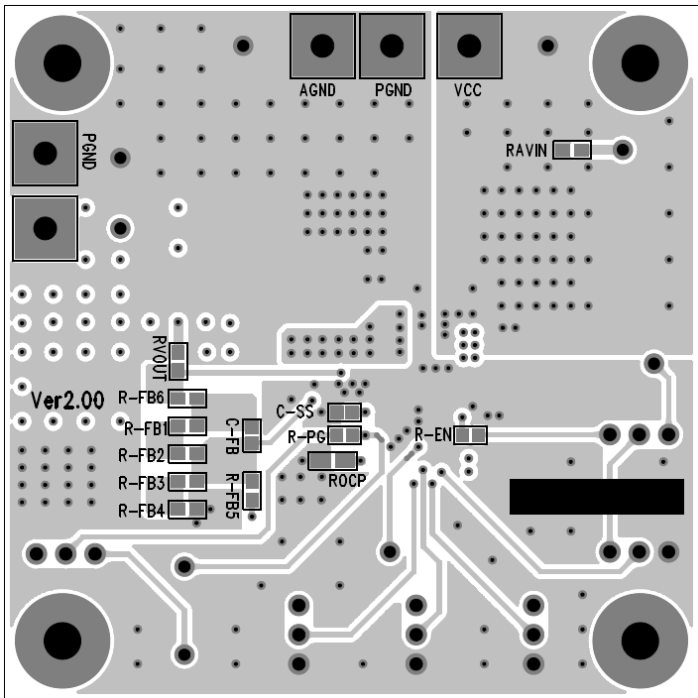


Figure 8. Bottom Layer with silk screen (Bottom View)

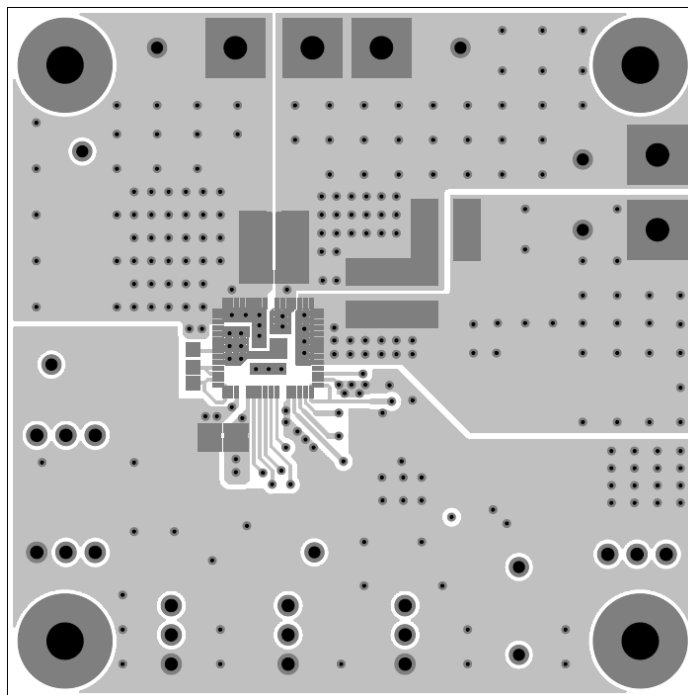


Figure 9. Top Layer (Top View)

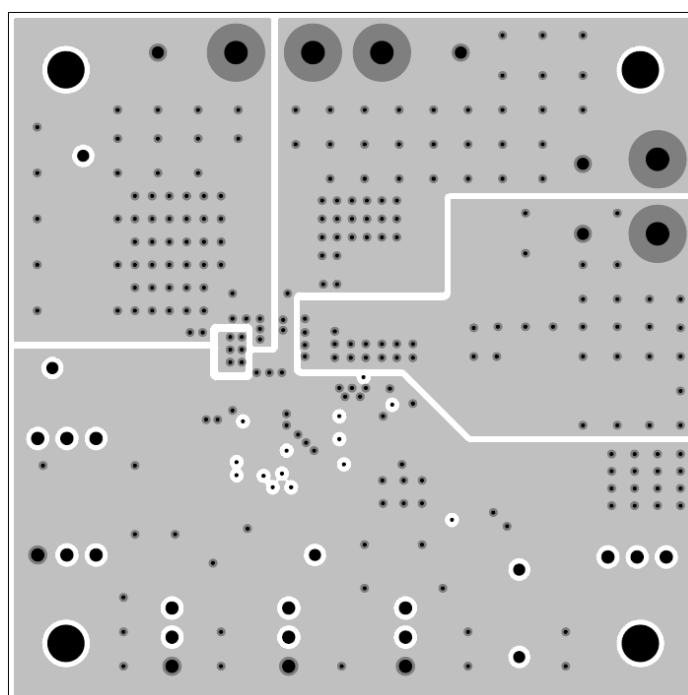


Figure 10. Layer 2 (Top View)

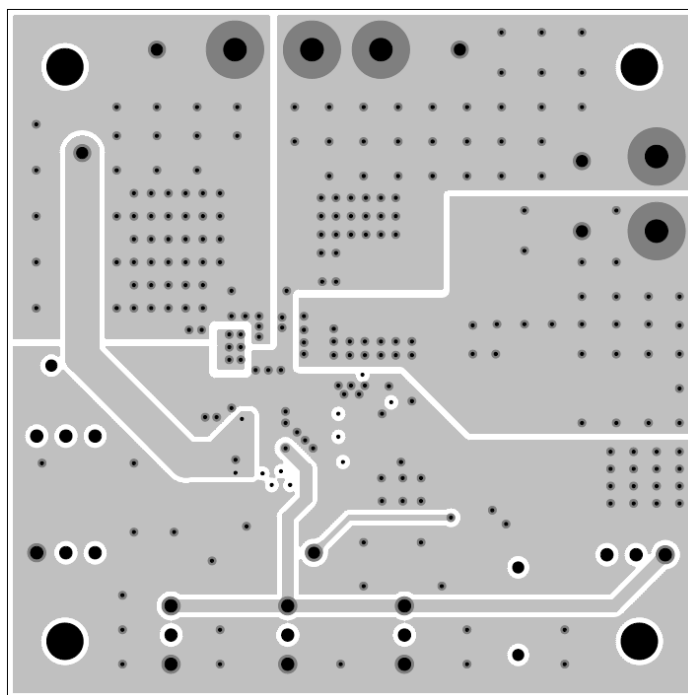


Figure 11. Layer 3 (Top View)

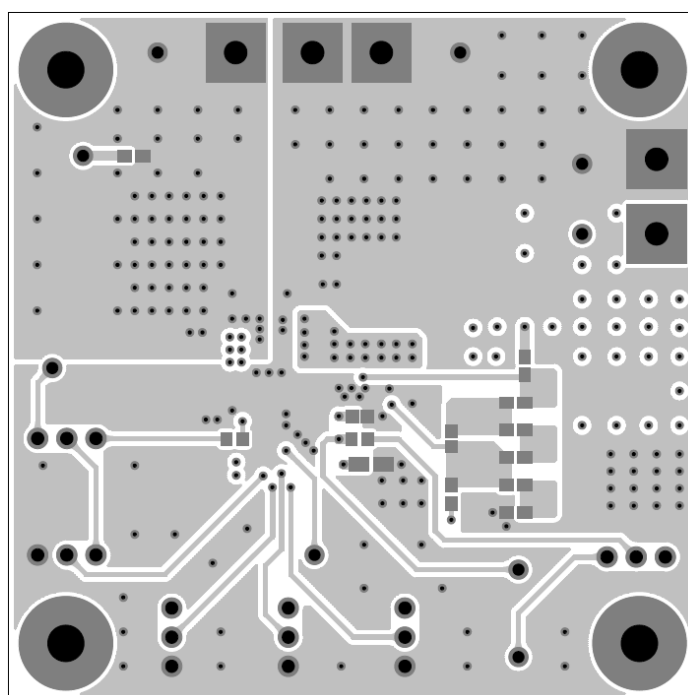


Figure 12. Bottom Layer (Top View)

IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
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 - (7) Weapon
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However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Product which has specified ASO (Area of Safe Operation) should be operated in ASO
13. Verify the risks which might be caused by the malfunctions of external components.
14. Connect the metallic plates (fins) on the back side of the LSI with their respective potentials (AGND, PGND, PVIN, LX, VOUT).
The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates (fins) are connected with their respective potentials.

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