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Specification for Production

Applicant / Manufacturer
Hardware

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Germany

Applicant / Manufacturer
Software

Please refer to chapter 32 / 32.1 Information regarding Software Versions

Software Version

Please refer to chapter 32 / 32.1 Information regarding Software Versions

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Power Electronics R&D Center Wireless Connectivity Panasonic Industrial Devices Europe GmbH	APPROVED genehmigt	CHECKED geprüft	DESIGNED erstellt
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1. SCOPE OF THIS DOCUMENT

This product specification applies to Panasonic's WLAN IEEE 802.11 b/g/n ^{2x2 MIMO} and Bluetooth^{®1} 4.0 High Speed / Low Energy - Radio Module with series number PAN9055 / PAN9045 ([88W8797 from Marvell[®]](#)).

2. HISTORY FOR THIS DOCUMENT

Revision	Date	Modification / Remarks
0.1	July 2014	1 st preliminary version

3. DATA SHEET STATUS

This data sheet contains the PRELIMINARY specification. Supplementary data will be published at a later date.

Panasonic reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Please consult the most recently issued data sheet before initiating or completing a design.

4. RELATED DOCUMENTS

For an update, please search in the suitable homepage.

- [1] PAN9055 and PAN9045 Design-Guide
[TBP](#)
- [2] Semiconductor Datasheet
[88W8797 from Marvell[®]](#)
- [3] Application Note Land Grid Array
<http://www.pideu.panasonic.de/pdf/184ext.pdf>
- [4] REACH and RoHS Certificate
<http://www.pideu.panasonic.de/pdf/182ext2.jpg>

¹ Bluetooth is a registered trademark of the Bluetooth Special Interest Group.

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5. KEY FEATURES

- Surface Mount Type 26.0 x 13.5 x 2.4 mm³
- Wireless Local Area Network (WLAN) and Bluetooth technology
- Operating in the 2.4GHz ISM band
- WLAN 2x2 MIMO operation
- Supports IEEE 802.11
 - IEEE 802.11b/g payload data rates
 - IEEE 802.11n high throughput data rates
 - IEEE 802.11i security standards AES-CCMP, WEP, TKIP, AES-CMAC and WAPI
 - IEEE 802.11e Quality of Service (QoS)
- Supports Bluetooth 4.0 + HS
 - Bluetooth Classic with BT Class 2 or Class 1.5 support
 - Bluetooth High Speed (BT 3.0)
 - Bluetooth Low Energy (BLE)
- Coexistence with cellular and other 2.4GHz on-chip radios
- WLAN Tx power up to +18 dBm (IEEE 802.11b CCK) and +14 dBm (IEEE 802.11g OFDM)
- WLAN High Rx sensitivity
 - -98dBm (IEEE 802.11b DSSS 1Mbps)
 - -76dBm (IEEE 802.11g OFDM 54Mbps)
 - -74dBm (IEEE 802.11n MCS7 HT20 65Mbps)
 - -71dBm (IEEE 802.11n MCS7 HT40 135Mbps)
- Marvell® 88W8797 WLAN / Bluetooth System-on-Chip (SoC) solution inside
- High performance low power CPU core
- Four powerful independent DMA channels
- Power Management Unit with internal Sleep Clock (for Power Save Mode)
- Internal crystal oscillator (38.4MHz)
- USB 2.0, SDIO 3.0 and HS-UART interface
- Integrated shielding to resist EMI
- Manufactured in conformance with RoHS

6. APPLICATIONS FOR THE MODULE

All Embedded Wireless Applications

- | | |
|--|--|
| <ul style="list-style-type: none"> • Platform • Consumer Electronic | <ul style="list-style-type: none"> • Game Console, Imaging • Home AV Entertainment, TV, Set-top Boxes, Media Servers |
| <ul style="list-style-type: none"> • Portable Application • Health & Fitness • Smart Energy | <ul style="list-style-type: none"> • Handsets, AV Device, Tablet, eBook • Home Gateways, Medical devices • Thermostat, Control panels |

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7. WIRELESS LOCAL AREA NETWORK (WLAN)

Wireless Local Area Network (WLAN) is indicating a local radio network meant as a part of the standard IEEE 802.11 family. The IEEE 802.11 is an international standard describing the wireless network. The standard defines the lower layers of the OSI model for wireless communication with the Physical Layer (PHY) and the Data Link Layer (DLL) with its two sub-layers Logical Link Control (LLC) and Media Access Control (MAC). It makes it possible to use any protocol over a IEEE 802.11 wireless network as used at an Ethernet network. Basically WLAN networks using two operating modes for connecting station computers (STA) equipped with a wireless network adapter. The first one is the infrastructure mode where the wireless clients are connected via one or more access points (AP) to a wired network. In this case the network is configured with the same Service Set Identifier (SSID) network name in order to communicate. The second one is the Ad-hoc mode where wireless clients are connected without any access point to the internet.

WLAN devices typically have a higher transmit power to cover a radio range about 100m. Furthermore WLAN is commonly used to transmit high throughput data using upon other the Orthogonal Frequency Division Multiplexing (OFDM) modulation technique. The Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA) mechanism enables the parallel access of more than one device to the media of a IEEE 802.11 network. By implementation of security mechanisms like Advanced Encryption Standard (AES) with Counter Mode CBC-MAC Protocol (CCMP) or Cipher-Based Message Authentication Code (CMAC) and Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP) the network is supporting the security standard IEEE 802.11i. Video, voice and multimedia applications are supported by the IEEE 802.11e Quality of Service amendment.

8. BLUETOOTH 4.0

Bluetooth Low Energy (BLE) is a part of Bluetooth Version 4.0, which covers both BLE as well as BT Classic 2.1 and 3.0. If both are implemented in one device it is called dual mode. Dual mode chips implement the low energy specification, providing connectivity to battery applications. Dual mode combines low energy with the power of classic Bluetooth and are likely to become a de facto feature in almost all new Bluetooth enabled cellular phones, computers or portable communication nodes.

Bluetooth Low Energy (BLE) is not backwards compatible with previous Bluetooth classic standards (2.1+EDR or 3.0). Dual mode Bluetooth 4.0 is backwards compatible but is not practical for low power devices but targeted to gateway products.

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9. DESCRIPTION FOR THE MODULE

The ENWF9101x1yF is a 2.4GHz ISM band wireless radio module for implementing WLAN and Bluetooth functionality into various electronic devices. A block diagram can be found in chapter 17.

The ENWF9101x1yF is a cost-effective, low-power operation, system-on-chip (SoC) solution for WLAN and Bluetooth applications. It enables wireless network adapters and cards to be built with low total bill-of-material costs. The ENWF9101x1yF combines an excellent IEEE 802.11 and BT4.0 wireless radio, baseband processor, medium access controller, encryption unit, CPU, boot ROM with patching capability, internal SRAM, in-system programmable flash memory and many other powerful supporting features and peripherals. The low-power operation supporting deep sleep and standby modes by using the on-board power management unit. The ENWF9101x1yF is suitable for wireless network systems based on WLAN IEEE 802.11 b/g/n and Bluetooth BT4.0 (2.4GHz) where small form factor, highly integration, high throughput data rates and low RF expertise are required.

Panasonic offers the software package supporting various Fedora Core Kernel versions. It includes the WLAN/BT SoC Firmware binary that powers the WLAN/BT SoC for client (STA), micro access point (uAP), Ad-hoc mode (Wi-Fi direct), Bluetooth Classic, High Speed and Low Energy (BLE) applications. In addition it includes the HOST Driver-Firmware Interface (API) which represents the interface between the host driver and SoC firmware.

For WLAN the Driver-Firmware Interface handles all 802.11 MAC management tasks by converting standard 802.3 frames to the SoC firmware to transmit over the wireless link as 802.11 frames and processes the received 802.11 frames and converts them into 802.3 frames before forwarding them to the host driver. The HOST driver is separated in three modules. The Standard Ethernet driver, the 802.11 Extensions and the Hardware Interface Driver. The 802.11 Extensions module extends the Standard Ethernet driver in order to view and control the state of the WLAN adapter. For Bluetooth the Driver-Firmware Interface handles the BT Baseband, Link Manager Protocol (LMP) and HCI functionality in cooperation with the CPU.

The Hardware Interface Driver controls the hardware interface on the HOST side. Furtheron the software package from Marvell® consists of various applications, demonstrations and utilities.

Refer to [1] PAN9055 and PAN9045 Design-Guide and chapter 32. Ordering Information.

Please contact your local sales office for further details on additional options and services:

www.panasonic.com/rfmodules for the US,

http://industrial.panasonic.com/eu/i/29606/wireless_modules/wireless_modules.html for EU

or write an e-mail to wireless@eu.panasonic.com.

10. DIFFERENCE PAN9055 TO PAN9045

The PAN9045 is the non antenna version with two bottom pads where the PAN9055 is the version with two antennas.

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11. DETAILED DESCRIPTION

11.1. PAN9055 / PAN9045 TERMINAL LAYOUT

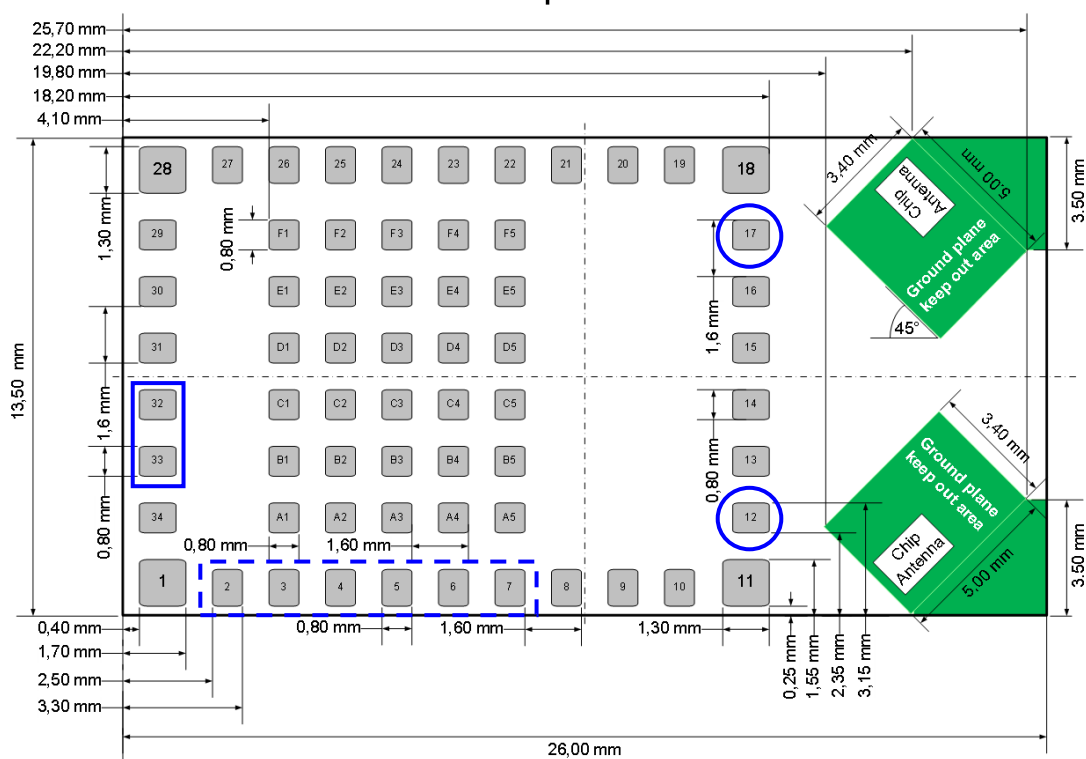
The USB pins are marked with a blue rectangular box.

The SDIO pins are marked with a blue dashed rectangular box.

The two PAN9045 antenna pins are marked with blue circles.

Top View, Application PCB

Top View



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11.2. PAN9055 / PAN9045 COMMON TERMINAL PIN-CONFIGURATION

No	Pin Name	Pin Type	Description
1	GND	Ground Pin	Connect to Ground
2..7	...	...	... for SDIO specific terminals see chapter 11.3
8	RESE _{Tn}	Input Signal	Reset, active-low
9	PD _n	Input Signal	Power down, active-low
10	S_CSN / CON2	Output / Input	S_CSN: Chip Select for external SPI EEPROM, chip select from the SoC CON2: Firmware Boot option
11	GND	Ground Pin	Connect to Ground
12	NC	NC	... for PAN9045 see chapter 11.4
13	GND	Ground Pin	Connect to Ground
14	GND	Ground Pin	Connect to Ground
15	GND	Ground Pin	Connect to Ground
16	GND	Ground Pin	Connect to Ground
17	NC	NC	... for PAN9045 see chapter 11.4
18	GND	Ground Pin	Connect to Ground
19	3.3V RF	Power	3.0V – 3.6V power supply connection
20	3.3V RF	Power	3.0V – 3.6V power supply connection
21	CON0	Digital I/O	CON0: Firmware Boot option see chapter
22	CON1	Digital I/O	CON1: Firmware Boot option see chapter
23	UART_SOUT	Output Signal	Serial data output to modem, data set, or peripheral device
24	UART_SIN	Input Signal	Serial data input from modem, data set, or peripheral device
25	UART_RTS	Output Signal	Request-to-Send output to modem, data set, or peripheral device (active low)
26	UART_CTS	Input Signal	Clear-to-Send input from modem, data set, or peripheral device (active low)
27	GPIO4	Digital I/O	Port 4 – GPIO[4]
28	GND	Ground Pin	Connect to Ground
29	3.3V	Power	3.0V – 3.6V power supply connection
30	3.3V	Power	3.0V – 3.6V power supply connection
31	3.3V USB	Power	3.0V – 3.6V power supply connection
32	USB_DMNS	D-	USB Bus Data Minus
33	USB_DPLS	D+	USB Bus Data Plus
34	SD_VIO	Power	1.8V or 3.3V Digital I/O SDIO Power Supply
A1	TMS / BT_FREQ	Input Signal	TMS: JTAG controller select BT_FREQ: Information BT using channel which overlaps WLAN channel or not
A2	TDO / BT_REQ	Output / Input	TDO: JTAG test data output / BT_REQ: BT device request access to medium
A3	S_WB	Input Signal	Serial Read/Write Control Signal input, SPI EEPROM serial data to the SoC
A4	S_CLK	Output Signal	Serial Clock Signal output, SPI EEPROM serial clock from the SoC
A5	S_DAT	Output Signal	Serial Data output, SPI EEPROM serial data from the SoC
B1	TCK / BT_GRANT _n	Input / Output	TCK: JTAG test clock BT_GRANT _n : Indicate permission to transmit, low BT can transmit
B2	TDI / BT_STATE	Input Signal	TDI: JTAG test data input BT_STATE: Information BT_REQ priority (1- or 2-bit) and direction BT RX/TX
B3	GND	Ground Pin	Connect to Ground
B4	GND	Ground Pin	Connect to Ground
B5	GND	Ground Pin	Connect to Ground
C1	CHIP_WAKEUP	Digital I/O	Port 18 – optional GPIO[18] or Host-to-Chip wake-up
C2	I2S2_LRCLK	Output / Input	I ² S Audio Left/Right Clock, Master mode as output, Slave mode as input
C3	GND	Ground Pin	Connect to Ground
C4	GND	Ground Pin	Connect to Ground
C5	GND	Ground Pin	Connect to Ground
D1	I2S2_DOUT	Output Signal	I ² S Audio output data (for playback)
D2	I2S2_DIN	Input Signal	I ² S Audio input data (for recording)
D3	PCM_SYNC	Input / Output	PCM Sync Pulse Signal, output if PCM Master, input if PCM Slave
D4	GND	Ground Pin	Connect to Ground
D5	GND	Ground Pin	Connect to Ground
E1	I2S2_BCLK	Input / Output	I ² S Audio Bit Clock, Master mode as output, Slave mode as input
E2	LED1	Digital Output	Port 17 – LED output with typ. 10mA drive capability
E3	PCM_CLK	Input / Output	PCM Clock Signal, output if PCM Master, input if PCM Slave
E4	GND	Ground Pin	Connect to Ground
E5	PCM_DOUT	Output Signal	PCM Data Output Signal
F1	HOST_WAKEUP	Digital I/O	Port 16 – optional GPIO[16] or Chip-to-Host wake-up
F2	LED0	Digital Output	Port 1 – LED output with typ. 10mA drive capability
F3	PCM_DIN	Input Signal	PCM Data Input Signal
F4	PCM_MCLK	Output Signal	PCM Clock Signal, optional clock used for some codec derived from PCM_CLK
F5	GND	Ground Pin	Connect to Ground

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11.3. PAN9055 / PAN9045 SDIO SPECIFIC TERMINAL PIN-CONFIGURATION

No	Pin Name	Pin Type	Description		
			4-bit mode	1-bit mode	SPI mode
2	SD_CMD	Digital I/O	-	Command Line	Data Input
3	SD_DAT[0]	Digital I/O	Data Line bit [0]	Data Line	Data Output
4	SD_DAT[1]	Digital I/O	Data Line bit [1]	Interrupt	Interrupt
5	SD_DAT[2]	Digital I/O	Data Line bit [2] or ... Read Wait (optional)		Reserved
6	SD_DAT[3]	Digital I/O	Data Line bit [3]	Not used	Chip Select, active low
7	SD_CLK	Digital I/O	Clock	Clock	Clock

11.4. PAN9045 RF-TERMINAL PIN-CONFIGURATIONS

No	Pin Name	Pin Type	Description
12	RF_B	RF Port B	50Ω bottom pad
17	RF_A	RF Port A	50Ω bottom pad

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12. GENERAL FEATURES

- Embedded WLAN / BT SoC with following features:
 - Integrated CPU with maximum clock speed of 256 MHz
 - Single-chip integration of IEEE 802.11 2x2 MIMO and BT4.0 wireless radio, baseband, MAC, CPU, memory and HOST interface
 - SRAM for Tx frame queues and Rx data buffer
 - Boot ROM and ROM patching capability
 - Independent Four-Channel Direct Memory Access (DMA)
 - Low power operation supporting deep sleep and stand-by modes
 - Optional power management with internal sleep clock crystal unit for near zero deep sleep

13. HOST INTERFACES

13.1. USB 2.0 INTERFACE

- Compliant with the Universal Serial Bus Specification, Revision 2.0
- Allows HOST controller using USB cable bus and USB 2.0 device interface
- High/full speed operation with (480/12 Mbps)
- Suspend / host resume / device resume (remote wake-up)
- Supports Link Power Management (LPM), corresponding host resume or device resume (remote wakeup) to exit from L1 sleep state
- USB 2.0 device interface with integrated level shifter for 3.3V signal level

13.2. SDIO 3.0 INTERFACE

- Supports SDIO 3.0 Standard
- SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification
- Supports SPI, 1-bit SDIO and 4-bit SDIO transfer modes at the full clock range of 0 to 100MHz
- Special interrupt register for information exchange
- Allows card to interrupt host
- SoC acts as a device on a SDIO bus

13.3. HIGH-SPEED UART INTERFACE

- Supports high-speed Universal Asynchronous Receiver / Transmitter (UART) interface
- Compliant with the industry standard 16550 specification
- High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data
- FIFO mode permanently selected for transmit and receive operations
- Two pins for transmit, receive and two for flow control
- Interrupt triggers for low-power, high throughput operation

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14. PERIPHERAL BUS INTERFACE

- Embedded SoC with following features:
 - Clocked Serial Unit (CSU)
 - 2-Wire Serial Interface (TWSI)
 - 1-Wire Serial Interface
 - SPI Serial (EEPROM) Interface
 - General-Purpose I/O (GPIO) Interface
 - User-defined GPIOs, I/O configured to either input or output
 - GPIOs independently controlled
 - Two GPIOs with LED output functionality
 - ❖ LED Pulse Stretching to observe short duration of status events
 - ❖ Two software controlled blink rates to indicate events
 - One-Time Programmable Memory (OTP)
 - Storing calibration data and hardware information of the device
 - Programmed during production process of device
 - Device performs calibration when it is powered up

15. AUDIO INTERFACE FEATURES

15.1. AUDIO CODEC INTERFACE

- Class D Audio Amplifier
- I²S (Inter-IC Sound) interface for audio data connection to ADC and DAC
- Master and slave mode for I²S, MSB and LSB audio interfaces
- Tri-state I²S interface capability

15.2. PCM INTERFACE

- Master or slave mode
- PCM bit width size of 8 bits or 16 bits
- Up to 4 slots with configurable bit width and start positions
- Short frame and long frame synchronization
- Tri-state PCM interface capability

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16. WLAN FEATURES

16.1. IEEE 802.11 / STANDARDS

- 802.11 data rates 1 and 2 Mbps (DSSS)
- 802.11b data rates 5.5 and 11 Mbps (CCK)
- 802.11g data rates 6, 9, 12, 18, 24, 36, 48 and 54 Mbps (OFDM)
- 802.11b/g performance enhancements
- 802.11n compliant with maximum data rates up to 145 Mbps (20 MHz channel) and 300 Mbps (40 MHz channel)
- 802.11d international roaming
- 802.11i enhanced security (WEP, WPA, WPA2)
- 802.11k radio resource measurement
- 802.11n block acknowledgement extensions
- 802.11r fast hand-off for AP roaming
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode
- Wi-Fi Direct connectivity

16.2. WLAN MAC

- Ad-Hoc and Infrastructure Modes
- RTS/CTS for operation und DCF
- Hardware filtering of 32 multicast addresses and duplicate frame detection for up to 32 unicast addresses
- WLAN SoC with Tx and Rx FIFO for maximum throughput
- Open System and Shared Key Authentication services
- A-MPDU Rx (de-aggregation) and Tx (aggregation)
- 20/40 MHz channel coexistence
- Reduced Inter-Frame Spacing (RIFS) receive
- Management Information Base (MIB) counter
- Radio resource measurement counters
- Quality of service queues
- Block acknowledgement with 802.11n extensions
- Beamforming
 - Supports beamforming to 802.11n MIMO and SISO devices
 - 802.11n explicit beamformer, supports NDP and Stagger sounding
 - 802.11n explicit beamformee, supports immediate feedback generation using un-compress and compress steering matrix or delayed feedback of all feedback types
- TIM frame transition
- Multiple-BSSID and Multiple-Station operation
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Marvell® Mobile Hotspot technology (MMH)

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16.3. WLAN BASEBAND

- 802.11n 2x2 MIMO (WLAN SoC with MIMO RF radio)
- Backward compatibility with legacy 802.11b/g technology
- WLAN / Bluetooth LNA sharing
- PHY data rates up to 300 Mbps (802.11n – MCS15)
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz packets in 40 MHz channel and 20 MHz duplicate legacy packets in 40 MHz channel mode operation
- Modulation and Coding Scheme MCS 0 ~ 15 and MCS 32 (duplicate 6 Mbps)
- Radio resource measurement
- Optional 802.11n MIMO features:
 - 20/40 MHz coexistence
 - 1 spatial stream Space-Time-Block-Coding (STBC) reception and transmission
 - Short Guard Interval
 - RIFS on receive path
 - Implicit beamforming
 - Explicit beamformer and beamformee support
 - Greenfield Tx/Rx
- Power save features

16.4. WLAN RADIO

- 20 and 40 MHz channel bandwidth
- Shared WLAN / Bluetooth receive input scheme for 2.4 GHz band
- Embedded WLAN SoC with following features:
 - Direct conversion radio (no SAW filter)
 - Closed/Open loop power control (0.5 dB step increments)
 - Optimized Tx gain distribution for linearity and noise performance
 - Fine channel step with AFC (adaptive frequency control)

16.5. WLAN RF PATH

- Shared WLAN / Bluetooth receive input scheme for 2.4 GHz band
- Two RF pathes with following features:
 - Two separate Front-End-Modules (FEM) for each RF path
 - 1st FEM with integrated 2.4GHz Tx/Rx switch, Power Amplifier (PA) and Low Noise Amplifier (LNA) path
 - 2nd FEM with integrated 2.4GHz Tx/Rx/BT switch, Power Amplifier (PA), Low Noise Amplifier (LNA) and RF Bypass path
 - Gain selectable LNAs with optimized noise figure and power consumption
 - Power Amplifiers with power control

16.6. WLAN ENCRYPTION

- Embedded WLAN SoC with following features:
 - WEP 64-bit and 128-bit encryption with hardware TKIP processing (WPA)
 - AES-CCMP hardware implementation as part of 802.11i security standard (WPA2)
 - Enhanced AES engine performance
 - AES-Chipher-Based Message Authentication Code (CMAC) as part of the 802.11w security standard
 - WLAN Authentication and Privacy Infrastructure (WAPI)

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17. BLUETOOTH FEATURES

17.1. GENERAL

- Supports Bluetooth 4.0 + High Speed
- Shared Tx/Rx path for Bluetooth
- Digital Audio Interface including PCM interface for voice applications and I²S for digital stereo applications
- BDR/EDR, BLE and WLAN coexistence
- WLAN/Bluetooth Coexistence (BCA) protocol support

17.2. BLUETOOTH CLASSIC

- Bluetooth Classic with BT Class 2 or Class 1.5 support
- Bluetooth High Speed (BT 3.0)
- Baseband and radio Basic Data Rate (BDR) and Enhanced Data Rate (EDR) packet types with 1Mbps (GFSK), 2Mbps ($\pi/4$ -DQPSK) and 3Mbps (8DPSK)
- Fully functional Bluetooth baseband with Adaptive Frequency Hopping (AFH), forward error correction, header error control, access code correlation, CRC, encryption bit stream generation and whitening
- Adaptive Frequency Hopping (AFH) including Packet Loss Rate (PLR) and RSSI
- Interlaced scan for faster connection setup
- Simultaneous active ACL connection support
- Automatic ACL packet type selection
- Full master and slave piconet support
- Scatternet support
- Standard UART and SDIO HCI transport layer
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard SCO/eSCO voice coding
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanism (i.e. hold, sniff modes and sniff-sub rating)
- Enhanced low power scan mode
- Enhanced Power Control (EPC)
- Channel Quality Driven (CQD) data rate
- SBC off load for A2DP streaming
- Wideband Speech (WBS) support (1 WBS link)

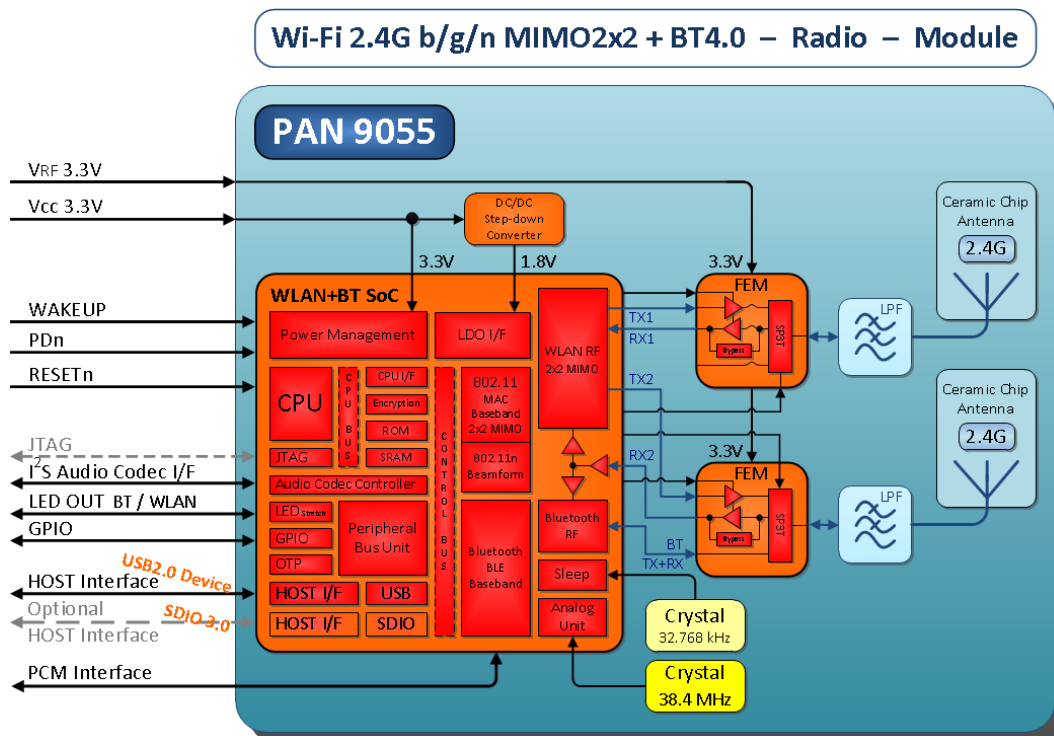
17.3. BLUETOOTH LOW ENERGY (BLE)

- Advertiser, Scanner, Initiator, Master and Slave roles support (connects up to 16 links)
- Shared RF with BDR/EDR
- Encryption AES support
- Hardware support for intelligent Adaptive Frequency Hopping (AFH)

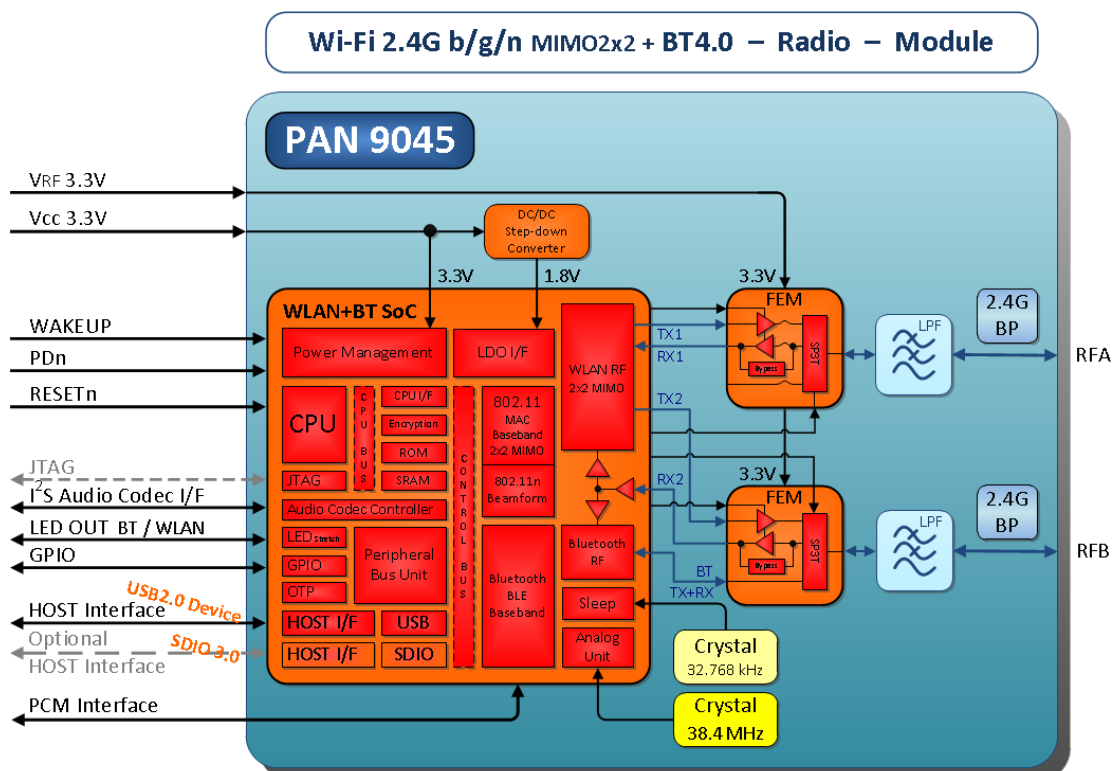
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18. PAN9055 / PAN9045 BLOCK DIAGRAM

18.1. PAN9055 VARIANT



18.2. PAN9045 VARIANT



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19. KEY PARTS LIST

Part Name	Material
P.W.Board	Glass cloth epoxide resin with gold plating
Casing	Material: C7521 or ZSNC S1S8 8/8, thickness 0.30mm
IC part name	88W8797 (Marvell®, www.marvell.com)

20. TEST CONDITIONS

Measurements shall be made under operating free-air temperature range unless otherwise specified.

Temperature	25 ± 10°C
Humidity	40 to 85%RH
Supply Voltage	3.3V

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21. GENERAL REQUIREMENTS AND OPERATION

All specifications are over temperature and process, unless indicated otherwise.

21.1. ABSOLUTE MAXIMUM RATINGS

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the module will result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T _{STOR}	Storage temperature		-40		+125	°C
V _{ESD}	ESD robustness	All pads, according to human-body model, JEDEC STD 22, method A114			1000	V
		According to charged-device model, JEDEC STD 22, method C101			500	V
P _{RF}	RF input level				+20	dBm
V _{DDMAX}	Maximum voltage	Maximum power supply voltage from any pin with respect to V _{SS} (GND)	-0.3		3.9	V
V _{IO}	Voltage on any digital pin	GPIOs, PDn, RESETn, Coex I/F	-0.3		V _{DDMAX}	V
V _{USBMAX}	USB Maximum voltage	Maximum power supply voltage from any pin with respect to V _{SS} (GND)	-0.3		3.9	V
V _{IO_SD}	3V3 SDIO Maximum voltage	Maximum power supply voltage from any pin with respect to V _{SS} (GND)	-0.3		3.9	V
	1V8 SDIO Maximum voltage		-0.3		2.1	V

21.2. RECOMMENDED OPERATING CONDITIONS

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the module will result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T _A	Ambient operating temperature range	Commercial Grade (refer to chapter 32.)	0		+70	°C
		Extended Grade (refer to chapter 32.)	-30		+85	°C
V _{DD}	3V3 Supply voltage ²	Voltage on pins 19 / 20 (3.3V RF), 29 / 30 (3.3V) I/O supply voltage V _{IO} internally connected to V _{DD}	3.0	3.3	3.6	V
V _{USB}	3V3 USB Supply voltage ²	Voltage on pin 31 (3.3V USB) Supply voltage V _{USB} connected to 3.3V USB	3.0	3.3	3.6	V
V _{IO_SD}	3V3 SDIO Supply voltage ²	Voltage on pin 34 (SD_VIO) Supply voltage V _{IO_SD} connected to SD_VIO	3.0	3.3	3.6	V
	1V8 SDIO Supply voltage ²	Voltage on pin 34 (SD_VIO) Supply voltage V _{IO_SD} connected to SD_VIO	1.6	1.8	2.0	V

² The supply current must be limited to max. 1A

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21.3. DIGITAL PIN CHARACTERISTICS

21.3.1. VIO with V_{DD} 3.3V Operation for GPIO's

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V _{IH}	High level input voltage ³	3.3V Operation (V _{IO} = V _{DD})	0.7V _{DD}		V _{DD} +0.3	V
V _{IL}	Low level input voltage ³	3.3V Operation (V _{IO} = V _{DD})	-0.3		0.3V _{DD}	V
V _{HYS}	Input hysteresis voltage ³	3.3V Operation (V _{IO} = V _{DD})	200			mV
V _{OH}	High level output voltage ³	3.3V Operation (V _{IO} = V _{DD})	V _{DD} - 0.4			V
V _{OL}	Low level output voltage ³	3.3V Operation (V _{IO} = V _{DD})			0.4	V

21.3.2. SD_VIO 1.8V Operation for SDIO I/F

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V _{IH}	High level input voltage ³	1.8V Operation (V _{IO_SD} = 1.8V)	0.7V _{IO_SD}		V _{IO_SD} +0.3	V
V _{IL}	Low level input voltage ³	1.8V Operation (V _{IO_SD} = 1.8V)	-0.3		0.3V _{IO_SD}	V
V _{HYS}	Input hysteresis voltage ³	1.8V Operation (V _{IO_SD} = 1.8V)	150			mV
V _{OH}	High level output voltage ³	1.8V Operation (V _{IO_SD} = 1.8V)	V _{IO_SD} - 0.4			V
V _{OL}	Low level output voltage ³	1.8V Operation (V _{IO_SD} = 1.8V)			0.4	V

21.3.1. SD_VIO 3.3V Operation for SDIO I/F

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V _{IH}	High level input voltage ³	3.3V Operation (V _{IO_SD} = 3.3V)	0.7V _{IO_SD}		V _{IO_SD} +0.3	V
V _{IL}	Low level input voltage ³	3.3V Operation (V _{IO_SD} = 3.3V)	-0.3		0.3V _{IO_SD}	V
V _{HYS}	Input hysteresis voltage ³	3.3V Operation (V _{IO_SD} = 3.3V)	200			mV
V _{OH}	High level output voltage ³	3.3V Operation (V _{IO_SD} = 3.3V)	V _{IO_SD} - 0.4			V
V _{OL}	Low level output voltage ³	3.3V Operation (V _{IO_SD} = 3.3V)			0.4	V

³ The capacitive load should not be larger than 50 pF for all I/O's when using the default driver strength settings. Generally, large capacitance loads increase the overall current consumption.

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21.4. ELECTRICAL CHARACTERISTICS

The current consumption depends on the user scenario and the setup and timing in the power modes. Assume $V_{DD} = 3.3V$, $T_{amb} = 25^{\circ}C$ if nothing else stated

21.4.1. Current consumption WLAN and Bluetooth with USB I/F

Symbol	Parameter Current Consumption	Mode	Condition	Min.	Typ.	Max.	Units
I _{TX WLAN}	Active Transmit ⁴	WLAN ⁵	P _{TX} = +18 dBm for 802.11b @ 11 Mbps		TBD		mA
			P _{TX} = +14 dBm for 802.11g @ 54 Mbps				mA
			P _{TX} = +13 dBm 802.11n @ MCS7 / 72Mbps / HT20 / 1x1 MIMO				mA
			P _{TX} = +13 dBm 802.11n @ MCS15 / 150Mbps / HT40 / 1x1 MIMO				mA
			P _{TX} = +13 dBm 802.11n @ MCS7 / 144.5Mbps / HT20 / 2x2 MIMO				mA
			P _{TX} = +13 dBm 802.11n @ MCS15 / 300Mbps / HT40 / 2x2 MIMO				mA
I _{RX WLAN}	Active Receive ⁶		802.11b @ 11 Mbps				mA
			802.11g @ 54 Mbps				mA
			802.11n @ MCS7 / 72Mbps / HT20 / 1x1 MIMO				mA
			802.11n @ MCS15 / 150Mbps / HT40 / 1x1 MIMO				mA
			802.11n @ MCS7 / 144.5Mbps / HT20 / 2x2 MIMO				mA
			802.11n @ MCS15 / 300Mbps / HT40 / 2x2 MIMO				mA
I _{IEEE-PS}	IEEE Power Save ⁷	DTIM = 1 with beacon interval 100ms				μA	
I _{TX BT}	Peak BT	BT (BDR) (EDR)	P _{TX BT} = +4 dBm / USB Active				mA
P _{TX BT} = +4 dBm / USB Suspend ⁸						mA	
I _{RX BT}			USB Active				mA
			USB Suspend				mA
I _{SCAN BT}	Page / Inquiry Scan		1.28s @ normal mode				mA
I _{SNIFF BT}	ACL Sniff		1.28s				mA
I _{A2DP BT}	A2DP		BDR / EDR @ 330 Kbps (3M baud rate)				mA
I _{TX BLE}	Peak BLE	BLE	P _{TX BLE} = +4 dBm				mA
I _{RX BLE}							mA
I _{PDn}	Power Down ⁹	WLAN and BT	Grounding of PDn pin				μA
I _{DeepSleep}	Deep Sleep ¹⁰		Low-power state used in sleep state				μA

⁴ Peak values for specified output power level and data rate with UDP traffic between the AP and Device (STA).

⁵ Using WLAN Client mode. Bluetooth is in Deep Sleep during this mode.

⁶ Peak values for specified data rate with UDP traffic between the AP and DUT.

⁷ In IEEE Power Save the device automatically wakes up on beacons. This is dependent on the DTIM value of the AP it is connected to. If it is a DTIM value of 1 along with a beacon interval of 100ms, the device wakes up every 100ms.

⁸ USB Suspend Mode is valid only for the USB Host interface. The low-power device automatically enters a suspend state after 3ms of no bus activity.

⁹ Power Down state can be achieved by grounding the PDn pin. All internal clocks are shut down, the registers and memory are not maintained. Upon exiting power down mode, a reset is automatically performed and a firmware re-download is required.

¹⁰ It is a low-power mode used in the deep sleep state of power save mode. In this case the external reference clock and many WLAN SoC specific blocks are switched-off. Only an internal slow sleep clock is used to maintain register and memory states.

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21.4.2. Current consumption WLAN and Bluetooth with SDIO I/F

Symbol	Parameter Current Consumption	Mode	Condition	Min.	Typ.	Max.	Units
I _{TX WLAN}	Active Transmit	WLAN	P _{TX} = +18 dBm for 802.11b @ 11 Mbps		TBD		mA
			P _{TX} = +14 dBm for 802.11g @ 54 Mbps				mA
			P _{TX} = +13 dBm 802.11n @ MCS7 / 72Mbps / HT20 / 1x1 MIMO				mA
			P _{TX} = +13 dBm 802.11n @ MCS15 / 150Mbps / HT40 / 1x1 MIMO				mA
			P _{TX} = +13 dBm 802.11n @ MCS7 / 144.5Mbps / HT20 / 2x2 MIMO				mA
			P _{TX} = +13 dBm 802.11n @ MCS15 / 300Mbps / HT40 / 2x2 MIMO				mA
I _{RX WLAN}	Active Receive		802.11b @ 11 Mbps				mA
			802.11g @ 54 Mbps				mA
			802.11n @ MCS7 / 72Mbps / HT20 / 1x1 MIMO				mA
			802.11n @ MCS15 / 150Mbps / HT40 / 1x1 MIMO				mA
			802.11n @ MCS7 / 144.5Mbps / HT20 / 2x2 MIMO				mA
			802.11n @ MCS15 / 300Mbps / HT40 / 2x2 MIMO				mA
I _{IEEE-PS}	IEEE Power Save		DTIM = 1 with beacon interval 100ms				μA
I _{TX BT}	Peak BT	BT (BDR) (EDR)	P _{TX BT} = +4 dBm / USB Active				mA
P _{TX BT} = +4 dBm / USB Suspend						mA	
I _{RX BT}			USB Active				mA
			USB Suspend				mA
I _{SCAN BT}	Page / Inquiry Scan		1.28s @ normal mode				mA
I _{SNIFF BT}	ACL Sniff		1.28s				mA
I _{A2DP BT}	A2DP		BDR / EDR @ 330 Kbps (3M baud rate)				mA
I _{TX BLE}	Peak BLE	BLE	P _{TX BLE} = +4 dBm				mA
I _{RX BLE}							mA
I _{PDn}	Power Down	WLAN and BT	Grounding of PDn pin				μA
I _{DeepSleep}	Deep Sleep		Low-power state used in sleep state				μA

21.5. INTERNAL OPERATING FREQUENCIES

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f _{SYSCCLK}	CPU clock speed	Refers to clock speed of WLAN SoC's CPU			256	MHz
	System / Encryption clock speed	Refers to clock speed of WLAN SoC's System and Encryption Unit			171	MHz
f _{REFCLK}	Crystal fundamental frequency	Frequency tolerance < ±10 ppm over operating temperature and process		38.4		MHz
f _{SLEEPCLK}	Sleep Clock frequency ¹¹	CMOS input clock signal type, ±250 ppm over temperature, aging and process		32.768		kHz

¹¹ Need to use module internal sleep clock crystal unit (optional) when low power operation mode near zero deep sleep is necessary. The internal sleep clock is not necessary for normal power modes.

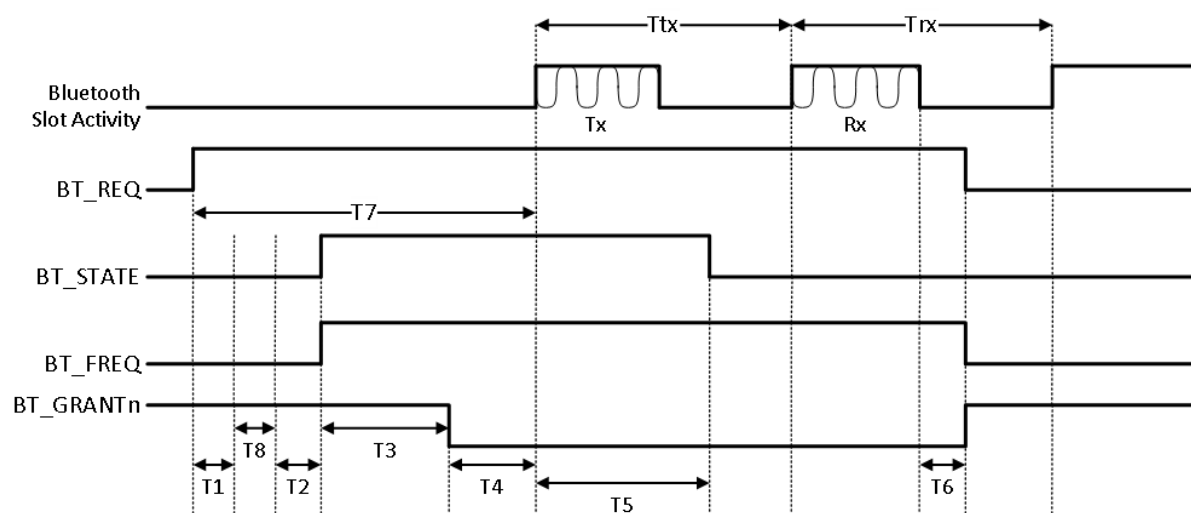
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21.6. COEXISTENCE INTERFACE SPECIFICATION

The Coexistence Interface pins are powered from the VIO voltage supply internally connected to $V_{DD} = 3.3V$. See Chapter 21.3 Digital Pin Characteristics for DC specification.

21.6.1. Marvell® 3/4-Wire Timing Data

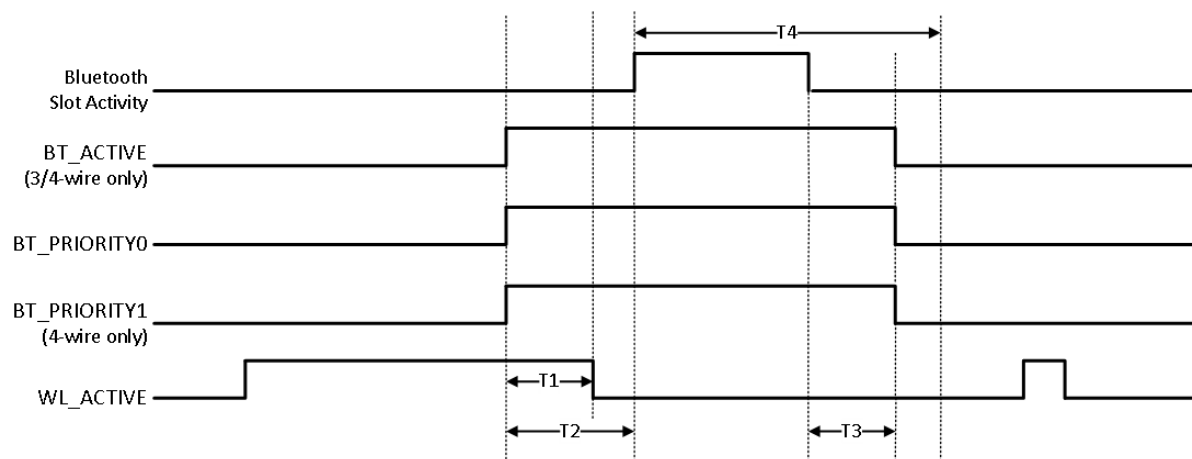
Symbol	Parameter	Min.	Typ.	Max.	Units
T1	Priority[0] info is valid in BT_STATE on and after T1 from BT_REQ rise.	0	1	100	µs
T2	TxRx Info is valid in BT_STATE on and after T2. The BT_STATE must hold until there is any change of direction in the next slots.	2	19	100	µs
T3	Time from TxRx Info valid to BCA grant decision ($T3 = T7 - T4 - T2 - T8 - T1$).	2	40	594	µs
T4	BT_GRANTn needs to be valid T4 time before the upcoming slot. BT_GRANTn indicates Tx grant, and may also indicate Rx grant. Once a slot is granted, the subsequent slots are also granted unless there is a change in direction from Rx to Tx. Rx to Tx change always re-arbitrates.	2	80	594	µs
T5	TxRx Info for the next slot is valid on and after T5 to the start of the next slot. If direction remains the same for the next slot, then BT_STATE must not change during the current slot. If the direction changes for the next slot, the BT_STATE must change only after the last bit of Bluetooth data is transferred; otherwise the transfer may be disrupted.	5	40	600	µs
T6	The BT_REQ signal de-asserts T6 time after last bit of Bluetooth data is transferred.	0	15	25	µs
T7	Time from BT_REQ rise to first Bluetooth slot boundary. Bluetooth slot boundary is marked by first bit of Bluetooth data.	8	150	600	µs
T8	Optional Priority[1] information is valid in BT_STAT on and after T8. This time parameter only exists if BCA is configured for 2-bit priority on same BT_STATE pin. Otherwise, the start of T2 would come after T1.	2	10	100	µs
Ttx	Slot time (fixed fpr Bluetooth)		625		µs
Trx	Slot time (fixed fpr Bluetooth)		625		µs



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21.6.2. WL_ACTIVE 2/3/4-Wire Timing Data

Symbol	Parameter	Min.	Typ.	Max.	Units
T1	- If WLAN can be stopped, WL_ACTIVE will de-assert prior to Bluetooth slot start ($T1 < T2$) - If the Bluetooth device samples WL_ACTIVE before starting priority transfer, WL_ACTIVE needs to de-assert earlier than the sampling time.	0		499	μs
T2	Time from BT_PRIORITY rise to start of Bluetooth activity.	20	50	499	μs
T3	Time from end of Bluetooth activity to BT_PRIORITY fall.	0	0	499	μs
T4	Slot time (fixed for Bluetooth)		625		μs



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21.7. HOST INTERFACE SPECIFICATION

21.7.1. USB 2.0 Host Interface

The USB 2.0 Host Interface pins are powered from the 3.3V_USB voltage supply with 3.3V. It supports the high / full speed operation (480 / 12 Mbps) depending on the USB bus termination. The default mode is high speed operation.

21.7.1.1. Common Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Input Levels for Low / Full Speed						
V _{IH}	Input high voltage (driven)		2.0			V
V _{IHZ}	Input high voltage (floating)		2.7		3.6	V
V _{IL}	Input low voltage				0.8	V
V _{DI}	Differential input sensitivity		0.2			V
V _{CM}	Differential common mode range		0.8		2.5	V
Input Levels for High Speed						
V _{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)		100		150	mV
V _{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)		525		625	mV
---	High-speed differential input signaling levels	Specified by eye pattern templates; see Section 7.1.7.2 in the USB 2.0 specification				
V _{HSCM}	High-speed data signaling common mode voltage range		-50		500	mV
Output Levels for Low / Full Speed						
V _{OL}	Output low voltage		0.0		0.3	V
V _{OH}	Output high voltage (driven)		2.8		3.6	V
V _{OSE1}	Output SE1 voltage		0.8			V
V _{CRS}	Output signal crossover voltage		1.3		2.0	V
Output Levels for High Speed						
V _{HSOI}	High-speed idle level		-10		10	mV
V _{HSOH}	High-speed data signaling high		360		440	mV
V _{HSOL}	High-speed data signaling low		-10		10	mV
V _{CHIRPJ}	Chirp J level (differential voltage)		700		1100	mV
V _{CHIRPK}	Chirp K level (differential voltage)		-900		-500	mV

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17.8.1.1 Common Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Decoupling Capacitance						
C _{RPB}	Upstream facing port bypass capacitance		1		10	μF
Input Capacitance for Low / Full Speed						
C _{INUB}	Upstream facing port capacitance (without cable)				100	pF
C _{EDGE}	Transceiver edge rate control capacitance				75	pF
Input Impedance for High Speed						
---	TDR specification for high-speed termination	Differential impedance	80		100	Ω
Terminations						
R _{PUI}	Bus pull-up resistor on upstream port (idles bus)		0.900		1.575	kΩ
R _{PUA}	Bus pull-up resistor on upstream port (receiving)		1.425		3.090	kΩ
Z _{INP}	Input impedance exclusive of pull-up / pull-down (for low / full speed)		300			kΩ
V _{TERM}	Termination voltage for upstream facing port pull-up resistor (R _{PU})		3.0		3.6	V
Terminations in High Speed						
V _{HSTERM}	Termination voltage in high speed		-10		10	mV

21.7.1.2. High Speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Driver Characteristics						
T _{HSR}	Rise Time (10% - 90%)		500			ps
T _{HSF}	Fall Time (10% - 90%)		500			ps
---	Driver waveform requirements	Specified by eye pattern templates; see Section 7.1.2 in the USB 2.0 specification				
Z _{HSDRV}	Driver output resistance (which also serves as high speed termination)		40.5		49.5	Ω
Clock Timings						
T _{HSDRAT}	High speed data rate		479.76		480.24	Mbps
T _{HSFRAM}	Microframe interval		124.9375		125.0625	μs
T _{HSRFI}	Consecutive microframe interval difference				4 high-speed bit times	
High Speed Data Timings						
---	Data source jitter	Specified by eye pattern templates; see Section 7.1.2.2 in the USB 2.0 specification				
---	Receiver jitter tolerance	Specified by eye pattern templates; see Section 7.1.2.2 in the USB 2.0 specification				

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21.7.1.3. Full Speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Driver Characteristics						
T _{FR}	Rise Time		4		20	ns
T _{FF}	Fall Time		4		20	ns
T _{FRFM}	Differential rise and fall time matching	T _{FR} / T _{FF}	90		111.11	%
Clock Timings						
T _{FDRATHS}	Full speed data rate	Average bit rate	11.994		12.006	Mbps
T _{FDRATE}	Frame interval		0.9995		1.0005	μs
T _{HSRFI}	Consecutive frame interval difference	No clock adjustment			42	ms
Full Speed Data Timings						
T _{DJ1}	Source Jitter total to next transition (including frequency tolerance)		-3.5		3.5	ns
T _{DJ2}	Source Jitter total to paired transitions (including frequency tolerance)		-4		4	ns
T _{FDEOP}	Source Jitter for differential transition to SE0 transition		-2		5	ns
T _{JR1}	Receiver Jitter to next transition		-18.5		18.5	ns
T _{JR2}	Receiver Jitter to paired transition		-9		9	ns
T _{FEOPT}	Source SE0 interval of EOP		160		175	ns
T _{FEOPR}	Receiver SE0 interval of EOP		82			ns
T _{FST}	Width of SE0 interval during differential transition				14	ns

21.7.1.4. Device Event Timings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T _{SIGATT}	Time from internal power good device pulling D+/D- beyond V _{IHZ} (min) (signaling attach)				100	ms
T _{ATTDB}	Debounce interval provided by USB system software after attach				100	ms
T _{2SUSP}	Maximum time a device can draw power > suspend power when bus is continuously in idle state				10	ms
T _{SUSAVGI}	Maximum duration of suspend averaging interval				1	s
T _{WTRSM}	Period of idle bus before device can initiate resum	Device must be remote-wake-up enabled	5			ms
T _{DRSMUP}	Duration of driving resume upstream		1		15	ms
T _{RSMCY}	Resume recovery time	Provided by USB system software	10			ms
T _{RSTRCYI}	Reset recovery time				10	ms
T _{IPD}	Inter-packet delay (for low/full speed)		2			bit times
T _{RSPIPD1}	Inter-packet delay for device response with detachable cable for low/full speed				6.5	bit times
T _{RSPIPD2}	Inter-packet delay for device response with captive cable for low/full speed				7.5	bit times
T _{DSETADDR}	SetAddress() completion time				50	ms

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17.8.1.4 Device Event Timings (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T _{DRQCMPLTND}	Time to complete standard request with no data				50	ms
T _{DRETDATA1}	Time to deliver first and subsequent (except last) data for standard request				500	ms
T _{DRETDATAN}	Time to deliver last data for standard request				50	ms
T _{HSRSPID2}	Inter-packet delay for device response with captive cable (high speed)				192 bit times + 52ns	ms
Reset Handshake Protocol						
F _{FILTSE0}	Time for which a suspended high speed capable device must see a continuous SE0 before beginning the high speed detection handshake		2.5			µs
T _{WTRSTFS}	Time for which high speed capable device operating in non-suspended full speed must wait after start of SE0 before beginning the high speed detection handshake		2.5		3000	µs
T _{WTREV}	Time for which high speed capable device operating in high speed must wait after start of SE0 before reverting to full speed		3.0		3.125	ms
T _{WTRSTHS}	Time for which a device must wait after reverting to full speed before sampling the bus state for SE0 and beginning the high speed detection handshake		100		875	µs
T _{UCH}	Minimum duration of a Chirp K from a high speed capable device within the reset protocol		1.0			ms
T _{UCHEND}	Time after start of SE0 by which a high speed capable device is required to have completed its Chirp K within the reset protocol				7.01	ms
T _{WTHS}	Time after end of upstream chirp at which device enters the high speed default state if downstream chirp is detected				500	µs
T _{WTFS}	Time after end of upstream chirp at which device reverts to full speed default state if no downstream chirp is detected		1.0		2.5	ms

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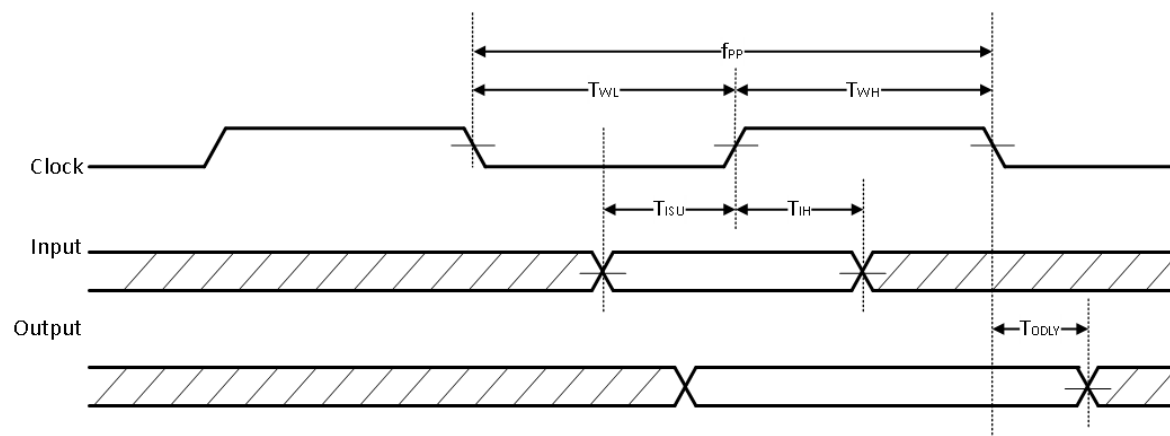
21.7.2. SDIO Host Interface

The SDIO Host Interface pins are powered from the SD_VIO voltage supply with either 3.3V or 1.8V. See Chapter 21.3 Digital Pin Characteristics for DC specification. The SDIO electrical specifications are identical for the 1-bit SDIO and 4-bit SDIO modes.

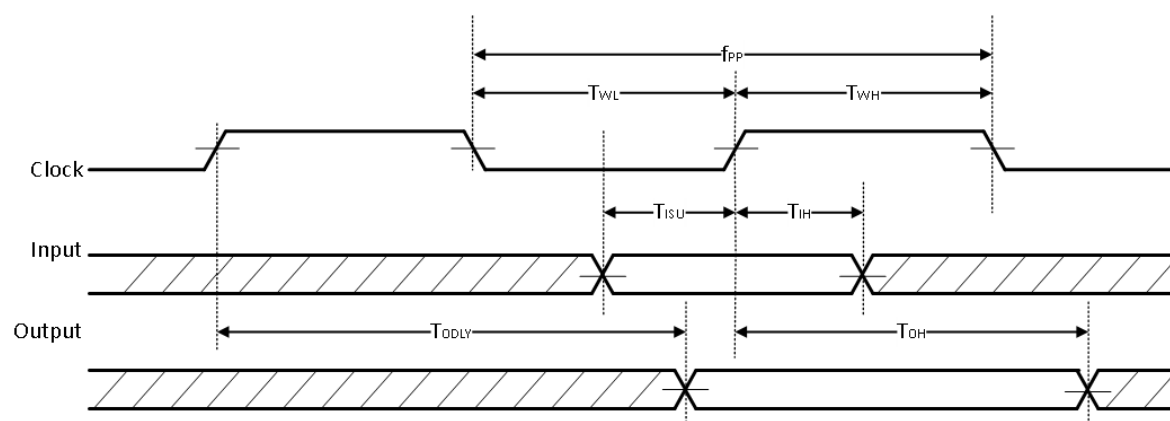
21.7.2.1. SDIO Timing Data – Default and High Speed Modes (3.3V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{PP}	Clock frequency	Normal	0		25	MHz
		High Speed	0		50	MHz
T_{WL}	Clock low time	Normal	10			ns
		High Speed	7			ns
T_{WH}	Clock high time	Normal	10			ns
		High Speed	7			ns
T_{ISU}	Input setup time	Normal	5			ns
		High Speed	6			ns
T_{IH}	Input hold time	Normal	5			ns
		High Speed	2			ns
T_{ODLY}	Output delay time, $CL \leq 40$ pF (1 card)				7.33	ns
T_{OH}	Output hold time	High Speed	2.5			ns

21.7.2.2. SDIO Protocol Timing – Default Speed Mode (3.3V)



21.7.2.3. SDIO Protocol Timing – High Speed Mode (3.3V)

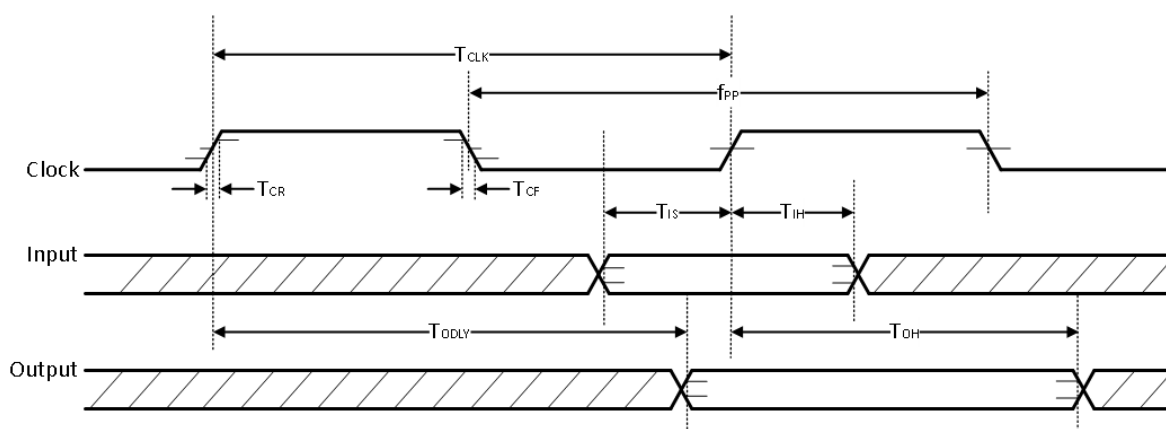


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21.7.2.4. SDIO Timing Data – SDR12, SDR25, SDR50 Modes (1.8V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{PP}	Clock frequency	SDR12 / SDR25 / SDR50	25		100	MHz
T_{IS}	Input setup time	SDR12 / SDR25 / SDR50	3			ns
T_{IH}	Input hold time	SDR12 / SDR25 / SDR50	0.8			ns
T_{CLK}	Clock time	SDR12 / SDR25 / SDR50	10		40	ns
T_{CR}, T_{CF}	Rise time, fall time $T_{CR}, T_{CF} < 2 \text{ ns (max) at 100 MHz}$ $C_{CARD} = 10 \text{ pF}$	SDR12 / SDR25 / SDR50			$0.2 T_{CLK}$	ns
T_{ODLY}	Output delay time, $CL \leq 30 \text{ pF}$	SDR12 / SDR25 / SDR50			7.5	ns
T_{OH}	Output hold time, $CL \leq 15 \text{ pF}$	SDR12 / SDR25 / SDR50	1.5			ns

21.7.2.5. SDIO Protocol Timing – SDR12, SDR25, SDR50 Modes (1.8V)



21.7.3. High-Speed UART Interface

The UART Tx / Rx pins are powered from the VIO voltage supply internally connected to $V_{DD} = 3.3V$. See Chapter 21.3 Digital Pin Characteristics for DC specification.

21.7.3.1. UART Baud Rates Supported

Baud Rate				
1200	19200	115200	1000000	2100000
2400	38400	230400	1382400	2764800
4800	57600	460800	1500000	3000000
9600	76800	500000	1834200	3250000
		921600	2000000	3692300
				4000000

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21.8. PERIPHERAL INTERFACE SPECIFICATION

21.8.1. GPIO

The GPIO pins are powered from the VIO voltage supply internally connected to $V_{DD} = 3.3V$. See Chapter 21.3 Digital Pin Characteristics for DC specification.

GPIO Function	GPIO Pin				
General Purpose	GPIO[1] Port 1	GPIO[4] Port 4	GPIO[16] Port 16	GPIO[17] Port 17	GPIO[18] Port 18
Pin	LED0	GPIO4	HOST_WAKEUP	LED1	CHIP_WAKEUP
Input	YES	YES	YES	YES	YES
Output	YES	YES	YES	YES	YES
Function by firmware	LED Mode WLAN		Chip-to-Host wake-up	LED Mode Bluetooth	Host-to-Chip wake-up
LED Output	YES	NO	NO	YES	NO

The basic function of the GPIOs are set by firmware default, but can be reconfigured by software.

21.8.1. LED Mode of LED0 and LED1

The GPIO pin for LED Mode is powered from the VIO voltage supply internally connected to $V_{DD} = 3.3V$. See Chapter 21.3 Digital Pin Characteristics for DC specification.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OH}	Switching current high	Tristate on pin (requires pull-up on board)	Tristate when driving high			mA
I_{OL}	Switching current low	@ 0.4V		10	31	mA

The LED Mode is independently selectable for the pin LED0 (Port1) and LED1 (Port17).

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22. RF ELECTRICAL CHARACTERISTICS

22.1. WLAN RADIO SPECIFICATION

Parameter	Operation mode				Specification
Standard Conformance	IEEE 802.11 / IEEE 802.11b				
	IEEE 802.11g				
	IEEE 802.11n				
Modulation	IEEE 802.11b				DSSS / CCK
	IEEE 802.11g				OFDM
	IEEE 802.11n				OFDM @ MCS0~15 and MCS32 (duplicate 6 Mbps)
Physical layer data rates	IEEE 802.11				1, 2 Mbps @ DSSS
	IEEE 802.11b				5.5, 11 Mbps @ DSSS / CCK
Supported data rates	IEEE 802.11g				6, 9, 12, 18, 24, 36, 48, 54 Mbps
	IEEE 802.11n	MCS0~7	HT20	LGI	6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps
				SGI	7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2 Mbps
			HT40	LGI	13.5, 27, 40.5, 54, 81, 108, 121.5, 135 Mbps
				SGI	15, 30, 45, 60, 90, 120, 135, 150 Mbps
		MCS8~15	HT20	LGI	13, 26, 39, 52, 78, 104, 117, 130 Mbps
				SGI	14.4, 28.9, 43.3, 57.8, 86.7, 115.6, 130, 144.4 Mbps
			HT40	LGI	27, 54, 81, 108, 162, 216, 243, 270 Mbps
				SGI	30, 60, 90, 120, 180, 240, 270, 300 Mbps
	MCS32				Duplicate 6 Mbps
Supported bandwidth	IEEE 802.11n				20, 40 MHz (BW)
Supported channel mode operation	IEEE 802.11n				20 MHz BW / channel, 40 MHz BW / channel, upper / lower 20 MHz BW @ 40 MHz channel, 20 MHz duplicate legacy BW @ 40 MHz channel
Supported Guard Interval	IEEE 802.11n				400 ns (SGI), 800 ns (LGI)
Supported Spatial Streams	IEEE 802.11n				2x2 MIMO
Supported channel 2.4GHz	IEEE 802.11g				1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13
	IEEE 802.11n	20 MHz Channel			1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13
		40 MHz Channel			1-5, 2-6, 3-7, 4-8, 5-9, 6-10, 7-11

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22.2. WLAN RF CHARACTERISTICS

22.2.1. RF Characteristics for IEEE 802.11b

Assume $V_{DD} = 3.3V$, $T_{amb} = 25^{\circ}C$ if nothing else stated

50 Ohm terminal load connected to the RF connector

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range			2400		2500	MHz
Carrier frequency tolerance			-25		+25	ppm
Transmit output power			+16	+18	+20	dBm
Spectrum mask	$f_C \pm 11$ MHz				-30	dBr
	$f_C \pm 22$ MHz				-50	
Power-on / Power-down ramp					2	μs
RF Carrier suppression					-15	dB
Error Vector Magnitude (EVM)	Peak				35	%
Minimum Receive Sensitivity	1 Mbps (DSSS)	$FER \leq 8\%$		-98	-86	dBm
	2 Mbps (DSSS)	$FER \leq 8\%$		-95	-83	dBm
	5.5 Mbps (CCK)	$FER \leq 8\%$		-91	-79	dBm
	11 Mbps (CCK)	$FER \leq 8\%$		-88	-76	dBm
Maximum Input Level		$FER \leq 8\%$	-10			dBm
Adjacent Channel Rejection		$FER \leq 8\%$	35			dB

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22.2.2. RF Characteristics for IEEE 802.11g

Assume $V_{DD} = 3.3V$, $T_{amb} = 25^{\circ}C$ if nothing else stated

50 Ohm terminal load connected to the RF connector

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range			2400		2500	MHz
Carrier frequency tolerance			-20		+20	ppm
Transmit output power			+12	+14	+16	dBm
Spectrum mask	$f_c \pm 11$ MHz				-20	dBr
	$f_c \pm 20$ MHz				-28	dBr
	$f_c \pm 30$ MHz				-40	dBr
Transmitter center frequency leakage					-15	dB
Transmitter Spectral Flatness			-2		+2	dB
Constellation Error (EVM)	BPSK, CR 1/2 (6 Mbps)				-5	dB
	BPSK, CR 3/4 (9 Mbps)				-8	dB
	QPSK, CR 1/2 (12 Mbps)				-10	dB
	QPSK, CR 3/4 (18 Mbps)				-13	dB
	16-QAM, CR 1/2 (24 Mbps)				-16	dB
	16-QAM, CR 3/4 (36 Mbps)				-19	dB
	64-QAM, CR 2/3 (48 Mbps)				-22	dB
	64-QAM, CR 3/4 (54 Mbps)				-25	dB
Minimum Receive Sensitivity	BPSK, CR 1/2 (6 Mbps)	PER $\leq 10\%$		-93	-82	dBm
	BPSK, CR 3/4 (9 Mbps)	PER $\leq 10\%$		-92	-81	dBm
	QPSK, CR 1/2 (12 Mbps)	PER $\leq 10\%$		-90	-79	dBm
	QPSK, CR 3/4 (18 Mbps)	PER $\leq 10\%$		-88	-77	dBm
	16-QAM, CR 1/2 (24 Mbps)	PER $\leq 10\%$		-85	-74	dBm
	16-QAM, CR 3/4 (36 Mbps)	PER $\leq 10\%$		-81	-70	dBm
	64-QAM, CR 2/3 (48 Mbps)	PER $\leq 10\%$		-77	-66	dBm
	64-QAM, CR 3/4 (54 Mbps)	PER $\leq 10\%$		-76	-65	dBm
Maximum Input Level		PER $\leq 10\%$			-20	dBm
Adjacent channel rejection	BPSK, CR 1/2 (6 Mbps)	PER $\leq 10\%$	16			dB
	64-QAM, CR 3/4 (54 Mbps)	PER $\leq 10\%$	-1			dB

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22.2.3. RF Characteristics for IEEE 802.11n (BW 20 MHz)

Assume $V_{DD} = 3.3V$, $T_{amb} = 25^{\circ}C$ if nothing else stated

50 Ohm terminal load connected to the RF connector

Parameter	Condition	Min.	Typ.	Max.	Units
RF frequency range		2400		2500	MHz
Carrier frequency tolerance		-20		+20	ppm
Transmit output power		11	13	15	dBm
Spectrum mask	$f_C \pm 11$ MHz			-20	dBr
	$f_C \pm 20$ MHz			-28	dBr
	$f_C \pm 30$ MHz			-45	dBr
Transmitter center frequency leakage				-15	dB
Transmitter Spectral Flatness		-2		+2	dB
Constellation Error (EVM)	BPSK, CR 1/2			-5	dB
	QPSK, CR 1/2			-10	dB
	QPSK, CR 3/4			-13	dB
	16-QAM, CR 1/2			-16	dB
	16-QAM, CR 3/4			-19	dB
	64-QAM, CR 2/3			-22	dB
	64-QAM, CR 3/4			-25	dB
	64-QAM, CR 5/6			-28	dB
Minimum Receive Sensitivity ¹²	6.5 Mbps (MCS0)	PER ≤ 10%	-92	-82	dBm
	13 Mbps (MCS1)	PER ≤ 10%	-89	-79	dBm
	19.5 Mbps (MCS2)	PER ≤ 10%	-87	-77	dBm
	26 Mbps (MCS3)	PER ≤ 10%	-84	-74	dBm
	39 Mbps (MCS4)	PER ≤ 10%	-80	-70	dBm
	52 Mbps (MCS5)	PER ≤ 10%	-76	-66	dBm
	58.5 Mbps (MCS6)	PER ≤ 10%	-75	-65	dBm
	65 Mbps (MCS7)	PER ≤ 10%	-74	-64	dBm
Maximum Input Level		PER ≤ 10%		-20	dBm
Adjacent channel rejection ¹³	65 Mbps (MCS7)	PER ≤ 10%	-2		dB

¹² The Minimum Sensitivity levels apply only to non-STBC modes, MCS 0~15, 800 ns LGI and BCC.

¹³ The Adjacent Channel Rejection levels apply only to non-STBC modes, MCS 0~15, 800 ns LGI and BCC.

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22.2.4. RF Characteristics for IEEE 802.11n (BW 40 MHz)

Assume $V_{DD} = 3.3V$, $T_{amb} = 25^{\circ}C$ if nothing else stated

50 Ohm terminal load connected to the RF connector

Parameter	Condition	Min.	Typ.	Max.	Units
RF frequency range		2400		2500	MHz
Carrier frequency tolerance		-20		+20	ppm
Transmit output power		11	13	15	dBm
Spectrum mask	$f_C \pm 21$ MHz			-20	dBr
	$f_C \pm 40$ MHz			-28	dBr
	$f_C \pm 60$ MHz			-45	dBr
Transmitter center frequency leakage				-15	dB
Transmitter Spectral Flatness		-2		+2	dB
Constellation Error (EVM)	BPSK, CR 1/2			-5	dB
	QPSK, CR 1/2			-10	dB
	QPSK, CR 3/4			-13	dB
	16-QAM, CR 1/2			-16	dB
	16-QAM, CR 3/4			-19	dB
	64-QAM, CR 2/3			-22	dB
	64-QAM, CR 3/4			-25	dB
	64-QAM, CR 5/6			-28	dB
Minimum Receive Sensitivity ¹²	13.5 Mbps (MCS0)	PER $\leq$ 10%	-89	-79	dBm
	27 Mbps (MCS1)	PER $\leq$ 10%	-86	-76	dBm
	40.5 Mbps (MCS2)	PER $\leq$ 10%	-84	-74	dBm
	54 Mbps (MCS3)	PER $\leq$ 10%	-81	-71	dBm
	81 Mbps (MCS4)	PER $\leq$ 10%	-77	-67	dBm
	108 Mbps (MCS5)	PER $\leq$ 10%	-73	-63	dBm
	121.5 Mbps (MCS6)	PER $\leq$ 10%	-72	-62	dBm
	135 Mbps (MCS7)	PER $\leq$ 10%	-71	-61	dBm
Maximum Input Level		PER $\leq$ 10%		-20	dBm
Adjacent channel rejection ¹³	135 Mbps (MCS7)	PER $\leq$ 10%	-2		dB

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22.3. BLUETOOTH RF CHARACTERISTICS

Assume $V_{DD} = 3.3V$, $T_{amb} = 25^{\circ}C$ if nothing else stated
50 Ohm terminal load connected to the RF connector

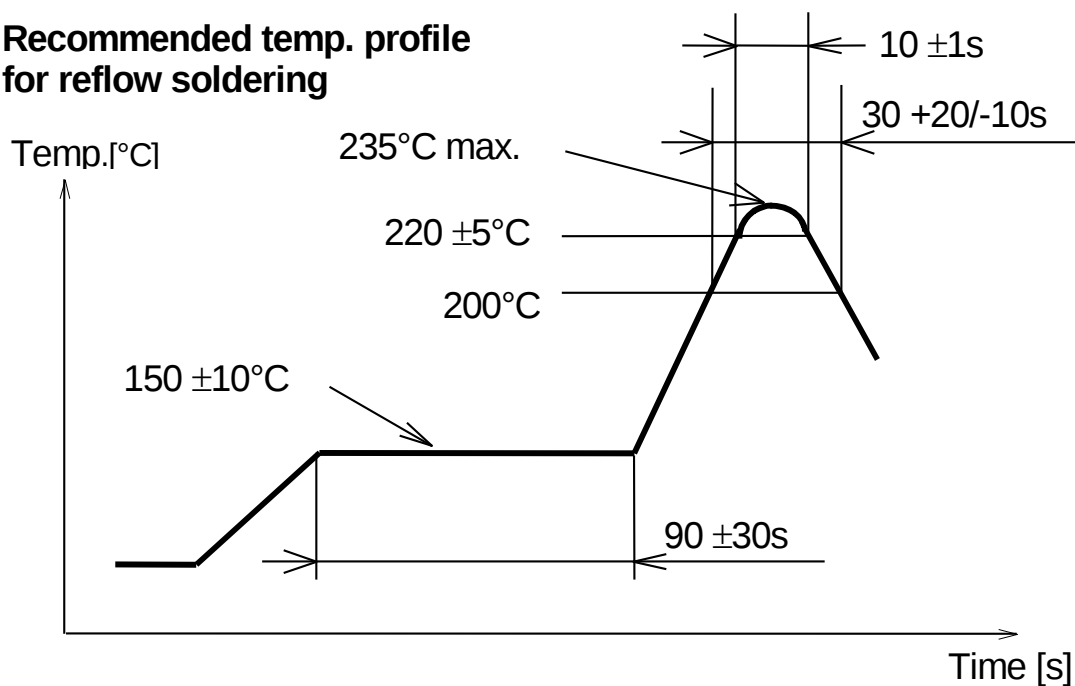
Parameter	Condition	Min.	Typ.	Max.	Units
RF frequency range		2400		2500	MHz
Channel Spacing	BDR, EDR		1 / 2		MHz
RSSI range	Resolution = 1 dB	-90		0	dBm
Output Power Class	BDR, EDR	Class 1.5			
Output Power	BDR		8		dBm
Minimum Receive Sensitivity	BDR			-70	dBm
Spurious Emission	Conducted measurement with a 50-Ω dual-ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66				dBm

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23. SOLDERING TEMPERATURE-TIME PROFILE (FOR REFLOW SOLDERING)

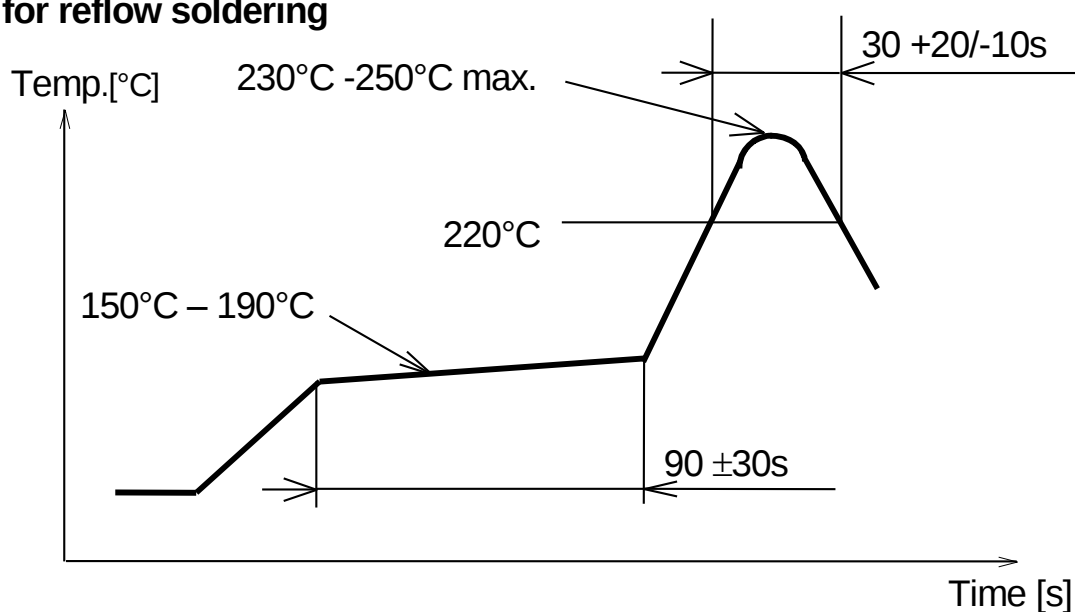
23.1. FOR LEAD SOLDER

Recommended temp. profile for reflow soldering



23.2. FOR LEADFREE SOLDER

Our used temp. profile for reflow soldering

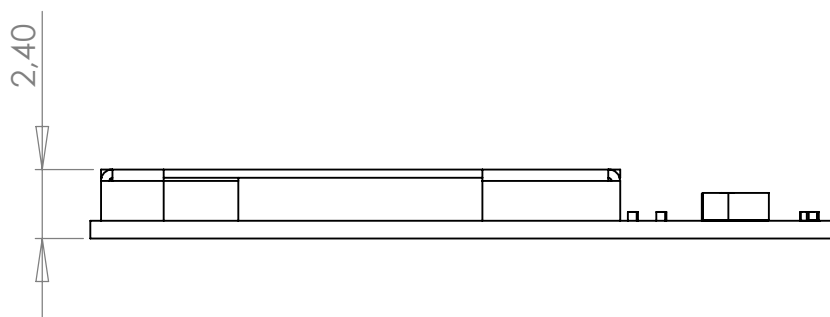
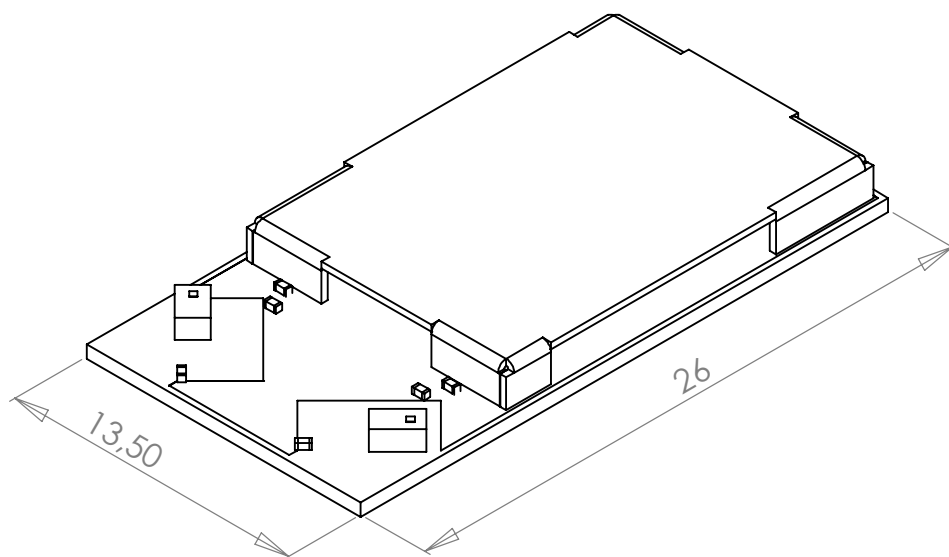


Reflow permissible cycle: 2
Opposite side reflow is prohibited due to module weight.

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24. PAN9055 / PAN9045 MODULE DIMENSION

No.	Item	Dimension	Tolerance	Remark
1	Width	13.50	± 0.20	
2	Length	26.00	± 0.20	
3	Height	2.40	± 0.20	With case



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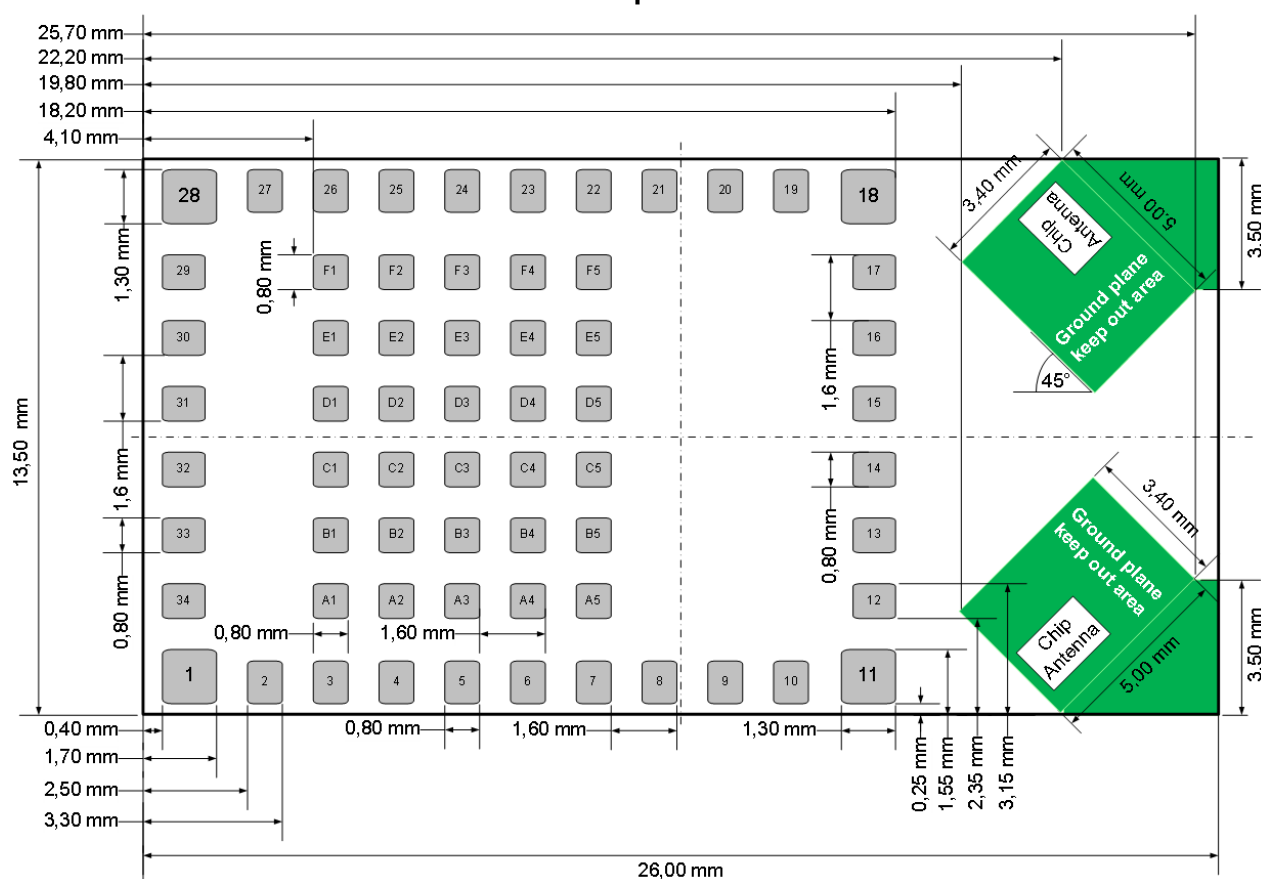
25. PAN9055 / PAN9045 FOOTPRINT OF THE MODULE

All dimensions are in millimeters.

The outer dimensions have a tolerance of $\pm 0.2\text{mm}$.

Top view, Application PCB

Top View



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26. CASE MARKING

TBP

No.	Remark
1	Marking for Pin 1 (Circle 0,15 mm)
2	2D-Code, for internal usage only and can be change without any notice
3	Marking definition see below

26.1. EXAMPLE FOR MARKING

P	A	N	9	0	5	5			H	W	/	S	W		E	S
E	N	W	F	9	1	0	1	x	1	y	F					
Y	Y	W	W	D	L	L										
S	N	S	N	S	N	S	N									
M	A	C	M	A	C	M	A	C	M	A	C					
M	A	C	M	A	C	M	A	C	M	A	C					

26.2. MARKING DEFINITION

(1) Pin1 marking

(2) 2D code (Serial number)

(3) Marking:

- PAN9055 (Model Name), HW/SW (Hardware/Software version)
- ES (Engineering Sample marking)
- ENWF9101x1yF (Part Number, refer to chapter 32. Ordering Information)
- Lot code (YearYear, WeekWeek, Day, LotLot)
- Serial Number (8 digits)
- WLAN MAC address (12 digits)
- Bluetooth MAC address (12 digits)

Note: For available Versions, refer to [1] PAN9055 and PAN9045 Design-Guide.
and chapter 32. Ordering Information.

27. MECHANICAL REQUIREMENTS

No.	Item	Limit	Condition
1	Solderability	More than 75% of the soldering area shall be coated by solder	Reflow soldering with recommendable temperature profile
2	Resistance to soldering heat	It shall be satisfied electrical requirements and not be mechanical damage	See chapter 23.2

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28. DEVELOPMENT OF APPLICATIONS

For development support please refer to [1] PAN9055 and PAN9045 Design-Guide.

29. RELIABILITY TESTS

The measurement should be done after being exposed to room temperature and humidity for 1 hour.

No.	Item	Limit	Condition
1	Vibration test	Electrical parameter should be in specification	a) Freq.:10~50Hz,Amplitude:1.5mm a) 20min. / cycle,1hrs. each of XYZ axis b) Freq.:30~100Hz, 6G b) 20min. / cycle,1hrs. each of XYZ axis
2	Shock test	the same as above	Dropped onto hard wood from height of 50cm for 3 times
3	Heat cycle test	the same as above	-40°C for 30min. and +85°C for 30min.; each temperature 300 cycles
4	Moisture test	the same as above	+60°C, 90% RH, 300h
5	Low temp. test	the same as above	-40°C, 300h
6	High temp. test	the same as above	+85°C, 300h

30. CAUTIONS

Failure to follow the guidelines set forth in this document may result in degrading of the product's functions and damage to the product.

30.1. DESIGN NOTES

- (1) Follow the conditions written in this specification, especially the control signals of this module.
- (2) The supply voltage has to be free of AC ripple voltage (for example from a battery or a low noise regulator output). For noisy supply voltages, provide a decoupling circuit (for example a ferrite in series connection and a bypass capacitor to ground of at least 47uF directly at the module).
- (3) This product should not be mechanically stressed when installed.
- (4) Keep this product away from heat. Heat is the major cause of decreasing the life of these products.
- (5) Avoid assembly and use of the target equipment in conditions where the products' temperature may exceed the maximum tolerance.
- (6) The supply voltage should not be exceedingly high or reversed. It should not carry noise and/or spikes.
- (7) Keep this product away from other high frequency circuits.

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30.2. INSTALLATION NOTES

- (1) Reflow soldering is possible twice based on the conditions in chapter 15.
Set up the temperature at the soldering portion of this product according to this reflow profile.
- (2) Carefully position the products so that their heat will not burn into printed circuit boards or affect the other components that are susceptible to heat.
- (3) Carefully locate these products so that their temperatures will not increase due to the effects of heat generated by neighboring components.
- (4) If a vinyl-covered wire comes into contact with the products, then the cover will melt and generate toxic gas, damaging the insulation. Never allow contact between the cover and these products to occur.
- (5) This product should not be mechanically stressed or vibrated when reflowed.
- (6) To repair the board by hand soldering, follow the conditions set forth in this chapter.
- (7) Do not wash this product.
- (8) Refer to the recommended pattern when designing a board.
- (9) Pressing on parts of the metal cover or fastening objects to the metal will cause damage to the unit.
- (10) For more details on LGA (Land Grid Array) soldering processes refer to the application note.

30.3. USAGE CONDITIONS NOTES

- (1) Take measures to protect the unit against static electricity.
If pulses or other transient loads (a large load applied in a short time) are applied to the products, check and evaluate their operation before assembly on the final products.
- (2) Do not use dropped products.
- (3) Do not touch, damage or soil the pins.
- (4) Follow the recommended condition ratings about the power supply applied to this product.
- (5) Electrode peeling strength: Do not add pressure of more than 4.9N when soldered on PCB.
- (6) Pressing on parts of the metal cover or fastening objects to the metal cover will cause damage.
- (7) These products are intended for general purpose and standard use in general electronic equipment, such as home appliances, office equipment, information and communication equipment.

30.4. STORAGE NOTES

- (1) The module should not be stressed mechanically during storage.
- (2) Do not store these products in the following conditions or the performance characteristics of the product, such as RF performance will be adversely affected:
 - Storage in salty air or in an environment with a high concentration of corrosive gas, such as Cl₂, H₂S, NH₃, SO₂, or NO_x
 - Storage in direct sunlight
 - Storage in an environment where the temperature may be outside the range of 5°C to 35°C range, or where the humidity may be outside the 45 to 85% range.
 - Storage of the products for more than one year after the date of delivery Storage period: Please check the adhesive strength of the embossed tape and soldering after 6 months of storage.
- (3) Keep this product away from water, poisonous gas and corrosive gas.
- (4) This product should not be stressed or shocked when transported.
- (5) Follow the specification when stacking packed crates (max. 10).

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30.5. SAFETY CAUTIONS

These specifications are intended to preserve the quality assurance of products and individual components.

Before use, check and evaluate the operation when mounted on your products. Abide by these specifications, without deviation when using the products. These products may short-circuit. If electrical shocks, smoke, fire, and/or accidents involving human life are anticipated when a short circuit occurs, then provide the following failsafe functions, as a minimum.

- (1) Ensure the safety of the whole system by installing a protection circuit and a protection device.
- (2) Ensure the safety of the whole system by installing a redundant circuit or another system to prevent a single fault causing an unsafe status.

30.6. OTHER CAUTIONS

- (1) This specification sheet is copyrighted. Please do not disclose it to a third party.
- (2) Please do not use the products for other purposes than those listed.
- (3) Be sure to provide an appropriate fail-safe function on your product to prevent an additional damage that may be caused by the abnormal function or the failure of the product.
- (4) This product has been manufactured without any ozone chemical controlled under the Montreal Protocol.
- (5) These products are not intended for other uses, other than under the special conditions shown below. Before using these products under such special conditions, check their performance and reliability under the said special conditions carefully to determine whether or not they can be used in such a manner.
 - In liquid, such as water, salt water, oil, alkali, or organic solvent, or in places where liquid may splash.
 - In direct sunlight, outdoors, or in a dusty environment
 - In an environment where condensation occurs.
 - In an environment with a high concentration of harmful gas (e.g. salty air, HCl, Cl₂, SO₂, H₂S, NH₃, and NO_x)
- (6) If an abnormal voltage is applied due to a problem occurring in other components or circuits, replace these products with new products because they may not be able to provide normal performance even if their electronic characteristics and appearances appear satisfactory.
- (7) When you have any question or uncertainty, contact Panasonic.

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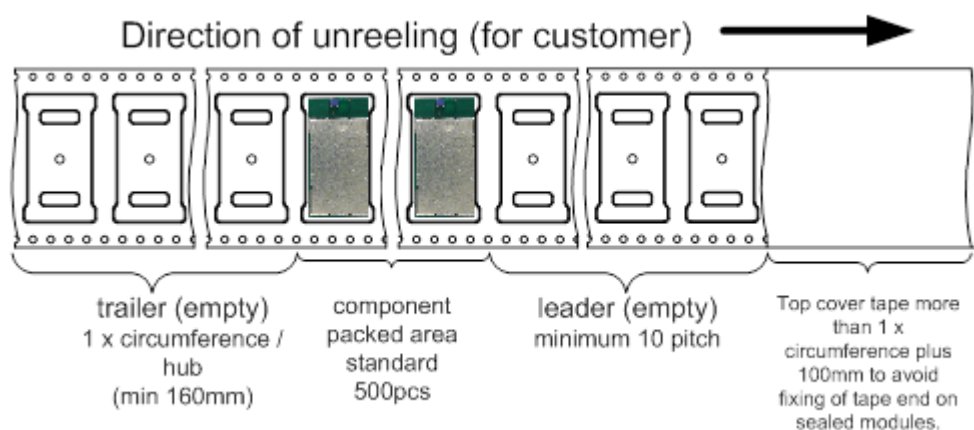
31. PACKAGING

If the product has mass production status, indicated in chapter 3, we will deliver the module in the package which are described below.

31.1. PAN9055 / PAN9045 TAPE DIMENSION

TBP

31.2. PACKING IN TAPE

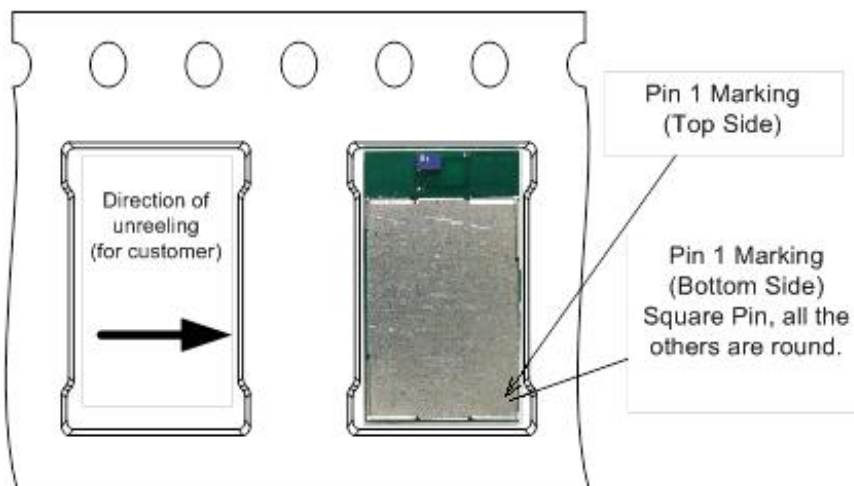


Empty spaces in component packed area shall be less than two per reel and those spaces shall not be consecutive.

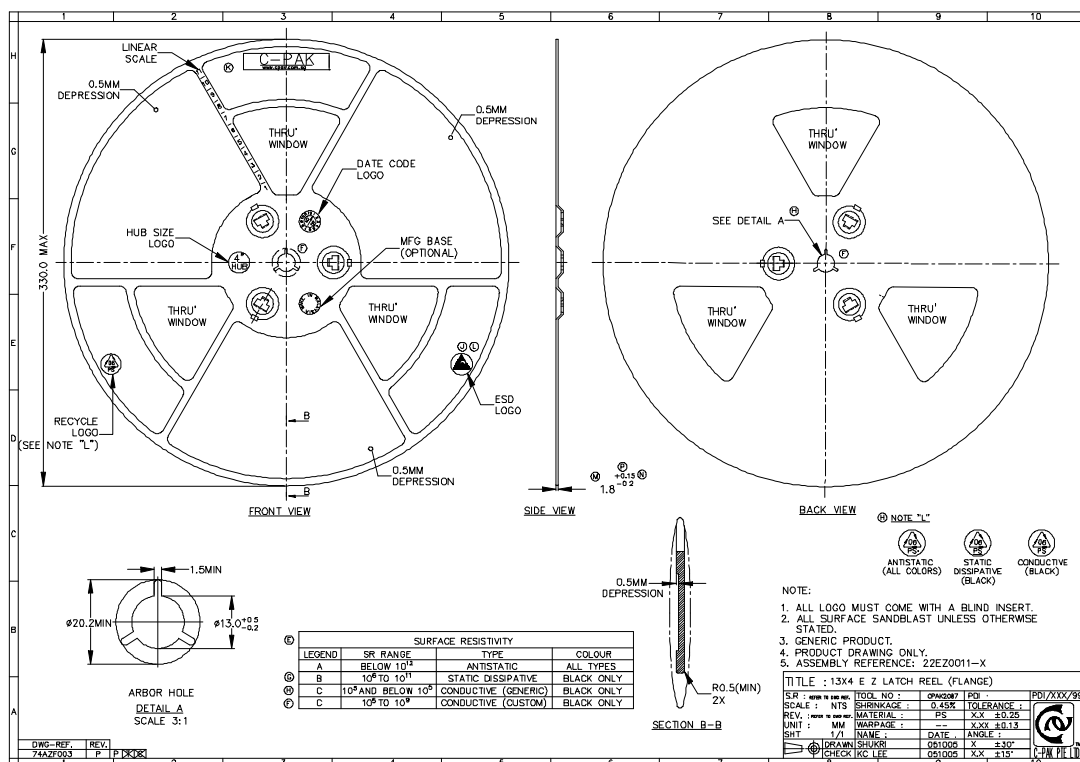
Top cover tape shall not be found on reel holes and shall not stick out from reel.

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31.3. COMPONENT DIRECTION



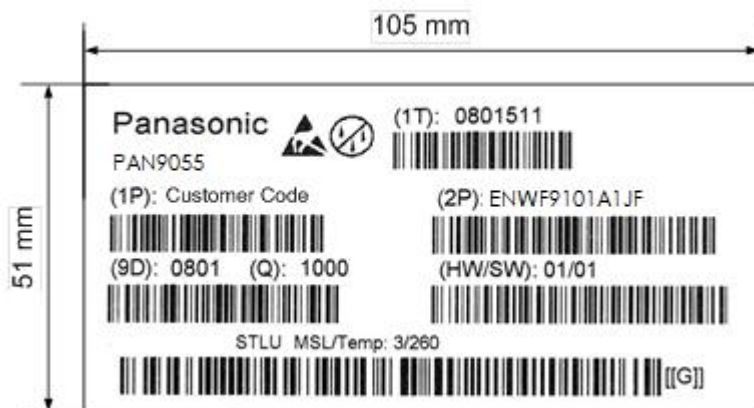
31.4. REEL DIMENSION



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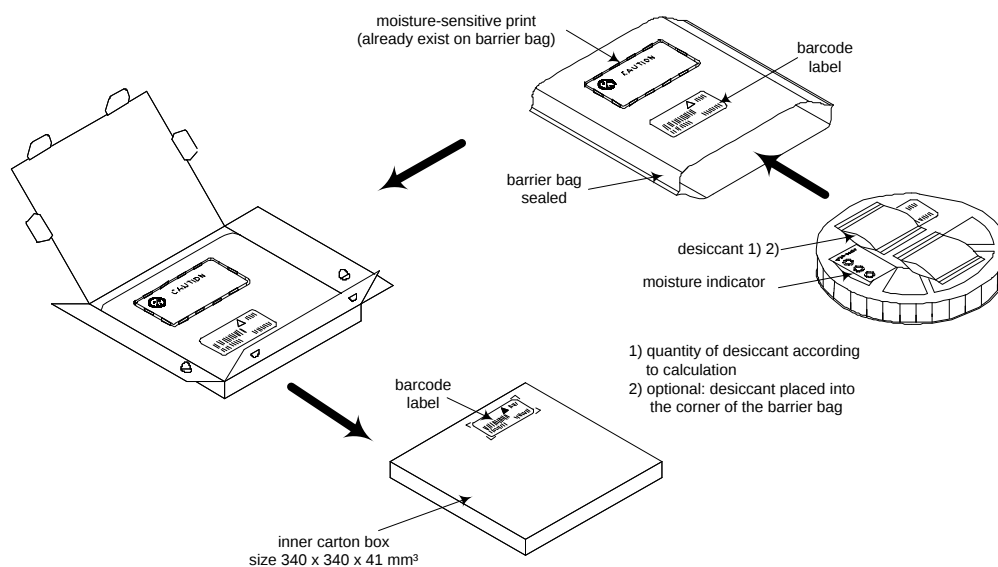
31.5. LABEL FOR PACKAGE

The picture shows an example from similar product.



(1T)	Lot code [YYWWDLL]	Example from above:
	YY year	printed 08
	WW normal calendar week	printed 01
	D day	printed 5 (Friday)
	L line identifier, if more as one	printed 1
	L lot identifier per day	printed 1
(1P)	Customer Order Code, if any, otherwise company name will be printed	
(2P)	Panasonic Order Code: ENWF9101x1yF	
(9D)	Date code as [YYWW]	
(Q)	Quantity [XXXX], variable max. 1500	
(HW/SW)	Hardware /Software Release	
	Hardware 01	Indicates the HW revision.
	Software 01	Indicates the SW revision.

31.6. TOTAL PACKAGE



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32. ORDERING INFORMATION

Ordering part number	Description	MOQ ⁽¹⁾
ENWF9101A1JF ⁽²⁾	PAN9055 WLAN IEEE 802.11 b/g/n 2.4GHz Radio Module with ceramic chip-antenna COMMERCIAL GRADE	ES
ENWF9101C1JF ⁽²⁾	PAN9045 WLAN IEEE 802.11 b/g/n 2.4GHz Radio Module with 50Ω bottom pad COMMERCIAL GRADE	ES
ENWF9101A1EF ⁽²⁾	PAN9055 WLAN IEEE 802.11 b/g/n 2.4GHz Radio Module with ceramic chip-antenna EXTENDED GRADE	ES
ENWF9101C1EF ⁽²⁾	PAN9045 WLAN IEEE 802.11 b/g/n 2.4GHz Radio Module with 50Ω bottom pad EXTENDED GRADE	ES

Notes:

- (1) Abbreviation for Minimum Order Quantity (MOQ). The standard MOQ for mass production is 1500 pieces, fewer only on customer demand. Samples for evaluation can be delivered at any quantity via the distribution channels.
- (2) Samples are available on customer demand

32.1. INFORMATION REGARDING SOFTWARE VERSIONS

ENWF9101A1JF / ENWF9101C1JF / ENWF9101A1EF / ENWF9101C1EF:

The modules will be delivered without any WLAN / BT Firmware but including calibration data.

The WLAN / BT SoC Firmware and HOST Driver-Firmware Interface software modules taking place on the customers HOST processor and need to be programmed on their own production process.

For details refer to the design guide.

33. ROHS DECLARATION

Declaration of environmental compatibility for supplied products:

Hereby we declare to our best present knowledge based on declaration of our suppliers that this product does not contain the following substances which are banned by Directive 2002/95/EC (RoHS) or contains a maximum concentration of 0.1% by weight in homogeneous materials for

- Lead and lead compounds
- Mercury and mercury compounds
- Chromium (VI)
- PBB (polybrominated biphenyl) category
- PBDE (polybrominated biphenyl ether) category

And a maximum concentration of 0.01% by weight in homogeneous materials for

- Cadmium and cadmium compounds

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34. REGULATORY INFORMATION

34.1. FCC FOR US

34.1.1. FCC Notice



The device PAN9055, including the ceramic antenna (ENWF9101A1JF and ENWF9101A1EF) and PAN9045 SMD type (ENWF9101C1JF and ENWF9101C1EF), including with the antennas, which are listed in 34.1.5, complies with Part 15 of the FCC Rules.

The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.transmitter Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

The FCC identifier is **FCC ID: T7V-9055** → [TBC](#).

34.1.2. Caution



The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Panasonic Industrial Devices Europe GmbH may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

34.1.3. Labeling Requirements



The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label (laser marking) on the outside of the OEM enclosure specifying the appropriate Panasonic FCC identifier for this product as well as the FCC Notice above. The FCC identifier is **FCC ID: T7V-9055** → [TBC](#).

This FCC identifier is valid for all PAN9055 modules, for details, see the Chapter 32. Ordering Information.

In any case the end product must be labelled exterior with
"Contains FCC ID: T7V-9055" → [TBC](#)

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34.1.4. Antenna Warning

The related part number for this device are ENWF9101C1JF and ENWF9101C1EF (PAN9045 with SMD pad). For details, see the Chapter 32. Ordering Information. These devices are tested with a standard SMA connector and with the antennas listed below. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions. The FCC identifier for this device with the antenna listed in item 1 is the same (FCC ID: T7V-9055 → TBC).

34.1.5. Approved Antenna List

Note: We are able to qualify your antenna and will add to this list as that process is completed.

Item	Part Number	Manufacturer	Frequency Band	Type	Gain (dBi)
1	ANT2012LL13R2400A	Taiyo Yuden	2.4GHz	Chip-Antenna	+2.72

34.1.6. RF Exposure PAN9055



To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure that the approved antenna in the previous table must be installed.

The preceding statement must be included as a CAUTION statement in manuals for products operating with the approved antennas in the previous table to alert users on FCC RF Exposure compliance.

Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of PAN9055 with mounted ceramic chip antenna (**FCC ID: T7V-9055 → TBC**) is far below the FCC radio frequency exposure limits. Nevertheless, the PAN9055 shall be used in such a manner that the potential for human contact during normal operation is minimized.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

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34.2. INDUSTRY CANADA CERTIFICATION

PAN9055 is licensed to meet the regulatory requirements of Industry Canada (IC),
license: IC: **216Q-9055** → [TBC](#)

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in Table 34.1.5 above, having a maximum gain of 2.72 dBi. Antennas not included in this list or having a gain greater than 2.72 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Due to the model size the IC identifier is displayed in the installation instruction only and can not be displayed on the modules label due to the limited size.

34.2.1. IC Notice



The device PAN9055, for details refer to Chapter 32, including the antennas, which are listed in 34.1.5, complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN.

Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

34.2.2. Labeling Requirements



The Original Equipment Manufacturer (OEM) must ensure that IC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Panasonic IC identifier for this product as well as the IC Notice above. The IC identifier is: 216Q-9055 → [TBC](#).

This IC identifier is valid for all PAN9055 modules, for details, see the Chapter 32. Ordering Information.

In any case the end product must be labelled exterior with
"Contains IC: 216Q-9055" → [TBC](#)

Les fabricants d'équipements (OEM) doivent s'assurer que les obligations d'étiquetage du produit final sont remplies. Ces obligations incluent une étiquette clairement visible à l'extérieur de l'emballage externe, comportant l'identifiant IC du module Panasonic inclus, ainsi que la notification ci-dessus.

Les identifiants IC sont: IC: 216Q-9055 → [TBC](#)

Ces identifiants sont valides pour tous les modules PAN9055 (Chapter 32. Ordering Information). Dans tous les cas les produits finaux doivent indiquer sur leur emballage externe une des mentions suivantes:

"Contient IC: 216Q-9055" → [TBC](#)

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34.3. EUROPEAN R&TTE DECLARATION OF CONFORMITY

All modules described in this data sheet comply to the standards according R&TTE article:

3.1a Safety/Health: EN60950-1:2006+A11:2009+A1:2010+A12:2011+AC:2011
EN62311:2008; EN 62479:2010

3.1b EMC: EN 301 489-17 V2.2.1:2012-09

3.2 Radio: EN 300 328 V1.8.1:2012-06

As a result of the conformity assessment procedure described in Annex III of the Directive 1999/5/EC, the end-customer equipment should be labelled as follows:



The end-customer has to assure that the device has a distance of more the 20cm from the human body under all circumstances.

The end-customer equipment must meet the actual Safety/Health requirements according R&TTE.

PAN9055 and their versions in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, Netherland, the United Kingdom, Switzerland, and Norway.

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35. GENERAL INFORMATION

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All rights reserved.

This product description does not lodge the claim to be complete and free of mistakes.

Please contact the related product manager in every case.

If we deliver ES samples to the customer, these samples have the status Engineering Samples. This means, the design of this product is not yet concluded. Engineering Samples may be partially or fully functional, and there may be differences to be published Data Sheet.

Engineering Samples are not qualified and are not to be used for reliability testing or series production.

Disclaimer:

Customer acknowledges that samples may deviate from the Data Sheet and may bear defects due to their status of development and the lack of qualification mentioned above.

Panasonic rejects any liability or product warranty for Engineering Samples. In particular, Panasonic disclaims liability for damages caused by

- the use of the Engineering Sample other than for Evaluation Purposes, particularly the installation or integration in another product to be sold by Customer,
- deviation or lapse in function of Engineering Sample,
- improper use of Engineering Samples.

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