FAIRCHILD SEMICONDUCTOR®

February 2009

SG6902
CCM PFC/Flyback PWM Combination Controller

Features

- Green-Mode PFC and PWM Operation
- No Switching of PFC at Light Loads Saves Power
- Low Startup and Operating Current
- Innovative Switching-Charge Multiplier-Divider
- Multi-Vector Control for Improved PFC Output Transient Response
- Interleaved PFC/PWM Switching
- Programmable Two-Level PFC Output Voltage
- Average-Current-Mode Control for PFC
- Cycle-by-Cycle Current Limiting for PFC/PWM
- PFC Over-Voltage and Under-Voltage Protections
- PFC and PWM Feedback Open-Loop Protection
- Brownout Protection
- Over-Temperature Protection

Applications

- Switching Power Supplies with Active PFC and Standby Power
- High-Power Adaptors

Description

The highly integrated SG6902 is designed for power supplies with boost PFC and flyback PWM. It requires few external components to achieve green mode operation and versatile protections. It is available in a 20-pin SOIC package.

The proprietary interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light loads, the switching frequency is continuously decreased to reduce power consumption. If output loading is further reduced, the PFC stage is turned off to reduce power consumption.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6902 shuts off PFC to prevent extra-high voltage on output. Programmable two-level output voltage control reduces the PFC output voltage at low line input to increase the efficiency of the power supply.

For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains a constant output power limit. Hiccup operation during output overloading is also guaranteed.

In addition, SG6902 provides protection functions, such as brownout and RI pin open/short protections.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
SG6902SZ	-30°C to +85°C	RoHS	20-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS013, .300 inch, Wide Bod	Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Circuit

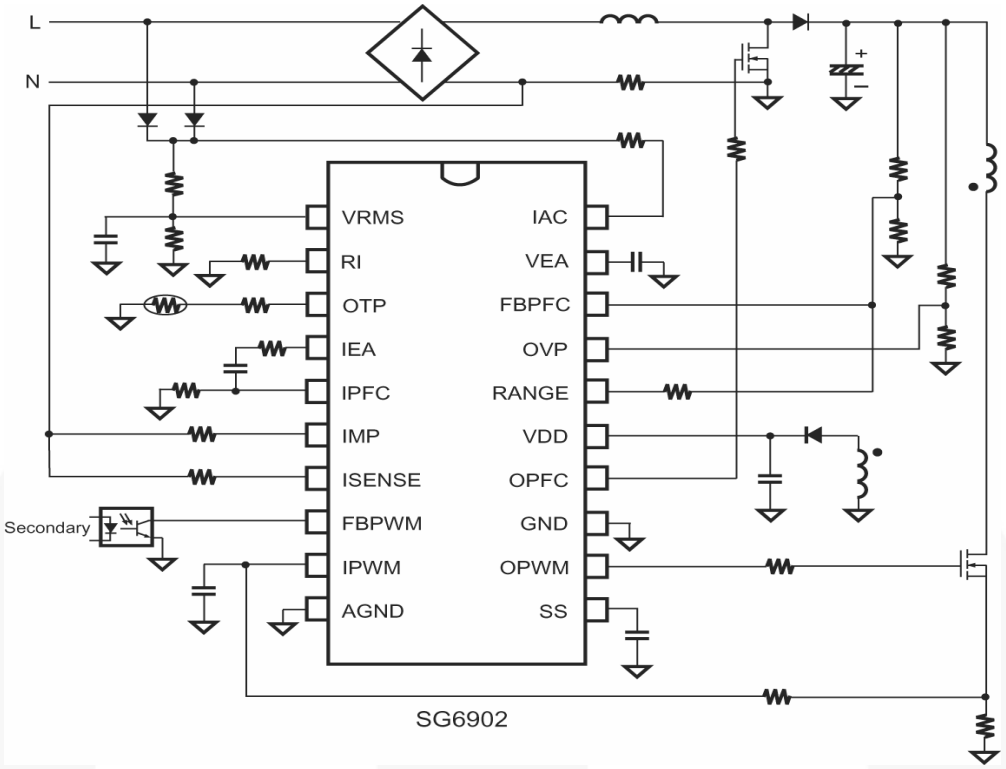

Figure 1. Typical Application

Block Diagram

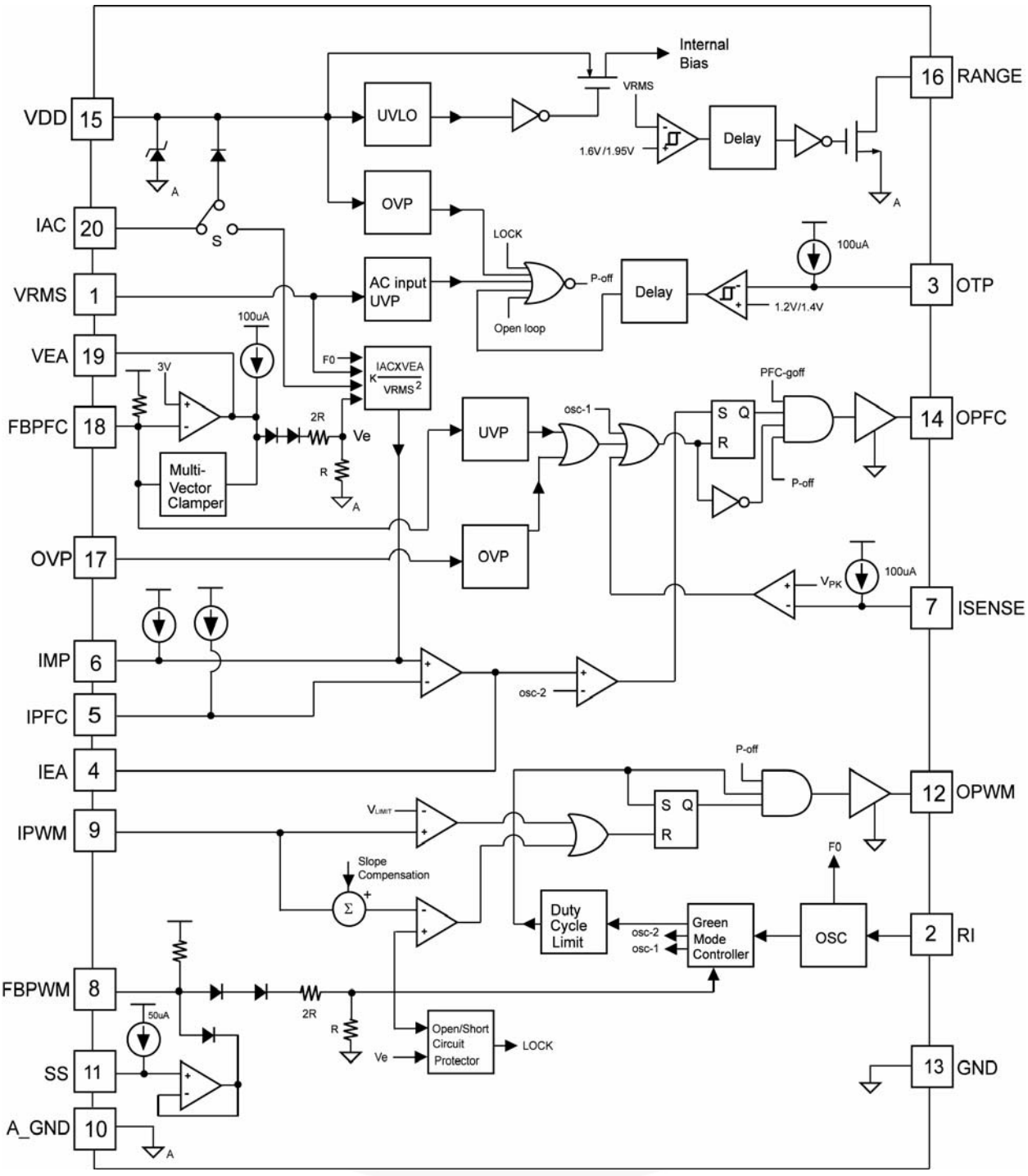

Figure 2. Block Diagram

Marking Information

T- S=SOP
P- Z=Lead Free
Null=Regular Package
XXXXXXXX- Wafer Lot
Y: Year; WW: Week
V: Assembly Location

Figure 3. Top Mark

Pin Configuration

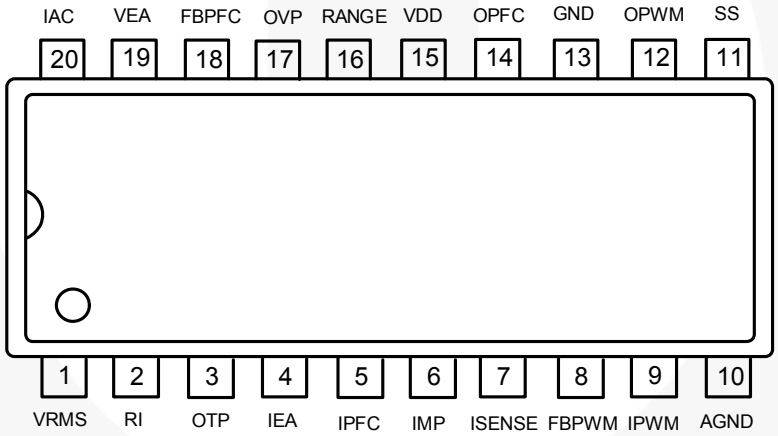

Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	VRMS	**Line Voltage Detection**. The pin is used for PFC multiplier, RANGE control of PFC output voltage, and brownout protection. For brownout protection, the controller is disabled after a delay time when the V_{RMS} voltage drops below a threshold.
2	RI	**Reference Setting**. One resistor connected between RI and ground determines the switching frequency. The switching frequency is equal to [1560 / R_I] KHz, where R_I is in KΩ. For example, if R_I is equal to 24KΩ, the switching frequency is 65KHz.
3	OTP	**Over-Temperature Protection**. A constant current is output from this pin. An external NTC thermistor must be connected from this pin to ground. The impedance of the NTC thermistor decreases whenever the temperature increases. Once the voltage of the OTP pin drops below the OTP threshold, the SG6902 is disabled.
4	IEA	**PFC Current Amplifier Output**. The signal from this pin is compared with an internal sawtooth to determine the pulse width for PFC gate drive.
5	IPFC	**Inverting Input of the PFC Current Amplifier**. Proper external compensation circuits result in excellent input power factor via average-current-mode control.
6	IMP	**Non-Inverting Input of the PFC Current Amplifier and the Output of Multiplier**. Proper external compensation circuits results in excellent input power factor via average-current-mode control.
7	ISENSE	**Current Limit**. A resistor from this pin to GND sets the current limit.
8	FBPWM	**Control Input for Voltage-Loop Feedback of PWM Stage**. It is internally pulled high through a 6.5kΩ resistance. Usually an external opto-coupler from secondary feedback circuit is connected to this pin.
9	IPWM	**Current-Sense Input for the flyback PWM.** Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
10	AGND	**Signal Ground**.
11	SS	**Soft-Start**. During startup, the SS pin charges an external capacitor with a 50μA (R_I=24KΩ) constant current source. The voltage on FBPWM is clamped by SS during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin quickly discharges.
12	OPWM	**Totem-Pole Output Drive for the Flyback PWM MOSFET**. This pin is internally clamped under 17V to protect the MOSFET.
13	GND	**Power Ground**.
14	OPFC	**Totem-Pole Output Drive for the PFC MOSFET**. This pin is internally clamped under 17V to protect the MOSFET.
15	VDD	**Power Supply Pin**.
16	RANGE	**RANGE Pin**. High impedance whenever the V_{RMS} voltage is lower than a threshold.
17	OVP	**PFC Stage Over-Voltage Input**. The comparator disables the PFC output driver if the voltage at this input exceeds a threshold. This pin can be connected to FBPFC or it can be connected to the PFC boost output through a divider network.
18	FBPFC	**Feedback Input for PFC Voltage Loop**. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
19	VEA	**Error Amplifier Output for PFC Voltage Feedback Loop.** A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value results in a narrow bandwidth and improves the power factor.
20	IAC	**Input used to Provide Current Reference for the Multiplier**.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{VDD}	DC Supply Voltage			25	V
I_{AC}	Input AC Current			2	mA
V_{HIGH}	OPWM, OPFC, IAC		-0.3	25.0	V
V_{LOW}	Others		-0.3	7.0	V
P_D	Power Dissipation at T_A< 50°C (SOP)			1.15	W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
Θ_{JC}	Thermal Resistance (Junction-to-case)			23.64	°C/W
T_L	Lead Temperature (Soldering)			+260	°C
ESD	Electrostatic Discharge Capability	Machine Model, JESD22-A115		4.5	KV
		HBM Model, JESD22-A114		250	V

Notes:
1. All voltage values, except differential voltage, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-30	+85	°C

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} SECTION						
V_{DD-OP}	Continuously Operating Voltage				20	V
I_{DD-ST}	Startup Current	0V < V_{DD} < V_{DD-ON}		10	25	μA
I_{DD-OP}	Operating Current	V_{DD}=15V; OPFC, OPWM Open; R_I=24KΩ		6	10	mA
V_{DD-ON}	Start Threshold Voltage		15	16	17	V
V_{DD-OFF}	Minimum Operating Voltage		9	10	11	V
V_{DD-OVP}	V_{DD} OVP Threshold		23.5	24.5	25.5	V
$t_{D-VDDOVP}$	Debounce Time of V_{DD} OVP	R_I=24KΩ	8		25	μs
$V_{DD-TH-G}$	V_{DD} Low-Threshold Voltage to Exit Green-off Mode		V_{DD-OFF}+0.9	V_{DD-OFF}+1.5	V_{DD-OFF}+2.1	V
OSCILLATOR SECTION						
f_{OSC}	PWM Frequency	R_I=24KΩ	62	65	68	KHz
$f_{OSC-MINFREQ}$	PWM Frequency	R_I=24KΩ	18.0	20.0	22.5	KHz
R_I	RI Pin Resistance Range		15.6		47.0	KΩ
V_{RI}	RI Voltage		1.176	1.200	1.224	V
R_{I-OPEN}	RI Pin Open Protection	If R_I>R_{I-OPEN}, SG6902 Turns off		200		KΩ
$R_{I-SHORT}$	RI Pin Short Protection	If R_I<$R_{I-SHORT}$, SG6902 Turns off		2		KΩ

Continued on following page…

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RMS} SECTION (for UVP and RANGE)						
$V_{RMS-UVP-1}$	RMS AC Voltage Under-Voltage Protection Threshold (with t_{UVP} Delay)		0.75	0.80	0.85	V
$V_{RMS-UVP-2}$	Recovery Level on V_{RMS}		$V_{RMS-UVP-1}$ + 0.16V	$V_{RMS-UVP-1}$ + 0.18V	$V_{RMS-UVP-1}$ + 0.2V	V
t_{D-PWM}	When UVP Occurs, Interval from PFC Off to PWM Off	R_I=24KΩ	$t_{UVP-Min}$+9		$t_{UVP-Min}$+14	ms
t_{UVP}	Under-Voltage Protection Delay Time(3)	R_I=24KΩ	150	195	240	ms
V_{RMS-H}	High V_{RMS} Threshold for RANGE Comparator		1.90	1.95	2.00	V
V_{RMS-L}	Low V_{RMS} Threshold for RANGE Comparator		1.55	1.60	1.65	V
t_{RANGE}	Range-Enable Delay Time	R_I=24KΩ	140	170	200	ms
V_{OL}	Output Low Voltage of RANGE Pin	I_o=1mA			0.5	V
I_{OH}	Output High Leakage Current of RANGE Pin	RANGE=5V			50	nA
PFC STAGE						
Voltage Error Amplifier						
V_{REF}	Reference Voltage		2.95	3.00	3.05	V
Av	Open-Loop Gain			60		dB
Z_o	Output Impedance			110		KΩ
OVP_{PFC}	PFC Over-Voltage Protection (OVP Pin)		3.20	3.25	3.30	V
$\triangle OVP_{PFC}$	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
$t_{OVP-PFC}$	Debounce Time of PFC OVP	R_I=24KΩ	40	70	120	µs
$V_{FBPFC-H}$	Clamp-High Feedback Voltage		3.10	3.15	3.20	V
$G_{FBPFC-H}$	Clamp-High Gain			0.5		µA/mV
$V_{FBPFC-L}$	Clamp-Low Feedback Voltage		2.75	2.85	2.90	V
$G_{FBPFC-L}$	Clamp-Low Gain			6.5		mA/mV
$I_{FBPFC-L}$	Maximum Source Current		1.5	2.0		mA
$I_{FBPFC-H}$	Maximum Sink Current		70	110		µA
UVP_{FBPFC}	PFC Feedback Under-Voltage Protection		0.35	0.40	0.45	V
V_{FBHIGH}	FB Open Voltage		6	7	8	V
$t_{UVP-FBPFC}$	Debounce Time of PFC UVP	R_I=24KΩ	40	70	120	µs

Note:

3. No delay time at startup.

Continued on following page…

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CURRENT ERROR AMPLIFIER						
V_{OFFSET}	Input Offset Voltage			8		mV
A_I	Open-Loop Gain			60		dB
BW	Unit Gain Bandwidth			1.5		MHz
CMRR	Common Mode Rejection Ratio	V_{CM}=0 to +1.5V		70		dB
$V_{OUT-HIGH}$	Output High Voltage		3.2			V
$V_{OUT-LOW}$	Output Low Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current Source	R_I=24KΩ (I_{MR}=20+I_{RI}•0.8)	50		70	μA
I_L	Maximum Source Current		3			mA
I_H	Maximum Sink Current			0.25		mA
PEAK CURRENT LIMIT						
I_P	Constant Current Output	R_I=24KΩ	90	100	110	μA
V_{PK}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{SENSE} < V_{PK})	V_{RMS}=1.05V	0.15	0.20	0.25	V
		V_{RMS}=3V	0.35	0.40	0.45	V
t_{PD-PFC}	Propagation Delay				200	ns
$t_{LEB-PFC}$	Leading-Edge Blanking Time		270	350	450	ns
MULTIPLIER						
I_{AC}	Input AC Current	Multiplier Linear Range	0		360	μA
I_{MO-max}	Maximum Multiplier Current Output	R_I=24KΩ		250		μA
I_{MO-1}	Multiplier Current Output (Low-Line, High-power)	V_{RMS}=1.05V; I_{AC}=90μA; V_{EA}=7.5V; R_I=24KΩ	200	250	280	μA
I_{MO-2}	Multiplier Current Output (High-Line, High-power)	V_{RMS}=3V; I_{AC}=264μA; V_{EA}=7.5V; R_I=24KΩ	65	85		μA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V
PFC OUTPUT DRIVER						
V_{Z-PFC}	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
V_{OL-PFC}	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
t_{PFC}	Interval OPFC Lags Behind OPWM at Startup		9.0	11.5	14.0	ms
V_{OH-PFC}	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
t_{R-PFC}	Rising Time	V_{DD}=15V; C_L=5nF; OPFC=2V to 9V	40	70	120	ns
t_{F-PFC}	Falling Time	V_{DD}=15V; C_L=5nF; OPFC=9V to 2V	40	60	110	ns
DCY_{MAX}	Maximum Duty Cycle		93		98	%

Continued on following page…

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PWM STAGE						
FBPWM						
$A_{v\text{-}PWM}$	FB to Current Comparator Attenuation		2.5	3.1	3.5	V/V
Z_{FB}	Input Impedance(4)		4	5	7	KΩ
I_{FB}	Maximum Source Current		0.8	1.2	1.5	mA
$FB_{OPEN\text{-}LOOP}$	PWM Open-Loop Protection Voltage		4.2	4.5	4.8	V
$t_{OPEN\text{-}PWM}$	PWM Open-Loop Protection Delay Time		45	56	70	ms
$V_{PFC\text{-}OFF1}$	PFC Off Voltage at FBPWM	RANGE=Ground		V_G+0.2V		V
$V_{PFC\text{-}OFF2}$	PFC Off Voltage at FBPWM	RANGE=Open		V_G+0.2V		V
$t_{PFC\text{-}OFF}$	PFC Off Delay Time	R_I=24kΩ	500	650	800	ms
$V_{PFC\text{-}ON\ 1.6}$	PFC On Voltage at FBPWM	RANGE=Ground V_{RMS}=1.6V		V_G+0.35V		V
$V_{PFC\text{-}ON\ 2.85}$	PFC On Voltage at FBPWM	RANGE=Ground V_{RMS}=2.85V		V_G+0.35V		V
$V_{PFC\text{-}ON\ 0.8}$	PFC On Voltage at FBPWM	RANGE=Open V_{RMS}=0.8V		V_G+0.85V		V
$V_{PFC\text{-}ON\ 1.95}$	PFC On Voltage at FBPWM	RANGE=Open V_{RMS}=1.95V		V_G+0.5V		V
V_N	Frequency Reduction Threshold on FBPWM	RANGE=Ground	1.9	2.1	2.3	V
S_G	Green Mode Modulation Slope(4)		60	75	90	Hz/V
V_G	Voltage on FBPWM at f_S=20KHz		1.35	1.60	1.75	V
PWM CURRENT SENSE						
$t_{PD\text{-}PWM}$	Propagation Delay to Output	V_{DD}=15V, OPWM<=9V	60		120	ns
$V_{LIMIT\text{-}1}$	Peak Current Limit Threshold Voltage1	RANGE=Open	0.65	0.70	0.75	V
$V_{LIMIT\text{-}2}$	Peak Current Limit Threshold Voltage2	RANGE=Ground	0.60	0.65	0.70	V
$t_{BNK\text{-}PWM}$	Leading-Edge Blanking Time		270	350	450	ns
ΔV_{SLOPE}	Slope Compensation	$\Delta V_S=\Delta V_{SLOPE}$ x (t_{ON}/t) ΔV_S: Compensation Voltage Added to Current Sense	0.45	0.50	0.55	V

Note:

4. Guaranteed by design.

Continued on following page…

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PWM OUTOUT DRIVER						
V_{Z-PWM}	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
V_{OL-PWM}	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
V_{OH-PWM}	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
t_{R-PWM}	Rising Time	V_{DD}=15V; C_L=5nF; OPWM=2V to 9V	30	60	120	ns
t_{F-PWM}	Falling Time	V_{DD}=15V; C_L=5nF; OPWM=9V to 2V	30	50	110	ns
DCY_{MAXPWM}	Maximum Duty Cycle		73	78	83	%
OTP SECTION						
I_{OTP}	OTP Pin Output Current	R_I=24KΩ	90	100	110	μA
V_{OTP-ON}	Recovery Level on OTP		1.35	1.40	1.45	V
$V_{OTP-OFF}$	OTP Threshold Voltage		1.15	1.20	1.25	V
t_{OTP}	OTP Debounce Time		8		25	μs
SOFT-START SECTION						
I_{SS}	Constant Current Output for Soft-Start	R_T=24KΩ	44	50	56	μA
R_D	Discharge R_{DSON}			470		Ω

Typical Performance Characteristics

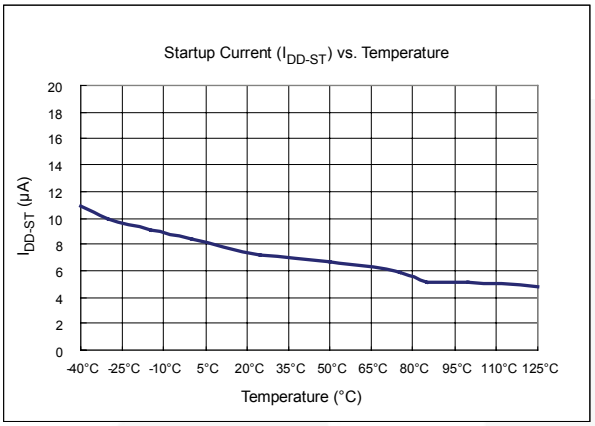

Figure 5. Startup Current

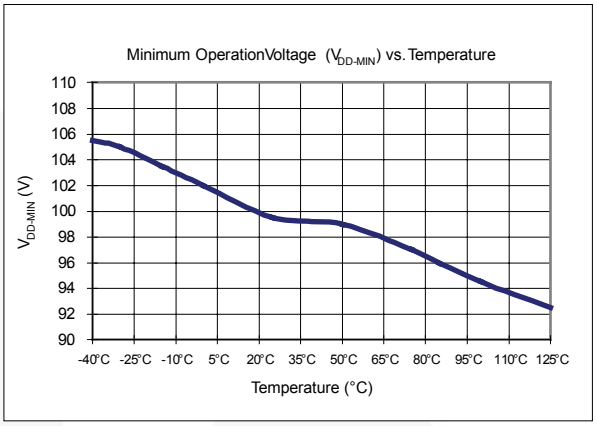

Figure 6. V_{DD-MIN} Threshold Voltage

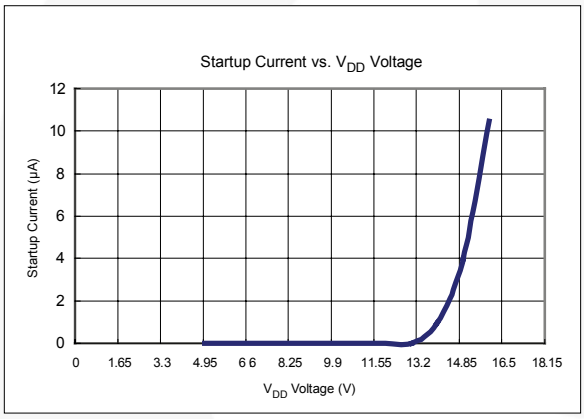

Figure 7. Startup Current vs. V_{DD} Voltage

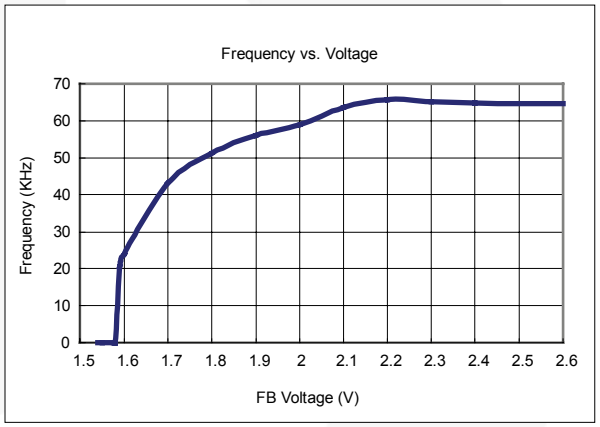

Figure 8. PWM Frequency vs. FB Voltage

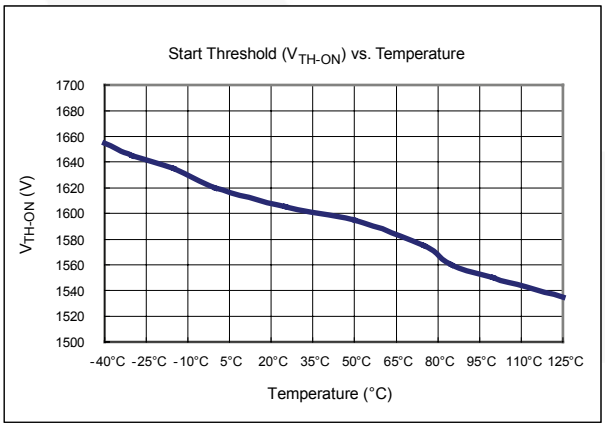

Figure 9. V_{TH-ON} Threshold Voltage

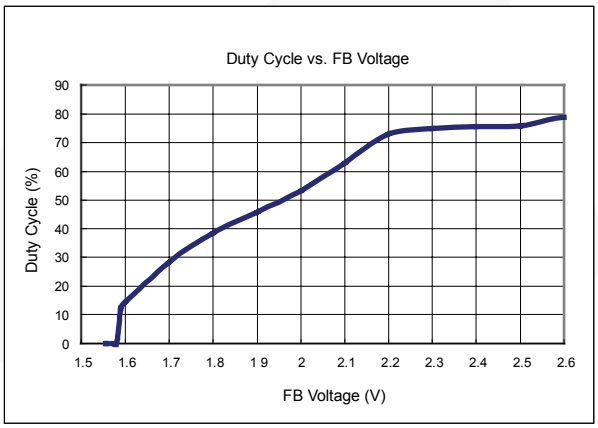

Figure 10. Duty Cycle vs. FB Voltage

Typical Performance Characteristics (Continued)

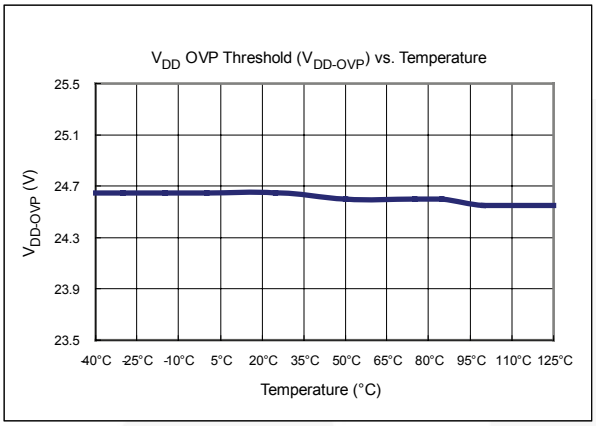

Figure 11. V_{DD} OVP

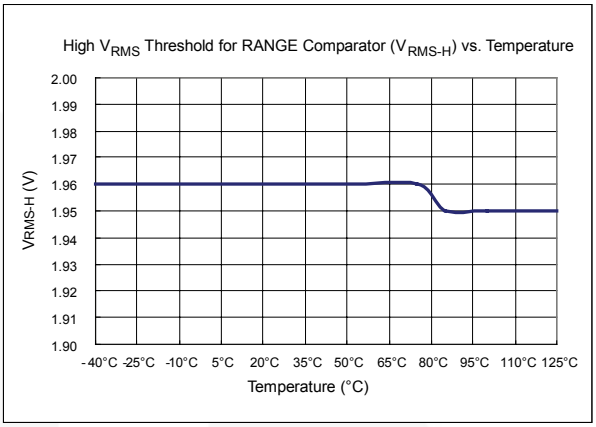

Figure 12. High V_{RMS} Threshold for RANGE

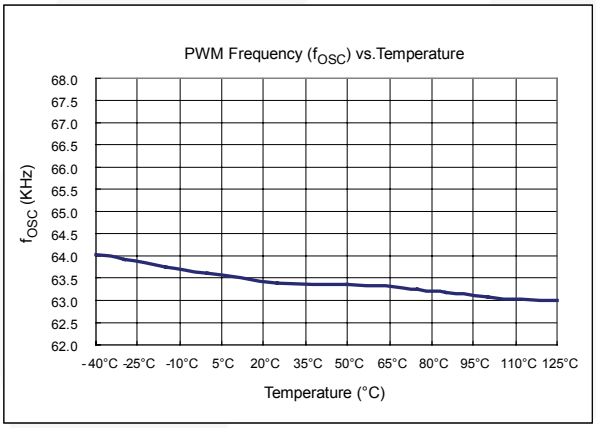

Figure 13. PWM Frequency

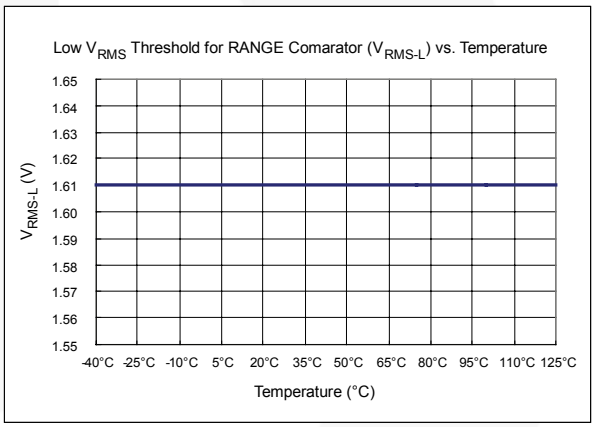

Figure 14. Low V_{RMS} Threshold for RANGE

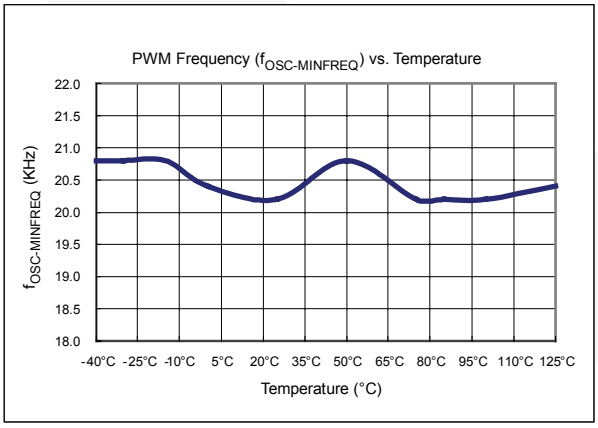

Figure 15. PWM Frequency ($f_{OSC-MINFREQ}$)

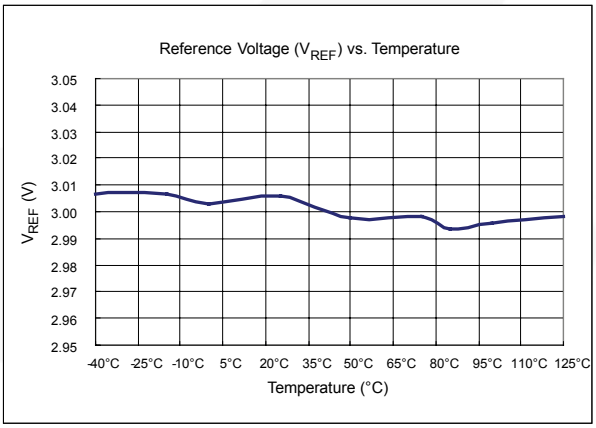

Figure 16. Reference Voltage

Typical Performance Characteristics (Continued)

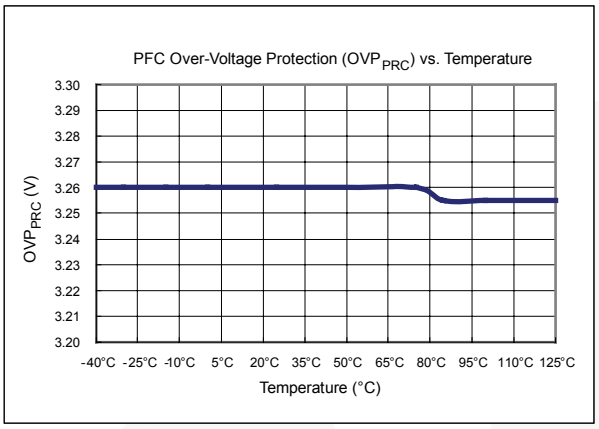

Figure 17. PFC Over-Voltage Protection

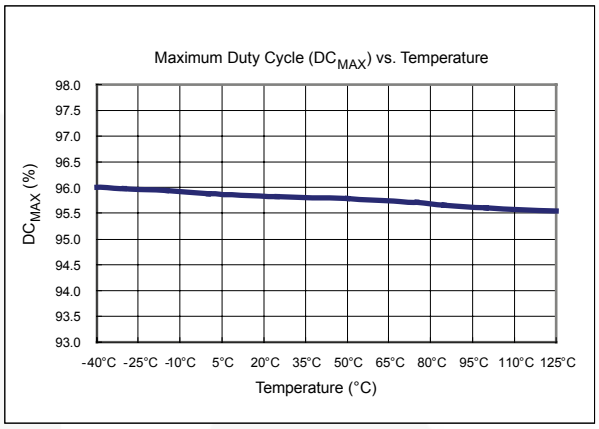

Figure 18. Maximum Duty Cycle (OPFC)

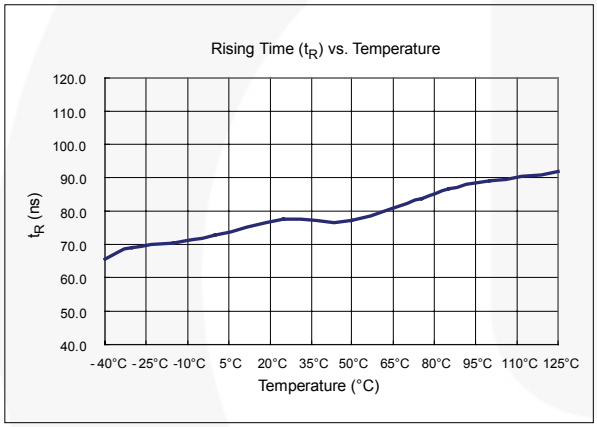

Figure 19. Rising Time (OPFC)

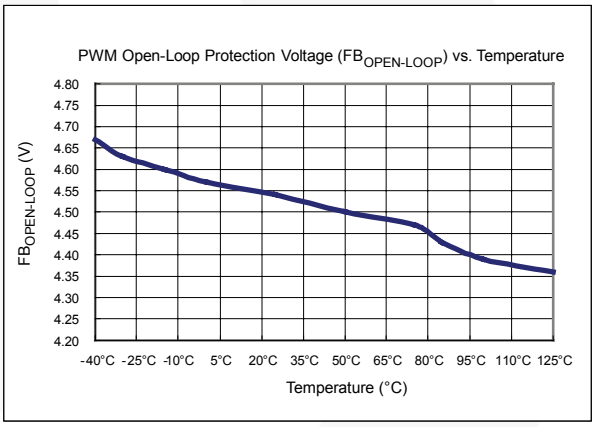

Figure 20. PWM Open-Loop Protection

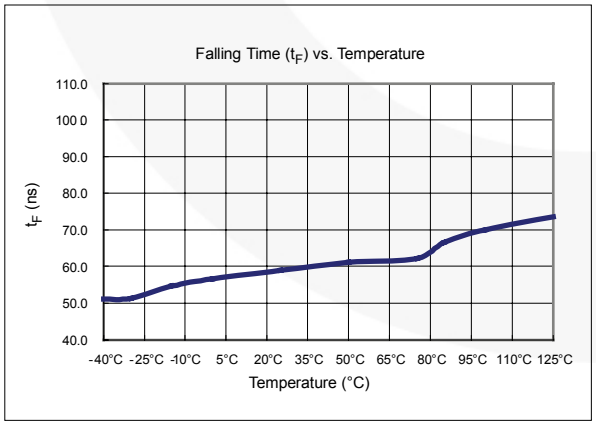

Figure 21. Falling Time (OPFC)

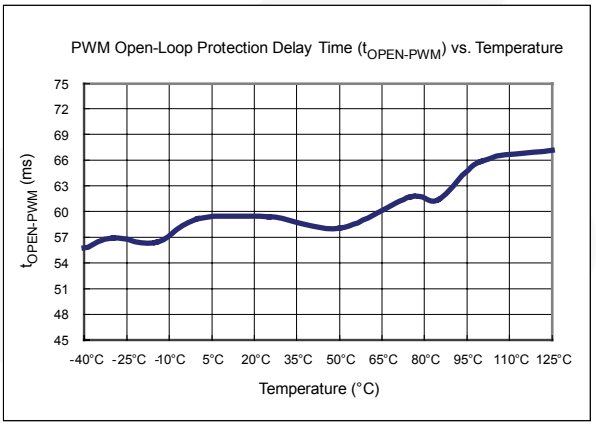

Figure 22. PWM Open-Loop Protection Delay Time

Typical Performance Characteristics (Continued)

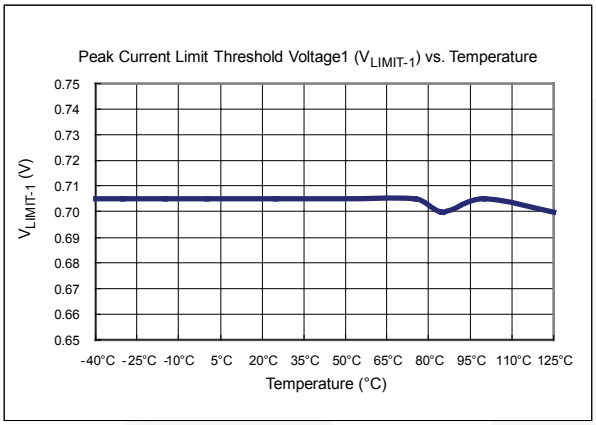

Figure 23. Peak Current Limit Threshold Voltage

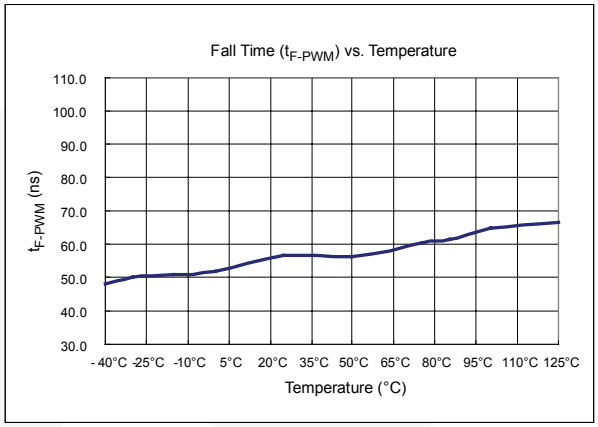

Figure 24. Falling Time (OPWM)

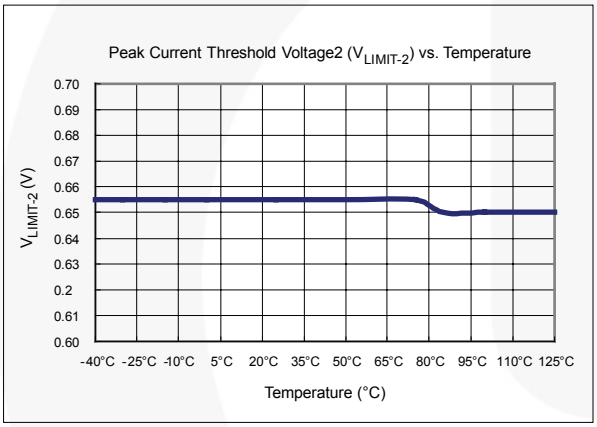

Figure 25. Peak Current Limit-2 Threshold Voltage

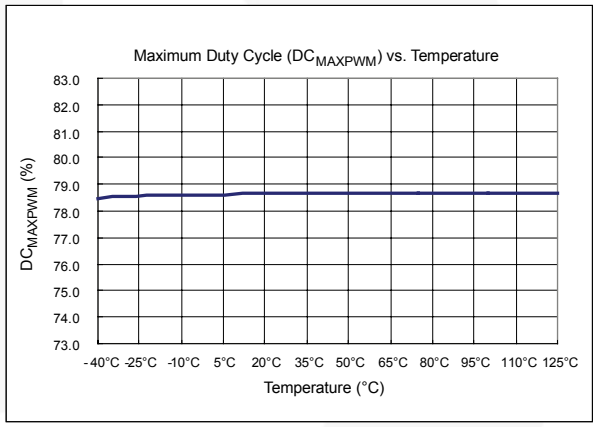

Figure 26. Maximum Duty Cycle (OPWM)

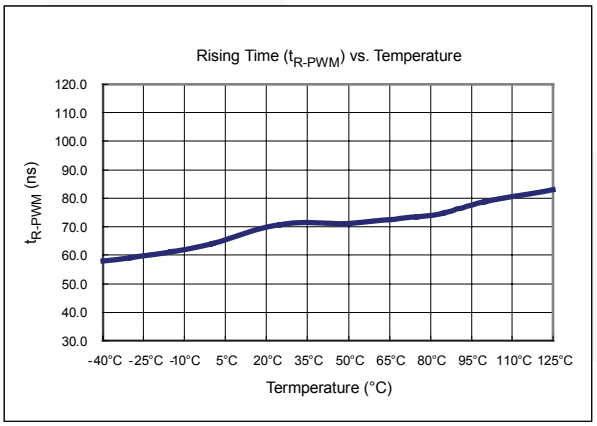

Figure 27. Rising Time (OPWM)

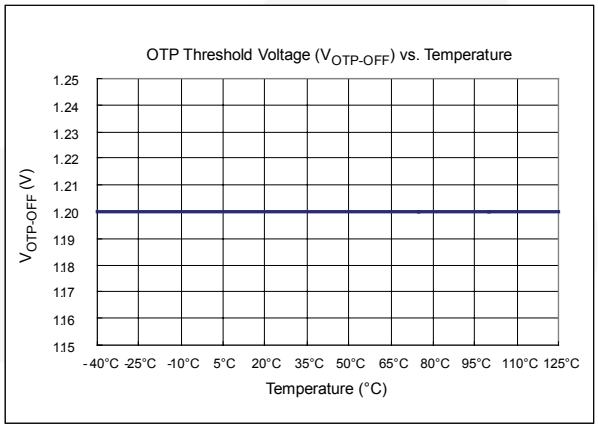

Figure 28. OTP Threshold Voltage

Functional Description

The highly integrated SG6902 is designed for power supplies with boost PFC and flyback PWM. It requires very few external components to achieve green-mode operation and versatile protections / compensation.

The proprietary interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light loads, the switching frequency is continuously decreased to reduce power consumption. If output loading is reduced, the PFC stage is turned off to reduce power consumption.

The PFC function is implemented by average-current-mode control. The proprietary switching charge multiplier-divider provides a high-degree noise immunity for the PFC circuit. The proprietary multi-vector output voltage control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6902 shuts off PFC to prevent extra-high voltage on output. Programmable two-level output voltage control reduces the PFC output voltage at low line input to increase the efficiency of the power supply.

For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-mode operation. Built-in line-voltage compensation maintains constant output power limit. Hiccup operation during output overloading is also guaranteed. To prevent the power supply from drawing large current during startup, the startup for PFC stage is delayed 11.5ms after the operation of PWM stage.

In addition, SG6902 provides complete protection functions, such as brownout, over-voltage, and RI pin open/short protections.

Startup

Figure 29 shows the startup circuit. A resistor R_{AC} is utilized to charge V_{DD} capacitor through S1. The turn-on and turn-off thresholds are fixed internally at 16V and 10V. During startup, the hold-up capacitor must be charged to 16V through the startup resistor to enable SG6902. The hold-up capacitor continues to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 10V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during startup. Since SG6902 consumes less than 25μA startup current, the value of R_{AC} can be large to reduce power consumption. One 10μF capacitor should hold enough energy for successful startup. After startup, S1 switches so that the current I_{AC} is the input for PFC multiplier. This helps reduce circuit complexity and power consumption.

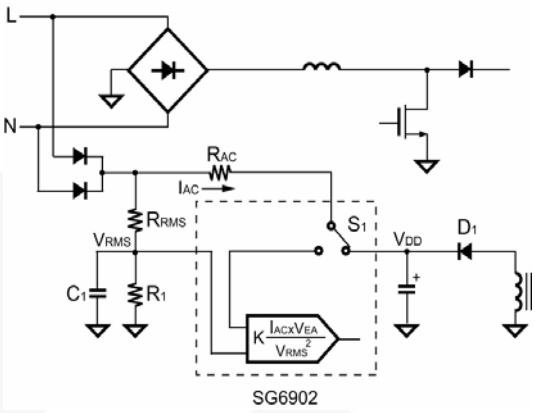

Figure 29. Startup Circuit

Switching Frequency and Current Sources

The switching frequency can be programmed by the resistor RI connected between RI pin and GND. The relationship is:

$$f_{OSC} = \frac{1560}{R_I\ (k\Omega)}(kHz) \quad (1)$$

For example, a 24KΩ resistor R_I results in a 65KHz switching frequency. Accordingly, a constant current, I_T, flows through R_I:

$$I_T = \frac{1.2V}{R_I\ (k\Omega)}(mA) \quad (2)$$

I_T is used to generate internal current reference.

Line Voltage Detection (VRMS)

Figure 30 shows a resistive divider with low-pass filtering for line-voltage detection on the VRMS pin. The V_{RMS} voltage is used for the PFC multiplier, brownout protection, and range control.

For brownout protection, the SG6902 is disabled with a 195ms delay time if the voltage V_{RMS} drops below 0.8V.

For PFC multiplier and range control, refer to the PFC Operation section below for details.

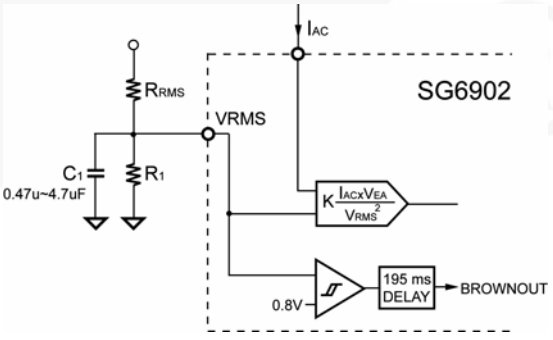

Figure 30. Line-Voltage Detection Circuit

Interleave Switching and Green Mode

The SG6902 uses interleaved switching to synchronize the PFC and flyback stages, which reduces switching noise and spreads the EMI emissions. Figure 31 shows off-time, t_{OFF}, inserted between the turn-off of the PFC gate drive and the turn-on of the PWM.

The off-time t_{OFF} is increased in response to the decreasing of the voltage level of FBPWM. Therefore, the PWM switching frequency is continuously decreased to reduce switching losses. To further reduce power losses under extra light-load conditions, the PFC stage is turned off with a 650ms delay time.

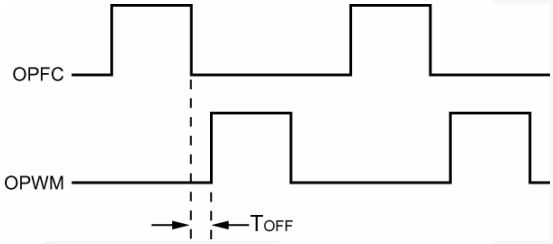

Figure 31. Interleaved Switching Pattern

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase follow that of the input voltage. Average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and switching charge multiplier-divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 32 shows the total control loop for the average-current-mode control circuit.

The current source output from the switching charge multiplier-divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (\mu A) \quad (4)$$

I_{IMP}, the current output from the IMP pin, is the summation of IMO and IMR1. IMR1 and IMR2 are identical fixed-current sources. R_2 and R_3 are also identical. They are used to pull high the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground. The constant current sources IMR1 and IMR2 are typically 60μA.

Through the differential amplification of the signal across R_S, better noise immunity is achieved. The output of I_{EA} is compared with an internal sawtooth and the pulse width for PFC is determined. Through the average current-mode control loop, the input current, I_S, is proportional to I_{MO}:

$$I_{MO} \times R_2 = I_S \times R_S \quad (5)$$

According to Equation 5, the minimum value of R_2 and maximum of R_S can be determined, because IMO should not exceed the specified maximum value.

There are different concerns in determining the value of the sense resistor R_S. The value of R_S should be small enough to reduce power consumption, but large enough to maintain the resolution. A current transformer (CT) can improve the efficiency of high-power converters.

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as DC as possible, according to Equation 6. Good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The transconductance error amplifier has output impedance Z_O (>90kΩ) and a capacitor C_{EA} (1μF ~ 10μF) that should be connected to ground (as shown in Figure 32). This establishes a dominant pole f1 for the voltage loop:

$$f_1 = \frac{1}{2\pi \times Z_O \times C_{EA}} \quad (6)$$

The average total input power can be expressed as:

$$\begin{aligned} Pin &= V_{IN(rms)} \times I_{IN(rms)} \\ &\propto V_{RMS} \times I_{MO} \\ &\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} \\ &\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^2} \\ &= \sqrt{2} \times \frac{V_{EA}}{R_{AC}} \end{aligned} \quad (7)$$

V_{EA}, the output of the voltage error amplifier, controls the total input power and the power delivered to the load.

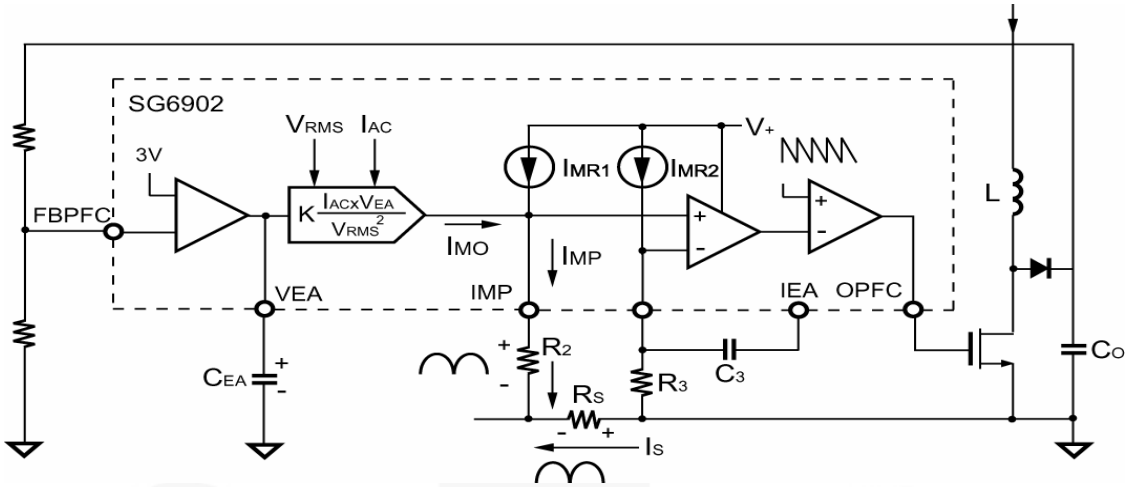

Figure 32. Average-Current-Mode Control Loop

Multi-Vector Error Amplifier

The voltage-loop error amplifier is transconductance, which has high output impedance (> 90kΩ). A capacitor C_{EA} (1μ ~ 10μF) connected from V_{EA} to ground provides a dominant pole for the voltage loop. Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative multi-vector error amplifier provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 33 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ±5% of the reference voltage, the transconductance error amplifier adjusts its output impedance to increase the loop response. If R_A is opened, SG6902 shuts off immediately to prevent extra-high voltage on the output capacitor.

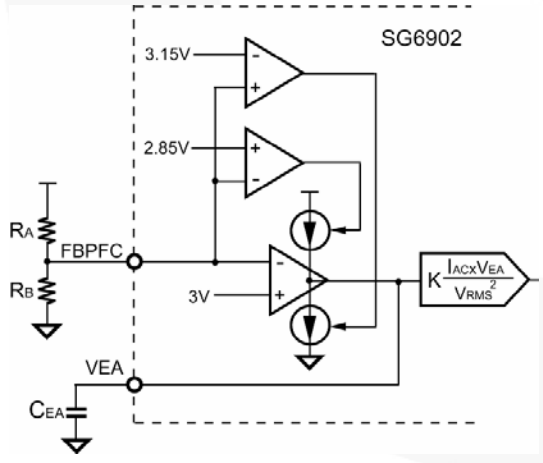

Figure 33. Multi-Vector Error Amplifier

PFC Over-Voltage Protection

When the OVP feedback voltage exceeds the over-voltage threshold, the SG6902 inhibits the PFC switching signal. This protection also prevents the PFC power converter from operating abnormally while the FBPFC pin is open.

Cycle-by-Cycle Current Limiting

SG6902 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 34 shows the peak current limit for the PFC stage. The PFC gate drive is terminated once the voltage on the ISENSE pin goes below V_{PK}.

The voltage of V_{RMS} determines the voltage of V_{PK}. The relationship between V_{PK} and V_{RMS} is shown in Figure 34.

The amplitude of the constant current, I_P, is determined by the internal current reference, I_T, according to the following equation:

$$I_P = 2 \times I_T = 2 \times \frac{1.2V}{R_I} \quad (8)$$

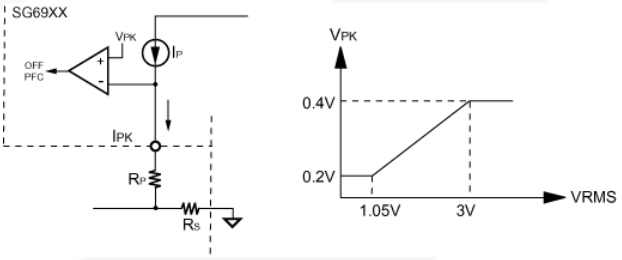

Figure 34. V_{RMS} Controlled Current Limiting

The peak current of the ISENSE is given by (V_{RMS}<1.05V):

$$I_{S\_peak} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad (9)$$

Flyback PWM and Slope Compensation

As shown in Figure 35, peak-current-mode control is utilized for flyback PWM. The SG6902 inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation ensures stable operation for continuous-current-mode operation.

When the IPWM voltage across the sense resistor, reaches the threshold voltage, 0.65V or 0.7V selected by RANGE, the OPWM is turned off after a small propagation delay, t_{PD-PWM}. This propagation delay introduces additional current, proportional to $t_{PD-PWM} \cdot V_{PFC}/L_P$, where V_{PFC} is the output voltage of P_{FC} and L_P is the magnetized inductance of the flyback transformer. Since the propagation delay is nearly constant, higher V_{PFC} results in a larger additional current and the output power limit is higher than under low V_{PFC}. To compensate for this variation, the peak current threshold is modulated by the RANGE output. When RANGE is shorted to GND, the PFC output voltage is high and the corresponding threshold is 0.65V. When RANGE is opened, the PFC output voltage is low and the corresponding threshold is 0.7V.

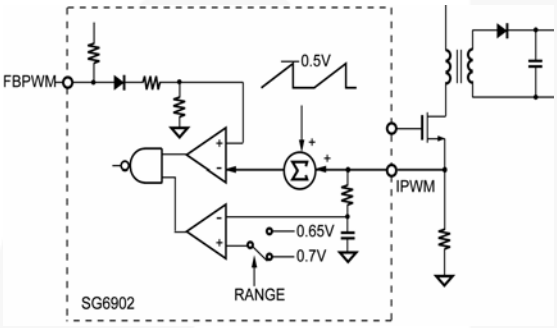

Figure 35. Peak Current Control Loop

Limited Power Control

Every time the output of power supply is shorted or overloaded, the FBPWM voltage increases. If the FB voltage is higher than a designed threshold, 4.5V, for longer than 56ms, the OPWM is turned off. As OPWM is turned off, the supply voltage V_{DD} begins decreasing.

When V_{DD} is lower than the turn-off threshold, such as 10V, SG6902 is totally shut down. Due to the startup resistor, V_{DD} is charged up to the turn-on threshold voltage, 16V, until enabled again. If the overloading condition persists, the protection occurs repeatedly to prevent the power supply from being overheated during overload condition.

Over-Temperature Protection

An OTP pin provides over-temperature protection. A constant current is output from this pin. If R_I is equal to 24kΩ, the magnitude of the constant current is 100μA. An external NTC thermistor must be connected from this pin to ground, as shown as Figure 36. When the OTP voltage drops below 1.2V, SG6902 is disabled until the OTP voltage exceeds 1.4V.

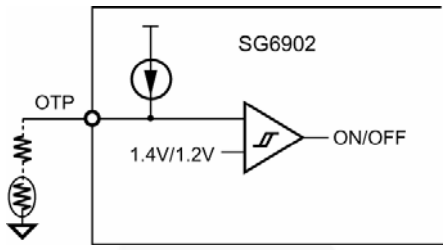

Figure 36. OTP Function

Soft-Start

During startup of PWM stage, the SS pin charges an external capacitor with a constant current source. The voltage on FBPWM is clamped by SS voltage during startup. In the event of a protection condition and/or PWM being disabled, the SS pin quickly discharges.

Gate Driver

SG6902 output stage is a fast totem-pole gate driver. The output driver is clamped by an internal 18V Zener diode to protect the power MOSFET.

PCB Layout

SG6902 has two ground pins. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near the SG6902. A resistor (5 ~ 20Ω) is recommended, connected in series from the OPFC and OPWM, to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure 37 shows an example of the PCB layout. The ground trace connected from the AGND pin to the decoupling capacitor should be low impedance and as short as possible. The ground trace 1 provides a signal ground and should be connected directly to the decoupling capacitor V_{DD} and/or to the AGND pin. The ground trace 2 shows that the AGND pins should connect to the PFC output capacitor C_O independently. The ground trace 3 is independently tied from the PGND to the PFC output capacitor C_O. The ground in the output capacitor C_O is the major ground reference for power switching. To provide a good ground reference and reduce switching noise of both the PFC and PWM stages, the ground traces 6 and 7 should be located very near and be low impedance.

The IPFC pin is connected directly to R_S through R_3 to improve noise immunity (do not incorrectly connect to ground trace 2). The IMP and ISENSE pins should be connected directly via the resistors R_2 and R_P to another terminal of R_S. Because ground traces 4 and 5 are PFC and PWM stages of the current loop, they should be as short as possible.

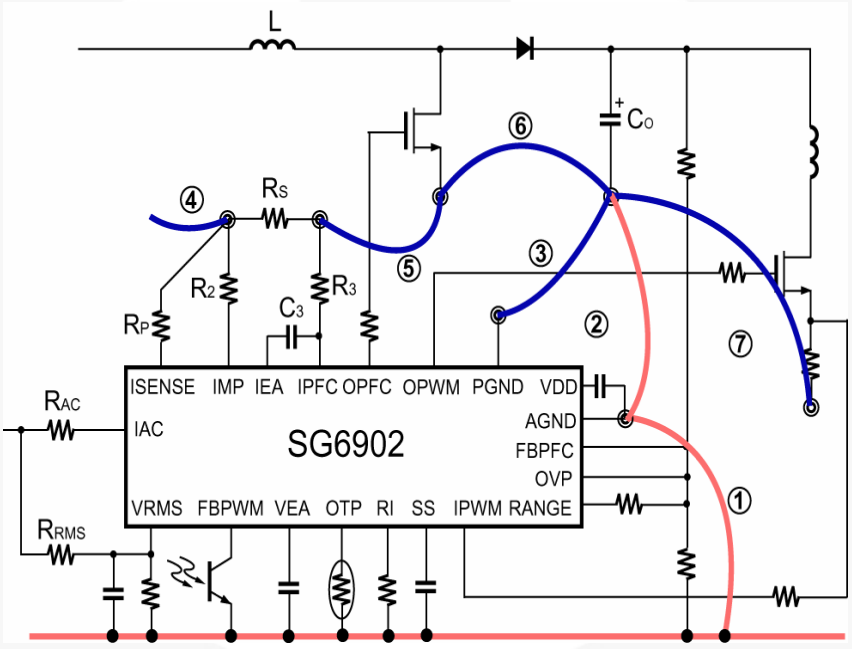

Figure 37. Layout Considerations

Physical Dimensions

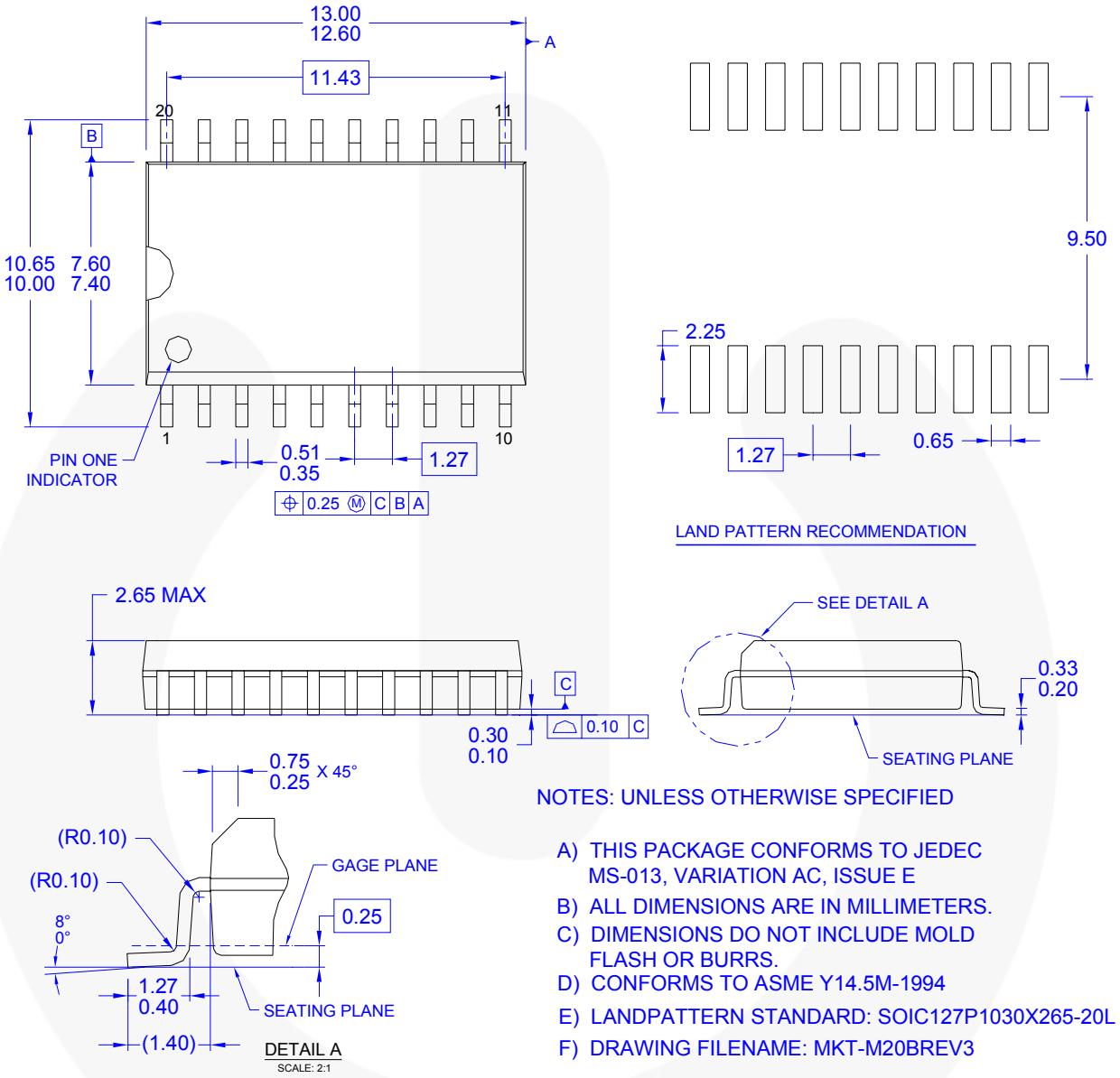

Figure 38. 20-Pin, Small Outline Package (SOIC)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging.

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EfficentMax™
EZSWITCH™ *
E²™
F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
PDP SPM™
Power-SPM™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
SYSTEM GENERAL®
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TriFault Detect™
µSerDes™
SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
XS™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I38

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

onsemi:
SG6902SZ