FAIRCHILD SEMICONDUCTOR™

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SCAN18245T
Non-Inverting Transceiver with 3-STATE Outputs

General Description

The SCAN18245T is a high speed, low-power bidirectional line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented output enable and direction control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

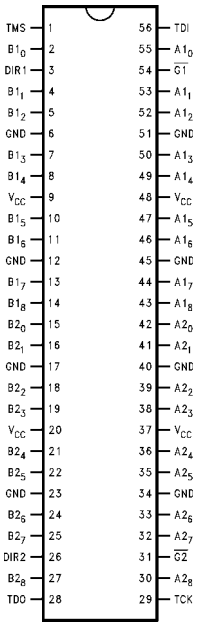
- IEEE 1149.1 (JTAG) Compliant
- Dual output enable control signals
- 3-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 32 mA/sink 64 mA
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP and HIGHZ instructions
- Member of Fairchild's SCAN Products

Ordering Code:

Order Number	Package Number	Package Description
SCAN18245TSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
$A1_{(0–8)}$	Side A1 Inputs or 3-STATE Outputs
$B1_{(0–8)}$	Side B1 Inputs or 3-STATE Outputs
$A2_{(0–8)}$	Side A2 Inputs or 3-STATE Outputs
$B2_{(0–8)}$	Side B2 Inputs or 3-STATE Outputs
$\overline{G1}$, $\overline{G2}$	Output Enable Pins
DIR1, DIR2	Direction of Data Flow Pins

Truth Table

Inputs		A1 (0–8)		B1 (0–8)
$\overline{G1}$	DIR1			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

H= HIGH Voltage Level
L= LOW Voltage Level

Inputs		A2 (0–8)		B2 (0–8)
$\overline{G2}$	DIR2			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

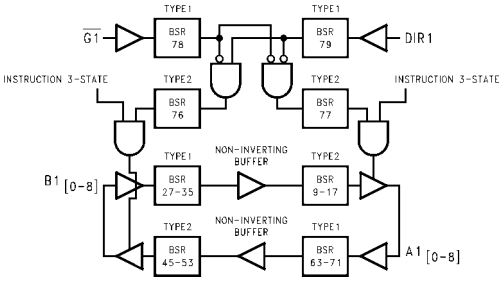
X= Immaterial
Z= High Impedance

Functional Description

The SCAN18245 consists of two sets of nine non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Direction pins (DIR1 and DIR2) LOW enables data from B Ports to A Ports, when HIGH enables data from A Ports to B Ports. The Output Enable pins ($\overline{G1}$ and $\overline{G2}$) when HIGH disables both A and B Ports by placing them in a high impedance condition.

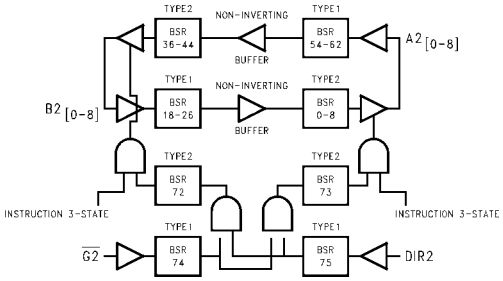
Block Diagrams

A1, B1, $\overline{G1}$ and DIR1



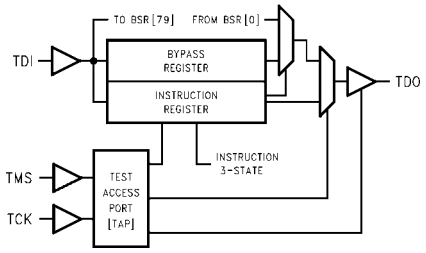
Note: BSR stands for Boundary Scan Register.

A2, B2, $\overline{G2}$ and DIR2



Note: BSR stands for Boundary Scan Register.

Tap Controller



Description of Boundary-Scan Circuitry

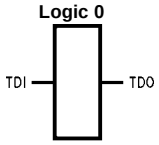
The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition

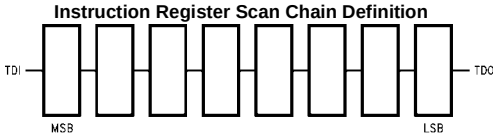
Logic 0



The INSTRUCTION register is an eight-bit register which captures the value 00111101.

The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18245T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a “pseudo ID” code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

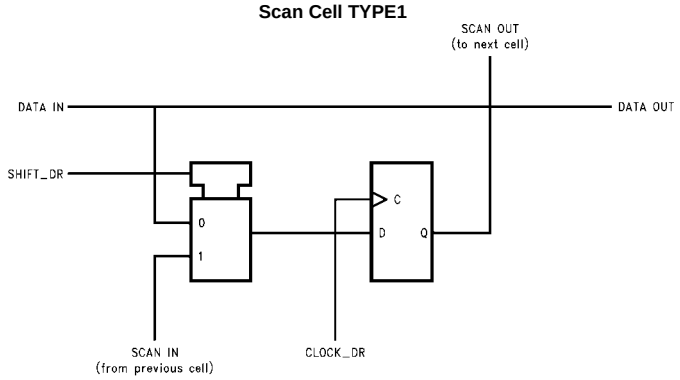
Instruction Register Scan Chain Definition



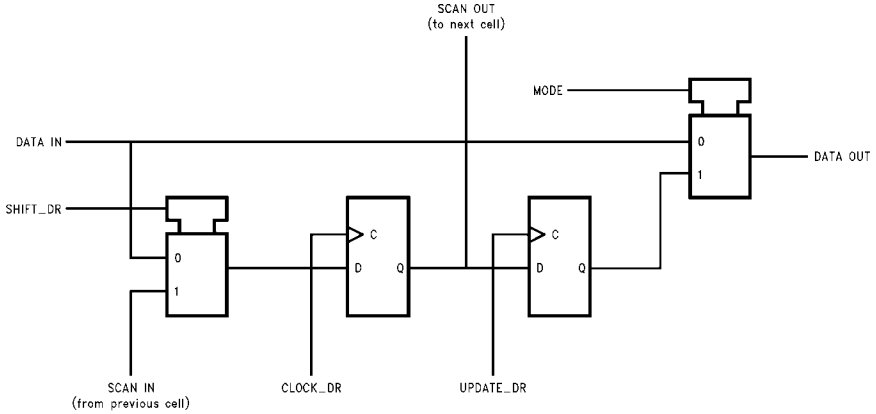
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
All Others	BYPASS

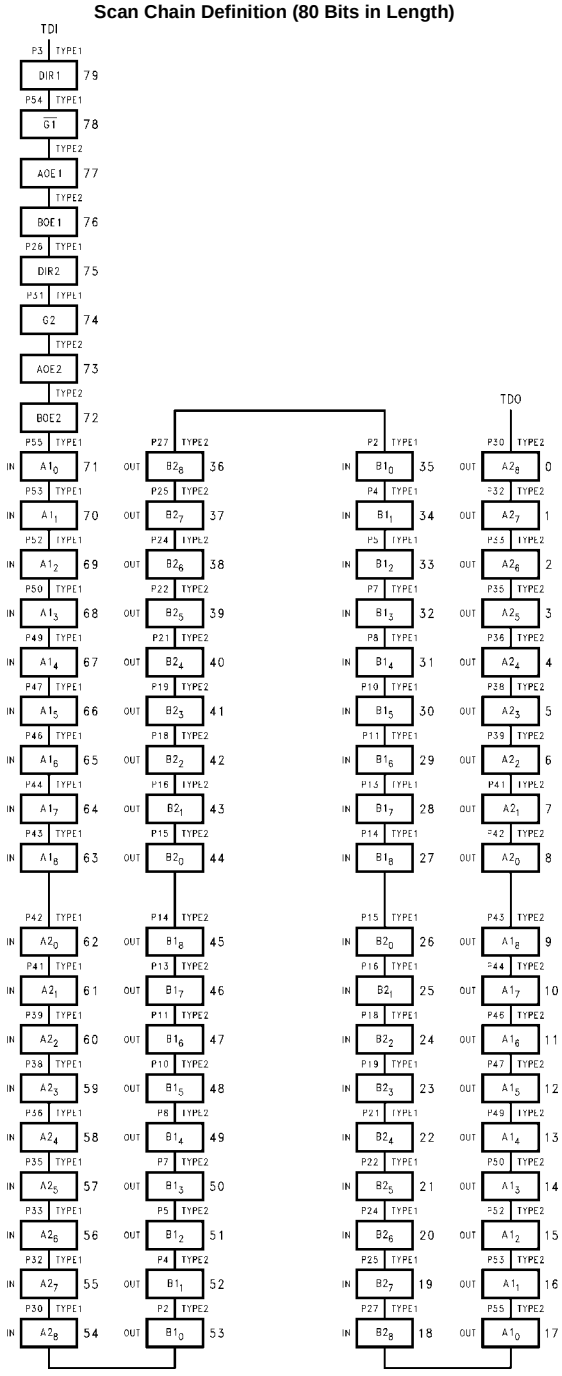
Scan Cell TYPE1



Scan Cell TYPE2



Boundary-Scan Register
Scan Chain Definition (80 Bits in Length)



Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
79	DIR1	3	Input	TYPE1	Control Signals
78	$\overline{G1}$	54	Input	TYPE1	
77	AOE_1		Internal	TYPE2	
76	BOE_1		Internal	TYPE2	
75	DIR2	26	Input	TYPE1	
74	$\overline{G2}$	31	Input	TYPE1	
73	AOE_2		Internal	TYPE2	
72	BOE_2		Internal	TYPE2	
71	$A1_0$	55	Input	TYPE1	A1–in
70	$A1_1$	53	Input	TYPE1	
69	$A1_2$	52	Input	TYPE1	
68	$A1_3$	50	Input	TYPE1	
67	$A1_4$	49	Input	TYPE1	
66	$A1_5$	47	Input	TYPE1	
65	$A1_6$	46	Input	TYPE1	
64	$A1_7$	44	Input	TYPE1	
63	$A1_8$	43	Input	TYPE1	
62	$A2_0$	42	Input	TYPE1	A2–in
61	$A2_1$	41	Input	TYPE1	
60	$A2_2$	39	Input	TYPE1	
59	$A2_3$	38	Input	TYPE1	
58	$A2_4$	36	Input	TYPE1	
57	$A2_5$	35	Input	TYPE1	
56	$A2_6$	33	Input	TYPE1	
55	$A2_7$	32	Input	TYPE1	
54	$A2_8$	30	Input	TYPE1	
53	$B1_0$	2	Output	TYPE2	B1–out
52	$B1_1$	4	Output	TYPE2	
51	$B1_2$	5	Output	TYPE2	
50	$B1_3$	7	Output	TYPE2	
49	$B1_4$	8	Output	TYPE2	
48	$B1_5$	10	Output	TYPE2	
47	$B1_6$	11	Output	TYPE2	
46	$B1_7$	13	Output	TYPE2	
45	$B1_8$	14	Output	TYPE2	
44	$B2_0$	15	Output	TYPE2	B2–out
43	$B2_1$	16	Output	TYPE2	
42	$B2_2$	18	Output	TYPE2	
41	$B2_3$	19	Output	TYPE2	
40	$B2_4$	21	Output	TYPE2	
39	$B2_5$	22	Output	TYPE2	
38	$B2_6$	24	Output	TYPE2	
37	$B2_7$	25	Output	TYPE2	
36	$B2_8$	27	Output	TYPE2	

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
35	$B1_0$	2	Input	TYPE1	B1–in
34	$B1_1$	4	Input	TYPE1	
33	$B1_2$	5	Input	TYPE1	
32	$B1_3$	7	Input	TYPE1	
31	$B1_4$	8	Input	TYPE1	
30	$B1_5$	10	Input	TYPE1	
29	$B1_6$	11	Input	TYPE1	
28	$B1_7$	13	Input	TYPE1	
27	$B1_8$	14	Input	TYPE1	
26	$B2_0$	15	Input	TYPE1	B2–in
25	$B2_1$	16	Input	TYPE1	
24	$B2_2$	18	Input	TYPE1	
23	$B2_3$	19	Input	TYPE1	
22	$B2_4$	21	Input	TYPE1	
21	$B2_5$	22	Input	TYPE1	
20	$B2_6$	24	Input	TYPE1	
19	$B2_7$	25	Input	TYPE1	
18	$B2_8$	27	Input	TYPE1	
17	$A1_0$	55	Output	TYPE2	A1–out
16	$A1_1$	53	Output	TYPE2	
15	$A1_2$	52	Output	TYPE2	
14	$A1_3$	50	Output	TYPE2	
13	$A1_4$	49	Output	TYPE2	
12	$A1_5$	47	Output	TYPE2	
11	$A1_6$	46	Output	TYPE2	
10	$A1_7$	44	Output	TYPE2	
9	$A1_8$	43	Output	TYPE2	
8	$A2_0$	42	Output	TYPE2	A2–out
7	$A2_1$	41	Output	TYPE2	
6	$A2_2$	39	Output	TYPE2	
5	$A2_3$	38	Output	TYPE2	
4	$A2_4$	36	Output	TYPE2	
3	$A2_5$	35	Output	TYPE2	
2	$A2_6$	33	Output	TYPE2	
1	$A2_7$	32	Output	TYPE2	
0	$A2_8$	30	Output	TYPE2	

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)	±70 mA
DC V_{CC} or Ground Current	
Per Output Pin	±70 mA
Junction Temperature	
SSOP	+140°C
Storage Temperature	−65°C to +150°C
ESD (Min)	2000V

Recommended Operating Conditions

Supply Voltage (V_{CC})	
SCAN Products	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ΔV/Δt	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of SCAN circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	2.0	2.0		or V_{CC} −0.1V
V_{IL}	Maximum LOW	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	0.8	0.8		or V_{CC} −0.1V
V_{OH}	Minimum HIGH	4.5		3.15	3.15	V	I_{OUT} = −50 μA
	Output Voltage	5.5		4.15	4.15		
	(Note 2)	4.5		2.4	2.4	V	V_{IN} = V_{IL} or V_{IH}
		5.5		2.4	2.4		I_{OH} = −32 mA
		4.5		2.4		V	V_{IN} = V_{IL} or V_{IH}
		5.5		2.4			I_{OH} = −24 mA
V_{OL}	Maximum LOW	4.5		0.1	0.1	V	I_{OUT} = 50 μA
	Output Voltage	5.5		0.1	0.1		
	(Note 2)	4.5		0.55	0.55	V	V_{IN} = V_{IL} or V_{IH}
		5.5		0.55	0.55		I_{OL} = 64 mA
		4.5		0.55		V	V_{IN} = V_{IL} or V_{IH}
		5.5		0.55			I_{OL} = 48 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{IN}	Maximum Input Leakage	5.5		2.8	3.6	μA	V_I = V_{CC}
TDI, TMS				−385	−385	μA	V_I = GND
	Minimum Input Leakage	5.5		−160	−160	μA	V_I = GND
I_{OLD}	Minimum Dynamic	5.5		94	94	mA	V_{OLD} = 0.8V Max
I_{OHD}	Output Current (Note 3)			−40	−40	mA	V_{OHD} = 2.0V Min
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OS}	Output Short Circuit Current	5.5		−100	−100	mA (min)	V_O = 0V
I_{CC}	Maximum Quiescent Supply Current	5.5		16.0	88	μA	V_O = HIGH TDI, TMS = V_{CC}
		5.5		750	820	μA	V_O = HIGH TDI, TMS = GND

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units	Conditions
			Typ	Guaranteed Limits			
I_{CCt}	Maximum I_{CC} Per Input	5.5		2.0	2.0	mA	$V_I = V_{CC}-2.1V$
		5.5		2.15	2.15	mA	$V_I = V_{CC}-2.1V$ TDI/TMS Pin, test one with the other floating

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Noise Specifications

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$		$T_A = -40°C$ to $+85°C$	Units
			Typ	Guaranteed Limits		
V_{OLP}	Maximum HIGH Output Noise (Note 5)(Note 6)	5.0	1.0	1.5		V
V_{OLV}	Minimum LOW Output Noise (Note 5)(Note 6)	5.0	–0.6	–1.2		V
V_{OHP}	Maximum Overshoot (Note 4)(Note 6)	5.0	$V_{OH}+1.0$	$V_{OH}+1.5$		V
V_{OHV}	Minimum V_{CC} Droop (Note 4)(Note 6)	5.0	$V_{OH}-1.0$	$V_{OH}-1.8$		V
V_{IHD}	Minimum HIGH Dynamic Input Voltage Level (Note 4)(Note 7)	5.5	1.6	2.0	2.0	V
V_{ILD}	Maximum LOW Dynamic Input Voltage Level (Note 4)(Note 7)	5.5	1.4	0.8	0.8	V

Note 4: Worst case package.

Note 5: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

Note 6: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

Note 7: Maximum number of data inputs (n) switching. (n-1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics

Normal Operation

Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay A to B, B to A	5.0	1.6 1.6		7.9 7.9	1.6 1.6	8.5 8.8	ns
t_{PLZ}, t_{PHZ}	Disable Time	5.0	1.2 1.2		8.6 8.5	1.2 1.2	9.5 9.0	ns
t_{PZL}, t_{PZH}	Enable Time	5.0	1.6 1.6		11.0 8.5	1.6 1.6	12.0 9.5	ns

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V.

Note: All Input Timing Delays involving TCK are measured from the rising edge of TCK.

AC Electrical Characteristics

Scan Test Operation

Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	2.8		13.2	2.8	14.5	ns
			2.8		13.2	2.8	14.5	
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.0		11.5	2.0	11.9	ns
			2.0		11.5	2.0	11.9	
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	2.4		14.5	2.4	15.8	ns
			2.4		14.5	2.4	15.8	
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0		18.0	4.0	19.8	ns
			4.0		18.0	4.0	19.8	
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-IR State	5.0	4.0		18.6	4.0	20.2	ns
			4.0		18.6	4.0	20.2	
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	4.4		19.9	4.4	21.5	ns
			4.4		19.9	4.4	21.5	
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-DR State	5.0	3.2		16.4	3.2	18.2	ns
			3.2		16.4	3.2	18.2	
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-IR State	5.0	2.8		18.0	2.8	19.3	ns
			2.8		18.0	2.8	19.3	
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	2.8		18.4	2.8	20.0	ns
			2.8		18.4	2.8	20.0	
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0		18.9	4.0	20.9	ns
			4.0		18.9	4.0	20.9	
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-IR State	5.0	3.2		19.9	3.2	21.7	ns
			3.2		19.9	3.2	21.7	
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	3.6		21.3	3.6	23.3	ns
			3.6		21.3	3.6	23.3	

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V.

Note: All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note: All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements

Scan Test Operation

Symbol	Parameter	V_{CC} (V) (Note 10)	$T_A = +25°C$, $C_L = 50$ pF Guaranteed Minimum	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Guaranteed Minimum	Units
t_S	Setup Time, H or L Data to TCK (Note 11)	5.0	0.0	0.0	ns
t_H	Hold Time, H or L TCK to Data (Note 11)	5.0	6.5	6.5	ns
t_S	Setup Time, H or L $\overline{G1}$, $\overline{G2}$ to TCK (Note 12)	5.0	0.0	0.0	ns
t_H	Hold Time, H or L TCK to $\overline{G1}$, $\overline{G2}$ (Note 12)	5.0	4.0	4.0	ns
t_S	Setup Time, H or L DIR1, DIR2 to TCK (Note 13)	5.0	0.0	0.0	ns
t_H	Hold Time, H or L TCK to DIR1, DIR2 (Note 13)	5.0	4.0	4.0	ns
t_S	Setup Time, H or L Internal AOE_n, BOE_n to TCK (Note 14)	5.0	1.0	1.0	ns
t_H	Hold Time, H or L TCK to Internal AOE_n, BOE_n (Note 14)	5.0	4.0	4.0	ns
t_S	Setup Time, H or L TMS to TCK	5.0	7.0	7.0	ns
t_H	Hold Time, H or L TCK to TMS	5.0	2.0	2.0	ns
t_S	Setup Time, H or L TDI to TCK	5.0	1.0	1.0	ns
t_H	Hold Time, H or L TCK to TDI	5.0	3.5	3.5	ns
t_W	Pulse Width	5.0			
	H		15.0	15.0	ns
	L		5.0	5.0	
f_{MAX}	Maximum TCK Clock Frequency	5.0	25	25	MHz
T_{PU}	Wait Time, Power Up to TCK	5.0	100	100	ns
T_{DN}	Power Down Delay	0.0	100	100	ms

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V.

Note 11: Timing pertains to the TYPE1 BSR and TYPE2 BSR after the buffer (BSR 0–8, 9–17, 18–26, 27–35, 36–44, 45–53, 54–62, 63–71).

Note 12: Timing pertains to BSR 74 and 78 only.

Note 13: Timing pertains to BSR 75 and 79 only.

Note 14: Timing pertains to BSR 72, 73, 76 and 77 only.

Note: All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Extended AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = 5.0V$ $C_L = 50$ pF 18 Outputs Switching (Note 15)			$T_A = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 0.5V$ $C_L = 250$ pF (Note 16)		Units
		Min	Typ	Max	Min	Max	
t_{PLH},	Propagation Delay	2.5		10.5	3.5	12.0	ns
t_{PHL}	Data to Output	2.5		10.5	3.5	13.5	
t_{PZH},	Output Enable Time	2.5		10.5	(Note 17)		ns
t_{PZL}		2.5		13.5			
t_{PHZ},	Output Disable Time	2.0		9.5	(Note 18)		ns
t_{PLZ}		2.0		10.0			
t_{OSHL} (Note 19)	Pin to Pin Skew HL Data to Output		0.5	1.0		1.0	ns
t_{OSLH} (Note 19)	Pin to Pin Skew LH data to Output		0.5	1.0		1.0	ns

Note 15: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)

Note 16: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 17: 3-STATE delays are load dominated and have been excluded from the datasheet.

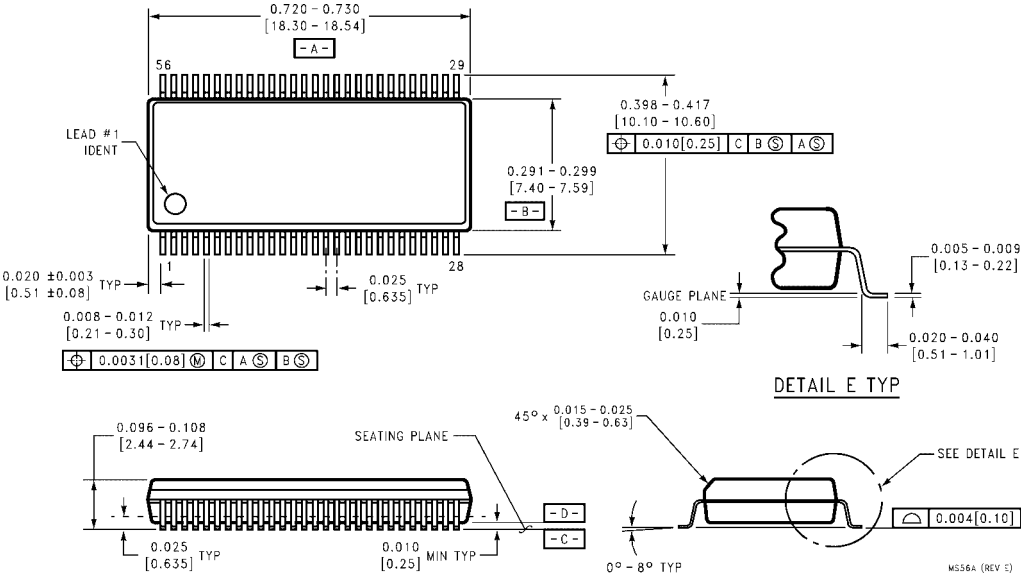
Note 18: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Note 19: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4	pF	$V_{CC} = 5.0V$
$C_{I/O}$	Input/Output Capacitance	20	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	41	pF	$V_{CC} = 5.0V$

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

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