

# ESDL2012

## ESD Protection Diode

### Micro-Packaged Diodes for ESD Protection

The ESDL2012 is designed to protect voltage sensitive components that require low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, the part is well suited for use in high speed data line applications.

#### Features

- Low Capacitance
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.60 mm x 0.30 mm
- Low Body Height: 0.2 mm
- Stand-off Voltage: 1.0 V
- IEC61000-4-2 Level 4 ESD Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- SZESDL2012MX2WT5G – Wettable Flank Package for optimal Automated Optical Inspection (AOI)
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- USB 3.x
- Thunderbolt 3.0

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) Contact Air		$\pm 16$ $\pm 16$	kV
Total Power Dissipation on FR-4 Board (Note 1) @ $T_A = 25^\circ\text{C}$	$P_D$	313	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	400	$^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature – Maximum (10 Second Duration)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-4 = 28 mm<sup>2</sup> 1 oz. Cu JEDEC JESD51-3 two layer PCB.

See Application Note AND8308/D for further description of survivability specs.



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**X4DFN2  
(0201)  
CASE 152AX**

#### MARKING DIAGRAM



K = Specific Device Code  
M = Date Code



**X2DFNW2  
CASE 717AB**



XX = Specific Device Code  
M = Date Code

#### ORDERING INFORMATION

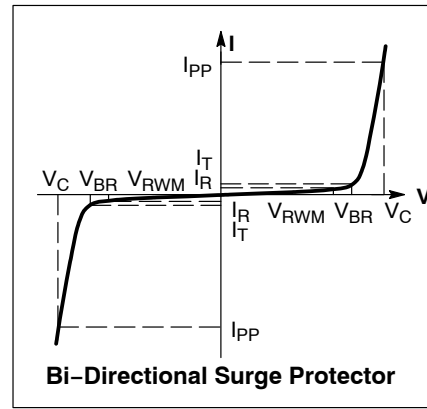
Device	Package	Shipping <sup>†</sup>
ESDL2012MX4T5G	X4DFN2 (Pb-Free)	10000 / Tape & Reel
SZESDL2012MX2WT5G (In Development)	X2DFNW2 (Pb-Free)	8000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS**(T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter
I <sub>PP</sub>	Maximum Reverse Peak Pulse Current
V <sub>C</sub>	Clamping Voltage @ I <sub>PP</sub>
V <sub>RWM</sub>	Working Peak Reverse Voltage
I <sub>R</sub>	Maximum Reverse Leakage Current @ V <sub>RWM</sub>
V <sub>BR</sub>	Breakdown Voltage @ I <sub>T</sub>
I <sub>T</sub>	Test Current

\*See Application Note AND8308/D for detailed explanations of datasheet parameters.

**ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V <sub>RWM</sub>	I/O Pin to GND			1.0	V
Breakdown Voltage	V <sub>BR</sub>	I <sub>T</sub> = 1 mA, I/O Pin to GND	1.4	1.6	2.1	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 1.0 V		30	500	nA
Clamping Voltage (Note 2)	V <sub>C</sub>	IEC61000-4-2, ±8 kV Contact	Figures 1 and 2			V
Clamping Voltage, 200 ns TLP, IEC61000-4-2 Level 1 Equivalent (±2 kV Contact, ±4 kV Air)	V <sub>C</sub>	I <sub>PP</sub> = 4 A		3.5	4.0	V
		I <sub>PP</sub> = 4 A (SZESDL2012)			5.0	
		I <sub>PP</sub> = 8 A		4.7	5.2	
		I <sub>PP</sub> = 8 A (SZESDL2012)			7.5	
Reverse Peak Pulse Current per Figure 12	I <sub>PP</sub>	per IEC61000-4-5 (1.2/50 μs), R <sub>eq</sub> = 12 Ω	3.5	4.7		A
Clamping Voltage, IEC61000-4-5 (1.2/50 μs) Waveform per Figure 12	V <sub>C</sub>	I <sub>PP</sub> = 2.1 A, R <sub>eq</sub> = 12 Ω		3.1	3.4	V
		I <sub>PP</sub> = 2.1 A, R <sub>eq</sub> = 12 Ω (SZESDL2012)			4.5	
Clamping Voltage, IEC61000-4-5 (1.2/50 μs) Waveform per Figure 12	V <sub>C</sub>	I <sub>PP</sub> = 3.5 A, R <sub>eq</sub> = 12 Ω		3.7	4.1	V
		I <sub>PP</sub> = 3.5 A, R <sub>eq</sub> = 12 Ω (SZESDL2012)			5.5	
Dynamic Resistance (200 ns TLP, 4 A to 8 A)	R <sub>DYN</sub>	I/O Pin to GND I/O Pin to GND (SZESDL2012)		0.30 0.65		Ω
Junction Capacitance	C <sub>J</sub>	V <sub>R</sub> = 0 V, f = 1 MHz V <sub>R</sub> = 0 V, f = 1 MHz (SZESDL2012)		0.18 0.25	0.23 0.35	pF
Insertion Loss	I <sub>L</sub>	f = 10 GHz f = 13 GHz f = 15 GHz		0.26 0.27 0.28	0.33 0.36 0.37	dB
Return Loss	R <sub>L</sub>	f = 10 GHz f = 13 GHz f = 15 GHz	14 12 11	16 14 13		dB

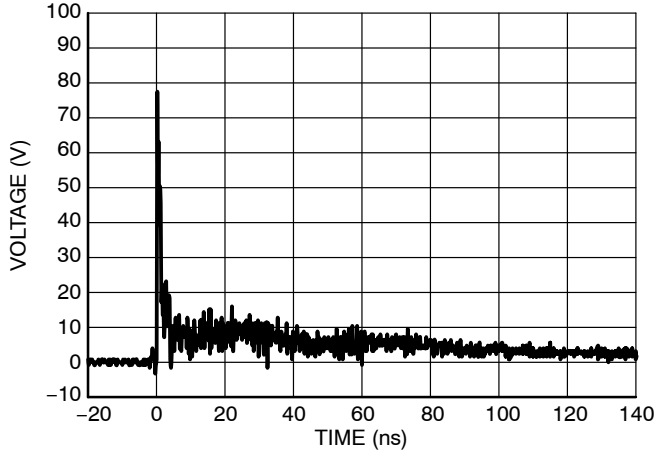
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. For test procedure see application note AND8307/D.

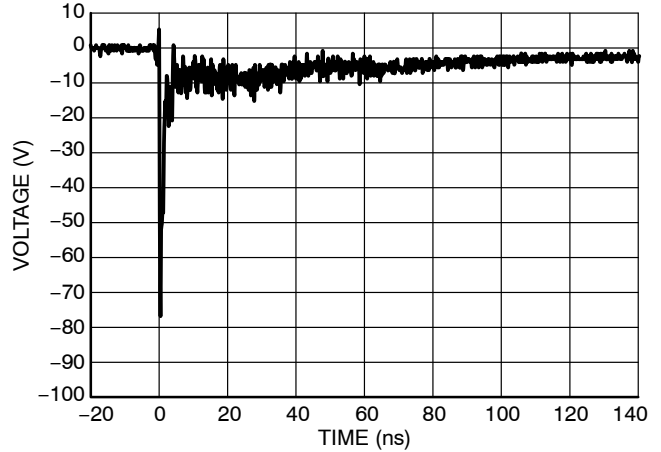
3. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.

TLP conditions: Z<sub>0</sub> = 50 Ω, t<sub>p</sub> = 200 ns, t<sub>r</sub> = 1 ns, averaging window; t<sub>1</sub> = 170 ns to t<sub>2</sub> = 190 ns.

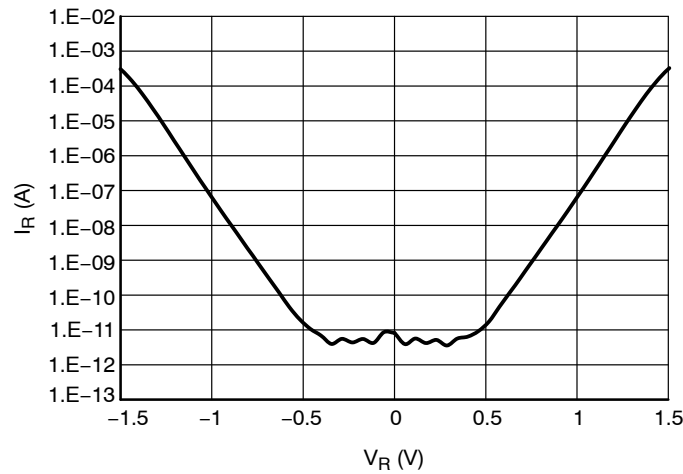
TYPICAL CHARACTERISTICS



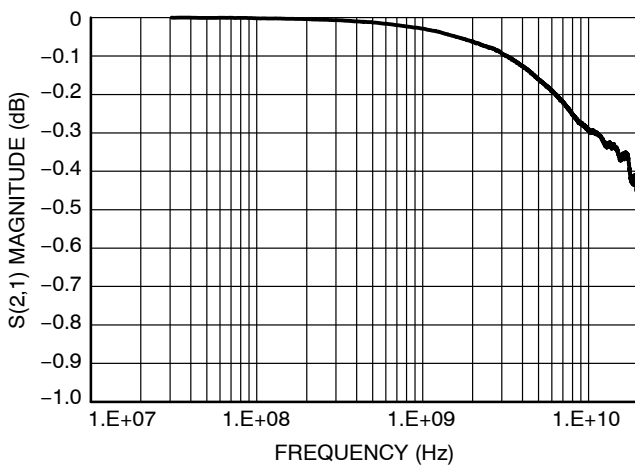
**Figure 1. ESD Clamping Voltage**  
Positive 8 kV Contact per IEC61000-4-2



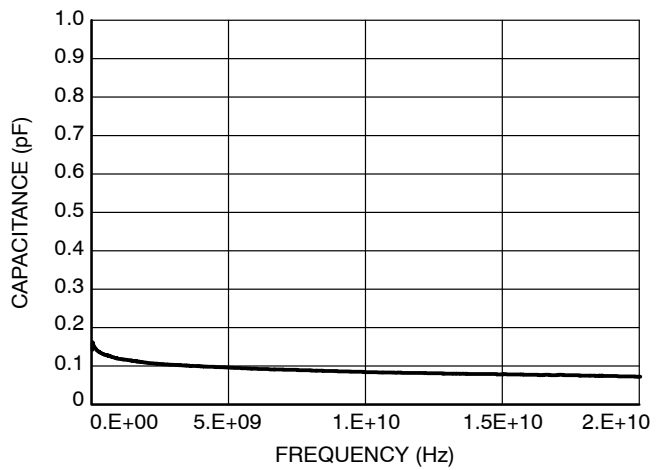
**Figure 2. ESD Clamping Voltage**  
Negative 8 kV Contact per IEC61000-4-2



**Figure 3. IV Characteristics**



**Figure 4. Insertion Loss**



**Figure 5. Capacitance Over Frequency**

TYPICAL CHARACTERISTICS

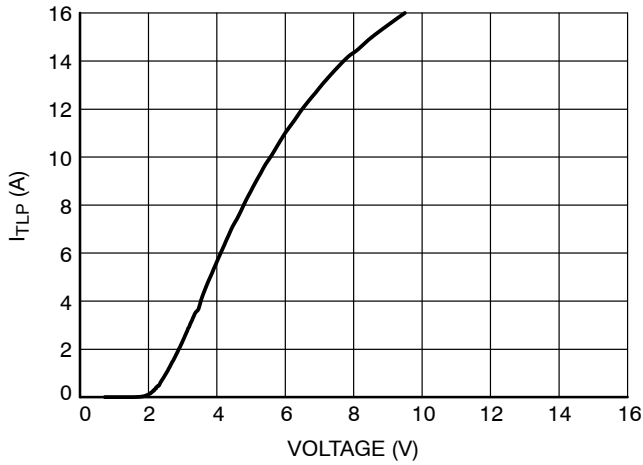


Figure 6. Positive 200 ns TLP IV Curve

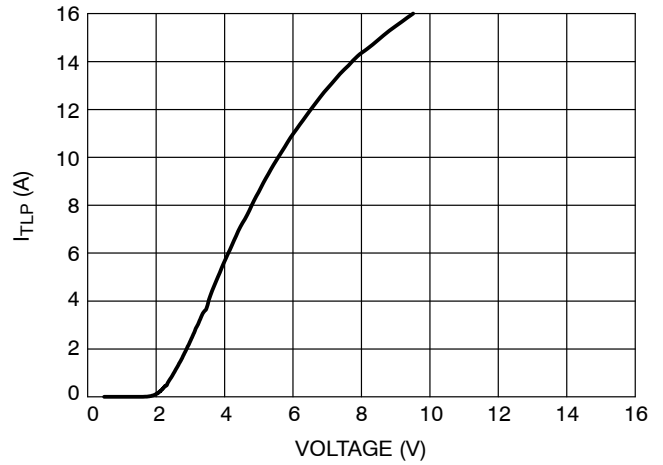


Figure 7. Negative 200 ns TLP IV Curve

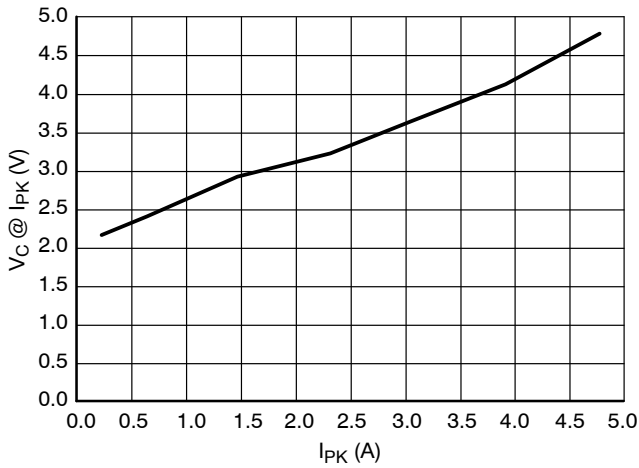


Figure 8. Positive Clamping Voltage vs. Peak Pulse Current (per IEC61000-4-5 ( $t_p = 1.2/50 \mu s$ ,  $R_{eq} = 12 \Omega$ ))

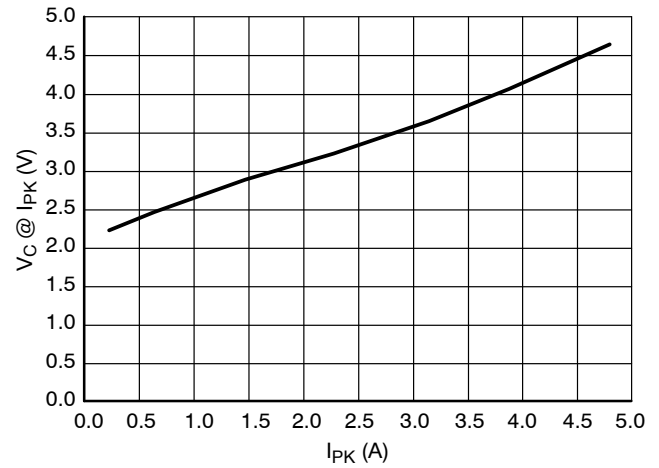


Figure 9. Negative Clamping Voltage vs. Peak Pulse Current (per IEC61000-4-5 ( $t_p = 1.2/50 \mu s$ ,  $R_{eq} = 12 \Omega$ ))

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

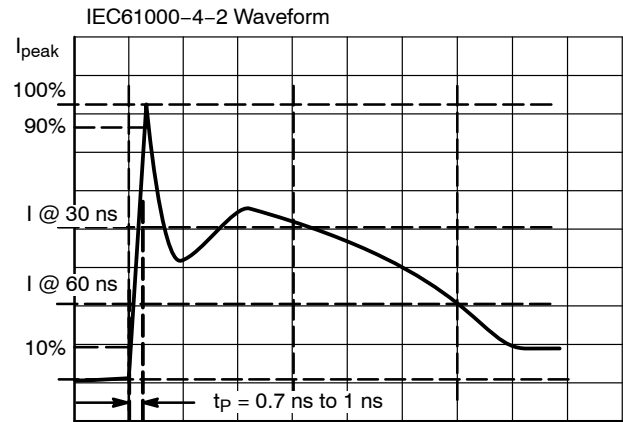


Figure 10. IEC61000-4-2 Spec

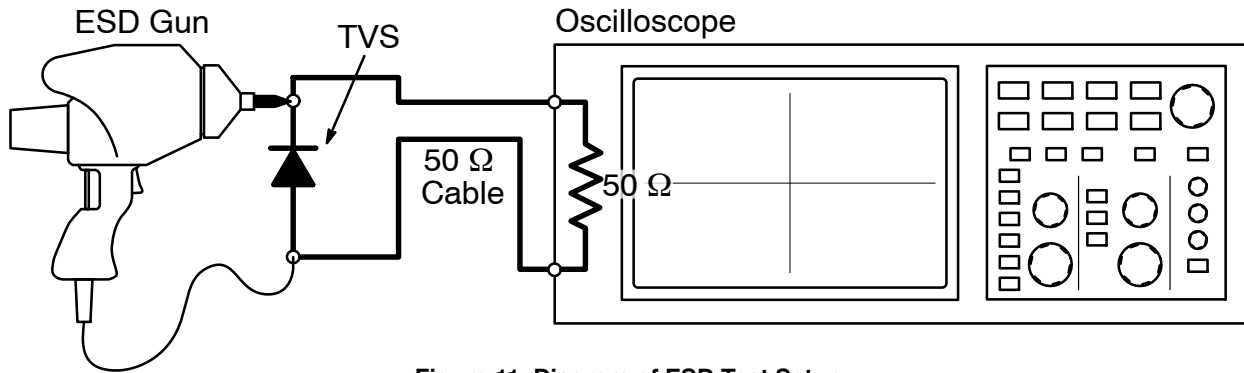


Figure 11. Diagram of ESD Test Setup

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage

at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

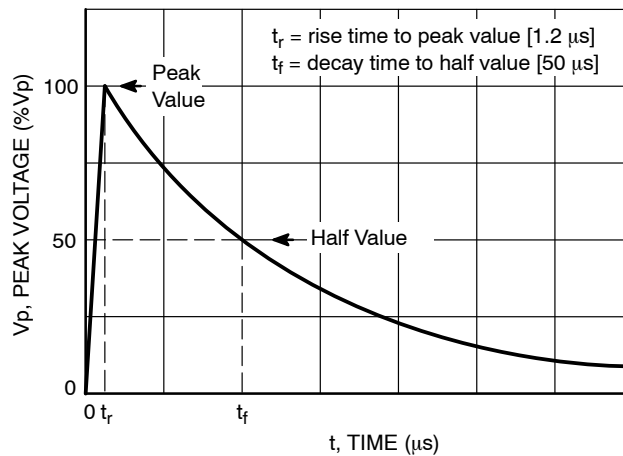
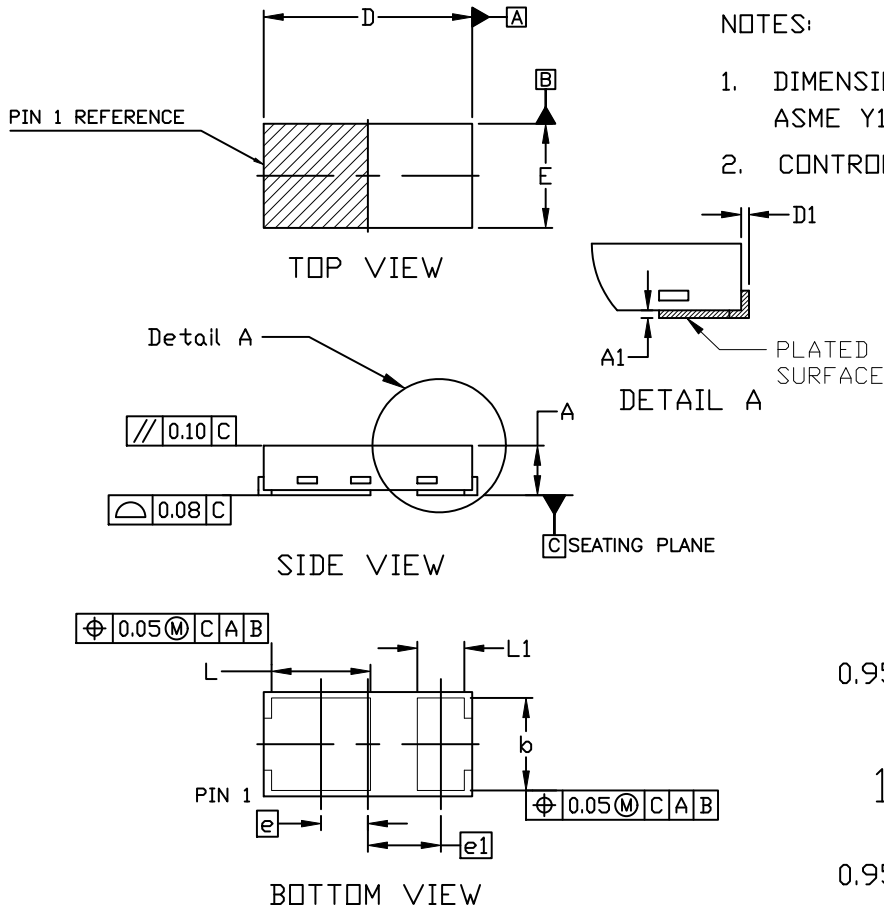


Figure 12. IEC61000-4-5 1.2/50  $\mu$ s Pulse Waveform



## PACKAGE DIMENSIONS

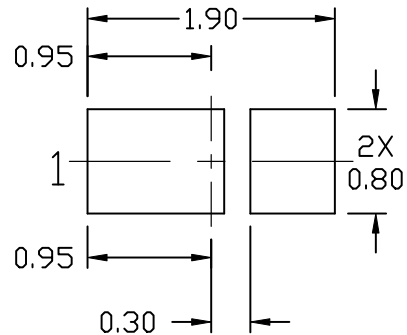
**X2DFNW2 1.60x0.80**  
CASE 717AB  
ISSUE B



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
A1	---	---	0.04
b	0.67	0.71	0.75
D	1.55	1.60	1.65
D1	---	---	0.04
E	0.75	0.80	0.85
e	0.36 BSC		
e1	0.56 BSC		
L	0.72	0.76	0.80
L1	0.32	0.36	0.40



**RECOMMENDED  
MOUNTING FOOTPRINT\***

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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