FAN108M6X

Offline Primary-Side-Regulation (PSR) Quasi-Resonant Valley Switch Controller

FAN108 is offline Primary−Side−Regulation (PSR) PWM controller with Quasi−Resonant (QR) mode controller to achieved constant−voltage (CV) and constant−current (CC) control for Travel Adaptor (TA) requirement and provide cost−effective, simplified circuit for energy−efficient power supplies.

FAN108 is designed to have good energy efficiency technology that offers options to users to meet different power consumption targets using different startup components.

FAN108 can be used in Travel Adapter design by stand−alone or co−work with secondary−side SR controller FAN6250/FAN6251. While pairing with FAN6292C, FAN108 can be used to design a high density Type−C travel adapter in compact system BOM.

Features

- Ultra−Low Standby Power Consumption Feasible: < 30 mW through HV FET and < 75 mW through HV Resistor
- Constant−Current (CC) and Constant−Voltage(CV) with Primary − Side Regulation Eliminates Secondary−Side Feedback Component
- Valley Switch Operation for Highest Average Efficiency
- Dynamic Response Enhancement (DRE) Function for Excellent Dynamic Response without the Need of OPTO
- Low EMI Emissions and Common Mode Noise
- Programmable Brown−In and Brown−Out Protection
- Output Over−Voltage Protection (OVP)
- Output Under−Voltage Protection (UVP)
- Capture Secondary Side Shut−Down Signal from the Proprietary Channel between FAN108 and FAN6250 to Perform Real System Protection
- Secondary Side Rectifier Short Detection via Current Sense Protection(CSP)
- Cycle−by−Cycle Current Limiting

Typical Applications

- Travel Adapter for Smart Phones, Feature Phones, and Tablet PCs
- AC−DC Adapters for Portable Devices or Battery Chargers that Require CV/CC Control

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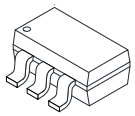
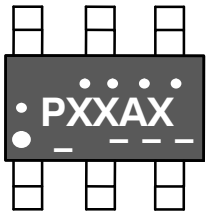


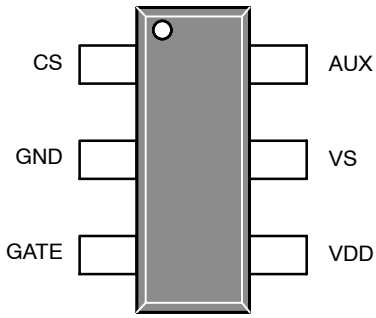
SOT23
CASE 527AJ

MARKING DIAGRAM



....	= Year Code
PXX	= 108 : FAN108M6X
AX	= Die Run Code
___	= Week Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

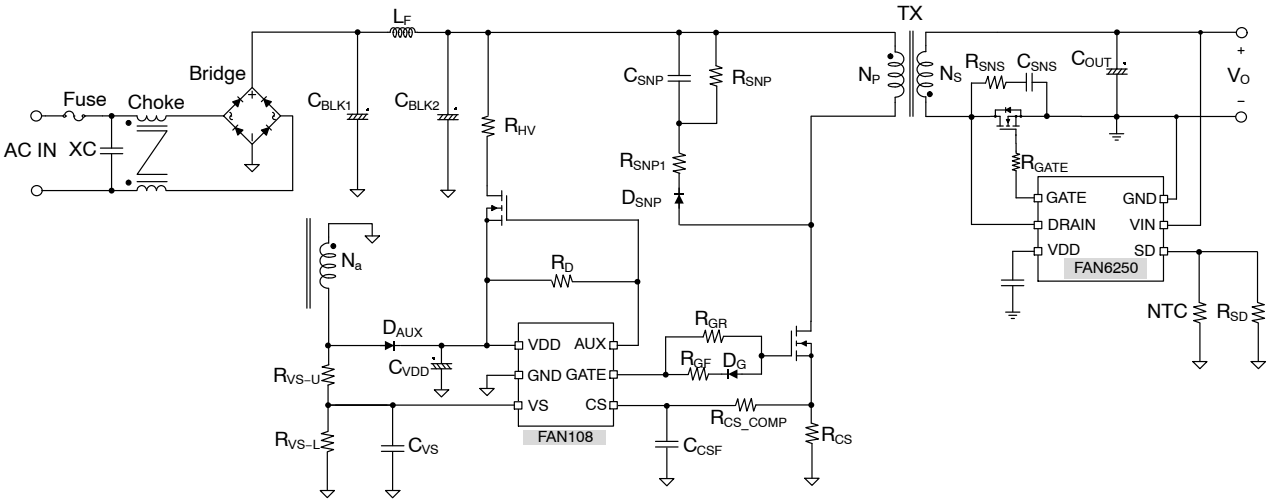


Figure 1. FAN108 Typical Application Schematic

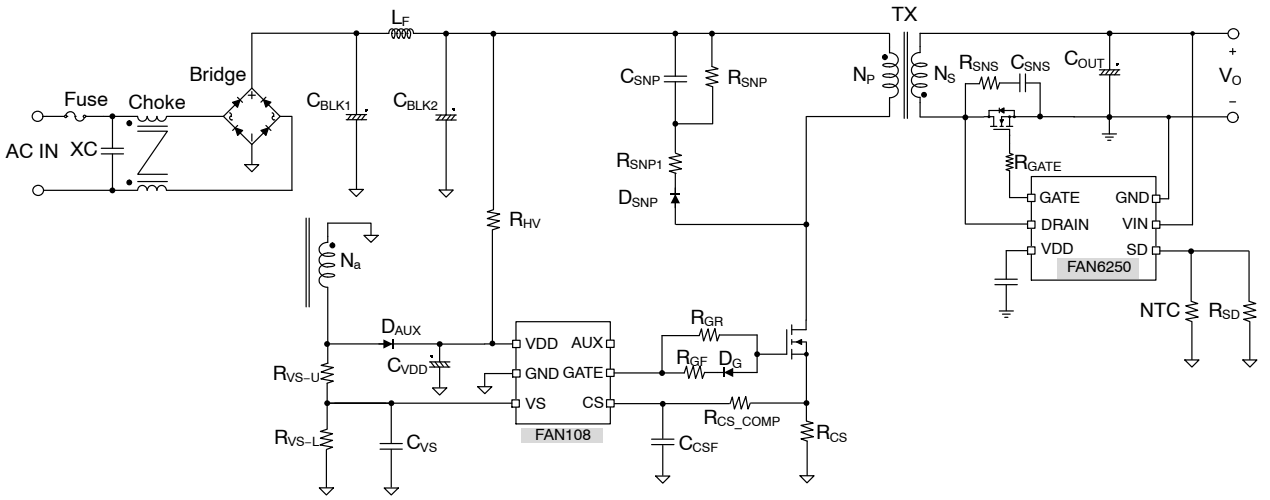


Figure 2. FAN108 Typical Application Schematic

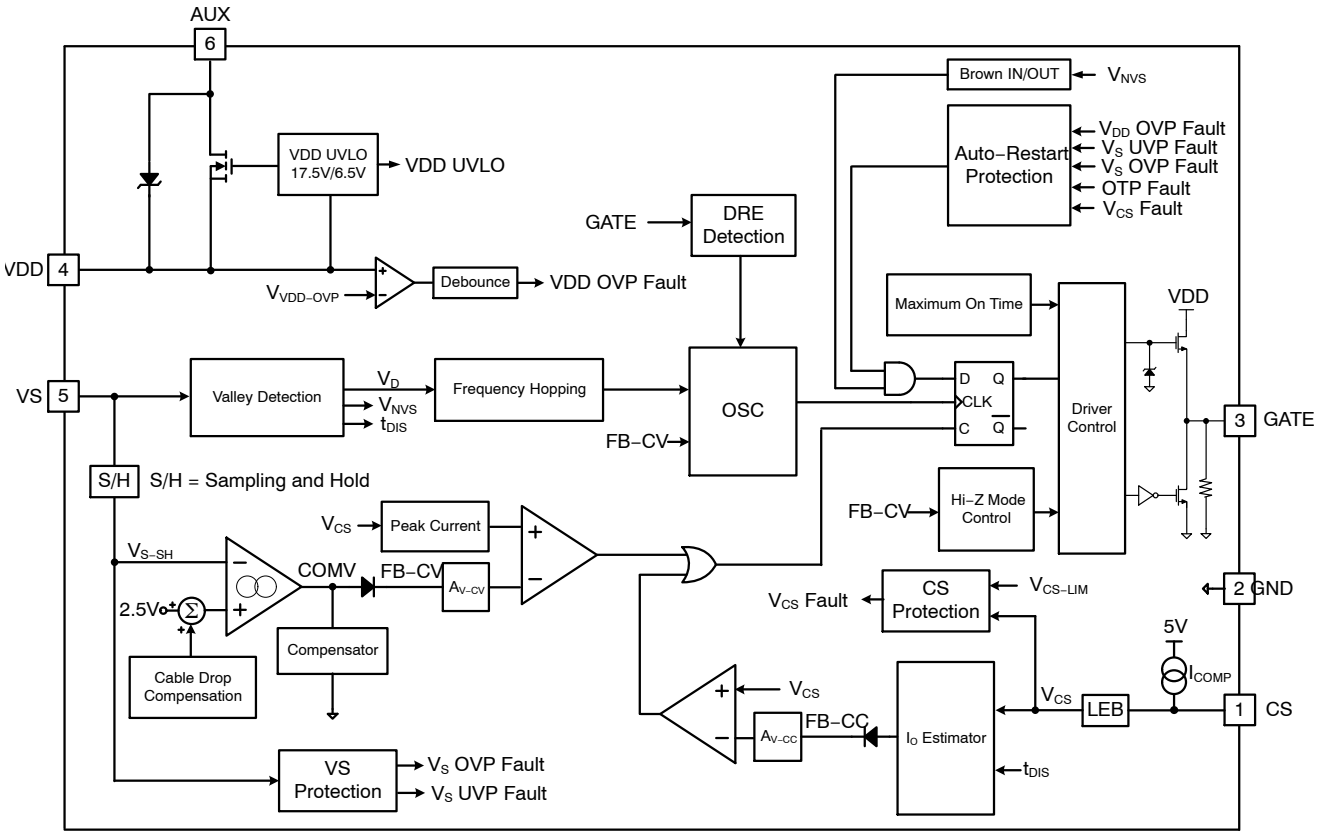


Figure 3. FAN108 Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Name	Description
1	CS	**Current Sense.** This pin connects to a current−sense resistor to detect the MOSFET current for Peak−Current−Mode control for output regulation. The current−sense information is also used to estimate the output current for CC regulation
2	GND	**Ground.**
3	GATE	**PWM Signal Output.** This pin has an internal totem−pole output driver to drive the power MOS-FET. The gate driving voltage is internally clamped at 7.5 V
4	VDD	**Power Supply.** IC operating current and MOSFET driving current are supplied through this pin. This pin is typically connected to an external VDD capacitor
5	VS	**Voltage Sense.** The VS voltage is used to detect resonant valleys for quasi−resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage. It also senses input voltage for Brown−IN/OUT protection
6	AUX	**Auxiliary Function.** The pin is used for startup with external depletion HV FET

MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
DC Supply Voltage		V_{VDD}	30	V
Maximum Voltage on GATE Pin		V_{GETE}	−0.3 to 30	V
Maximum Voltage on Low Power Pins (Except Pin 3, Pin 4, Pin 6)		V_{max}	−0.3 to 6	V
Power Dissipation (T_A = 25°C)		P_D	467.4	mW
Thermal Resistance (Junction−to−Ambient)		θ_{JA}	218.5	C/W
Thermal Resistance (Junction−to−Top)		θ_{JT}	33.1	°C/W
Operating Junction Temperature		T_J	−40 to +125	°C
Storage Temperature Range		T_{STG}	−40 to +125	°C
Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22_A114	ESD	1.5	kV
	Charged Device Model, JEDEC:JESD22_C101		0.5	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS−001−2012 and JESD 22−C101.

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
VDD Pin Supply Voltage	V_{VDD}	6	25	V
VS Pin Supply Voltage	V_{VS}	0.65	3.0	V
CS Pin Supply Voltage	V_{CS}	0	0.8	V
AUX Pin Supply Voltage	V_{AUX}	0	V_{DD} − 5V	V
Operating Temperature	T_A	−40	+85	°C

4. The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. ON Semiconductor does not recommend exceeding them or designing to Maximum Ratings.

ELECTRICAL CHARACTERISTICS

For typical values T_J = 25°C, for min/max values T_J = −40°C to 125°C, V_{DD} = 12 V; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VDD SECTION						
Turn−On Threshold Voltage	V_{DD} Rising	V_{DD-ON}	16.5	17.5	18.5	V
Turn−Off Threshold Voltage	V_{DD} Falling	V_{DD-OFF}	6.1	6.5	6.9	V
Startup Current	V_{DD} = V_{DD-ON}−0.16 V	I_{DD-ST}	−		20	μA
Operating Supply Current		I_{DD-OP}	−	1.2		mA
Deep Green−Mode Operating Supply Current		$I_{DD-DPGN}$	−	−	460	μA
V_{DD} Over−Voltage−Protection Level		$V_{VDD-OVP}$	26.5	28.0	29.5	V
V_{DD} Over−Voltage−Protection Debounce Time		$t_{D-VDDOVP}$	−	120	200	μs
OSCILLATOR SECTION						
Maximum Blanking Frequency		$f_{BNK-MAX}$	70	77	83	kHz
Minimum Blanking Frequency		$f_{BNK-MIN}$	24	27	30	kHz
Maximum DCM Operation Frequency		$f_{OSC-DCM-MAX}$	22	25	28	kHz

ELECTRICAL CHARACTERISTICS

For typical values T_J = 25°C, for min/max values T_J = −40°C to 125°C, V_{DD} = 12 V; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION						
Minimum DCM Operation Frequency		$f_{OSC-DCM-MIN}$	0.080	0.105	0.130	kHz
Minimum Frequency for CCM Prevention		$f_{OSC-CCM}$	18	21	24	kHz
Frequency Hopping Range		$\Delta f_{Hopping}$	3	4	5	kHz
Frequency Hopping Period		$\Delta t_{Hopping}$	1.8	2.5	3.2	ms
AUX SECTION						
Clamping Voltage between VDD and AUX pin	$V_{DD} = V_{DD-ON}$	ΔV_{CLAMP}	–	5	–	V
CURRENT−SENSE SECTION						
Current Limit Threshold Voltage		V_{CS-LIM}	0.67	0.70	0.73	V
High Threshold Voltage of Current Sense		$V_{CS-IMIN}$	0.15	0.175	0.20	V
GATE Output Turn−Off Delay (Note 5)		t_{PD}	–	100	–	ns
Leading−Edge Blanking Time		t_{LEB}	170	220	270	ns
CONSTANT CURRENT ESTIMATOR SECTION						
Reference Voltage of Constant Current		V_{VR-CC}	1.19	1.2	1.21	V
Peak Value Amplifying Gain (Note 5)		A_{PK}		3.6		V/V
CONSTANT CURRENT CORRECTION SECTION						
High Line Compensation Current	V_{IN} = 264 V_{rms}	I_{COMP-H}	71	75	79	μA
Low Line Compensation Current	V_{IN} = 90 V_{rms}	I_{COMP-L}	23.5	25.5	27.5	μA
Internal Line Voltage Compensation Resistance (Note 5)		$R_{COMP-LINE}$		575		Ω
CABLE DROP COMPENSATION SECTION						
Cable Drop Compensation Voltage		ΔV_{CDC}	147	160	173	mV
OVER−TEMPERATURE PROTECTION SECTION						
Threshold Temperature for Over−Temperature−Protection (Note 5)		T_{OTP-H}	–	130	–	°C
Threshold Temperature for Over−Temperature−Protection (Note 5)		T_{OTP-L}	–	110	–	°C
VOLTAGE−SENSE SECTION						
Reference Voltage of Constant Voltage		V_{VR-CV}	2.475	2.500	2.525	V
VS Sampling Blanking Time L	T_J = 25°C	$t_{VS-BNK-L}$	1.1	1.3	1.5	μs
VS Sampling Blanking Time H	T_J = 25°C	$t_{VS-BNK-H}$	1.5	1.8	2.1	μs
VS Source Current Threshold to Enable Brown−OUT	Set V_{IN} = 264 VAC (373 VDC) N_P:N_S:N_A = 54:8:4, R_{VS-U} = 27.4 kΩ	$I_{VS-Brown-OUT}$	270	320	370	μA
Brown−OUT Debounce Time		$t_{D-Brown-OUT}$	12	17	22	ms
VS Source Current Threshold to Enable Brown−IN	Set V_{IN} = 264 VAC (373 VDC) N_P:N_S:N_A=54:8:4, R_{VS-U} = 27.4 kΩ	$I_{VS-Brown-IN}$	395	465	535	μA
Brown−IN Debounce Time		$N_{Brown-IN}$	–	4	–	Pulse
Output Over−Voltage−Protection with Vs Sampling Voltage		V_{VS-OVP}	2.85	2.95	3.05	V
Output Over−Voltage−Protection Debounce Pulse Counts		N_{VS-OVP}	–	4	–	Pulse
Output Under−Voltage−Protection with Vs Sampling Voltage		$V_{VS-UVP-L}$	1.50	1.60	1.70	V

ELECTRICAL CHARACTERISTICS

For typical values T_J = 25°C, for min/max values T_J = −40°C to 125°C, V_{DD} = 12 V; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VOLTAGE−SENSE SECTION						
Output Under−Voltage−Protection Debounce Pulse Counts		N_{VS-UVP}	−	4	−	Pulse
Output Under−Voltage Protection Blanking Time at start−up		$t_{VS-UVP-BLANK}$	30	40	50	ms
DYNAMIC RESPONSE ENHANCEMENT						
Dynamic Event Enable Threshold Voltage	T_J = 25°C	$V_{VS-EAV-DYN-EN}$	2.413	2.45	2.488	V
Dynamic Event Disable Threshold Voltage		$V_{VS-EAV-DYN-DIS}$		2.475		V
Hi−Z Mode Enable Time		t_{HIZ-EN}	54	67	91	μs
Hi−Z Mode Clamping Voltage		$V_{CLMP-HIZ}$	1.0	1.4	1.8	V
GATE SECTION						
Gate Output Voltage Low		V_{GATE-L}	0	−	1.5	V
Internal Gate PMOS Driver ON		$V_{DD-PMOS-ON}$	7.0	7.5	8.0	V
Internal Gate PMOS Driver OFF		$V_{DD-PMOS-OFF}$	9.0	9.5	10.0	V
Rising Time		t_r	100	140	180	ns
Falling Time		t_f	30	50	70	ns
Gate Output Clamping Voltage		$V_{GATE-CLAMP}$	7.0	7.5	8.0	V
Maximum On Time		t_{ON-MAX}	15	−	22	μs

5. Design guaranteed.

TYPICAL CHARACTERISTICS

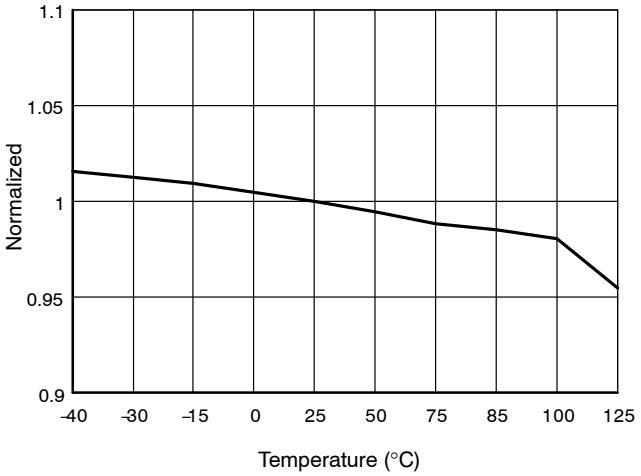


Figure 4. Turn−On Threshold Voltage (V_{DD-ON}) vs. Temperature

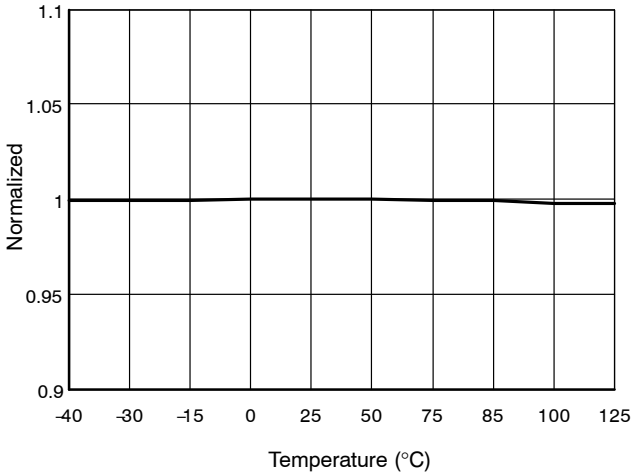


Figure 5. Turn−Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

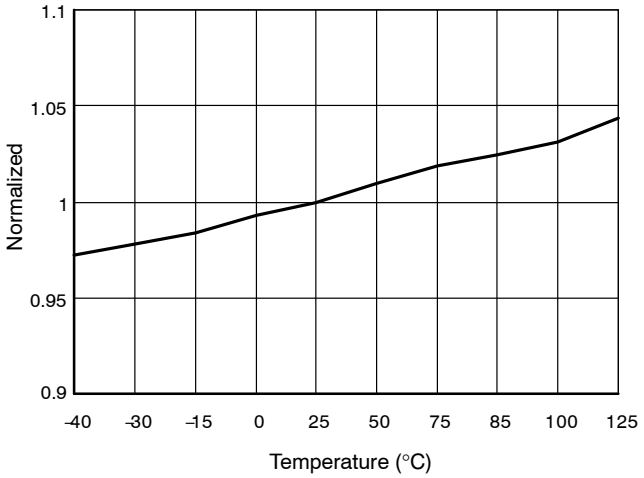


Figure 6. VS Source Current Threshold to Enabled Brown−IN ($I_{VS-Brown-IN}$) vs. Temperature

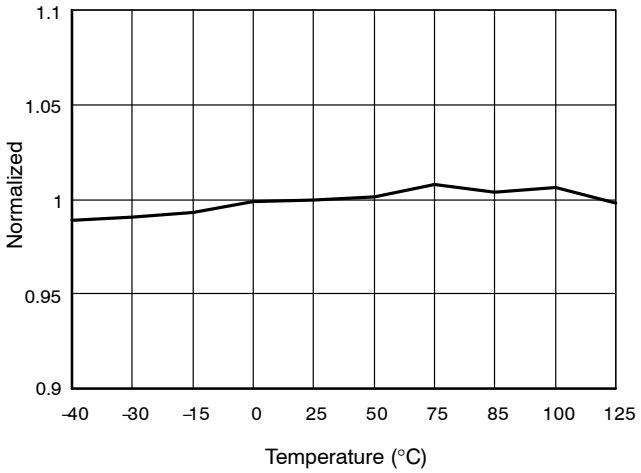


Figure 7. VS Source Current Threshold to Enabled Brown−OUT ($I_{VS-Brown-OUT}$) vs. Temperature

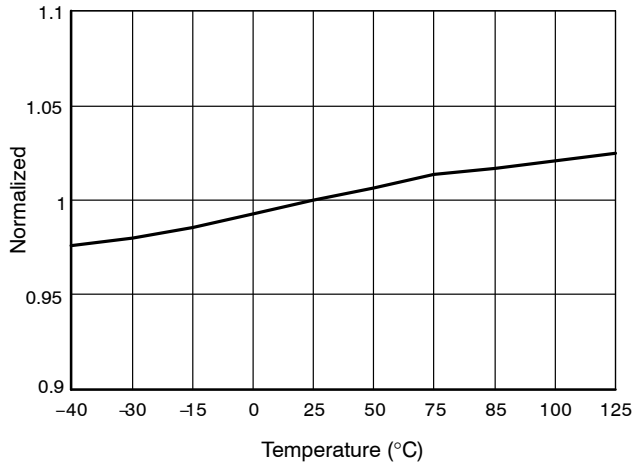


Figure 8. Maximum Blanking Frequency ($f_{BNK-MAX}$) vs. Temperature

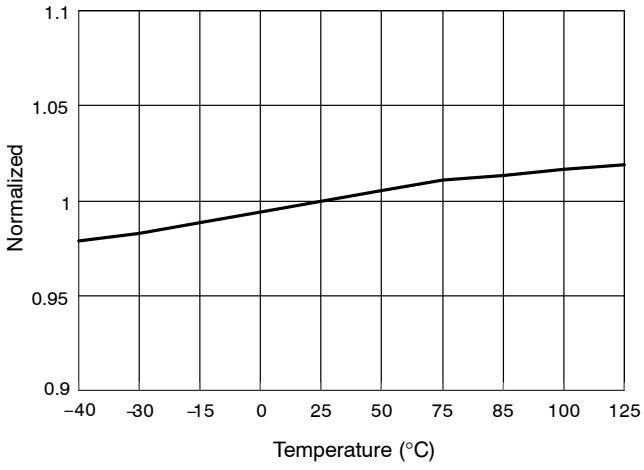


Figure 9. Minimum Blanking Frequency ($f_{BNK-MIN}$) vs. Temperature

TYPICAL CHARACTERISTICS (continued)

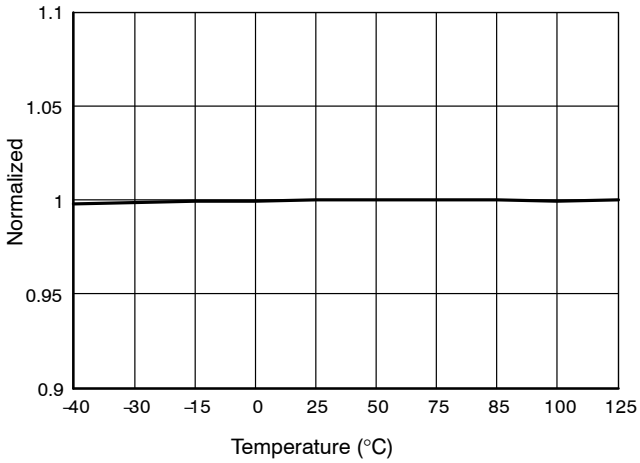


Figure 10. Reference Voltage of Constant Voltage (V_{VR-CV}) vs. Temperature

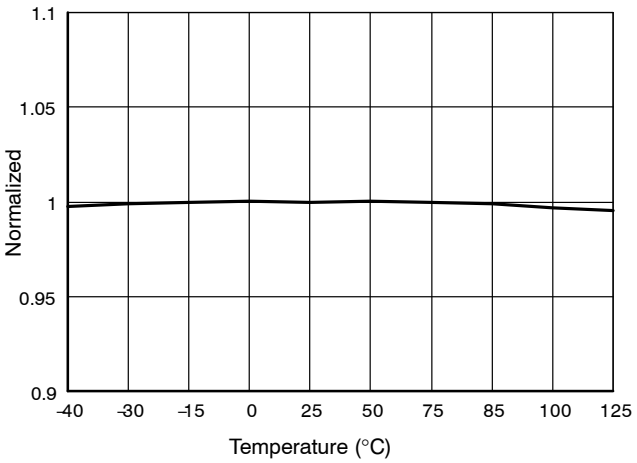


Figure 11. Reference Voltage of Constant Current (V_{VR-CC}) vs. Temperature

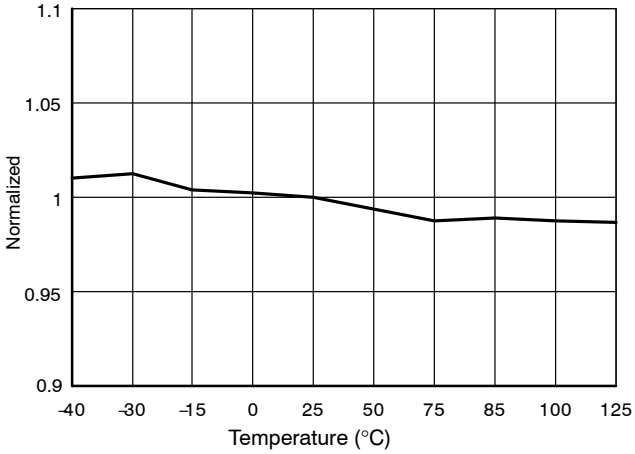


Figure 12. VS Sampling Blanking Time L ($t_{VS-BNK-L}$) vs. Temperature

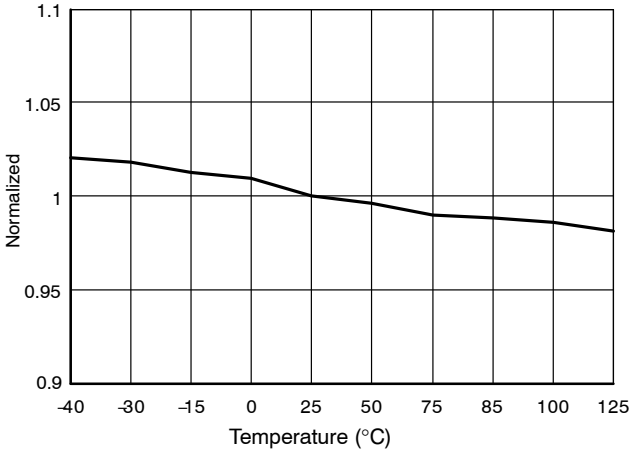


Figure 13. Figure 14 VS Sampling Blanking Time H ($t_{VS-BNK-H}$) vs. Temperature

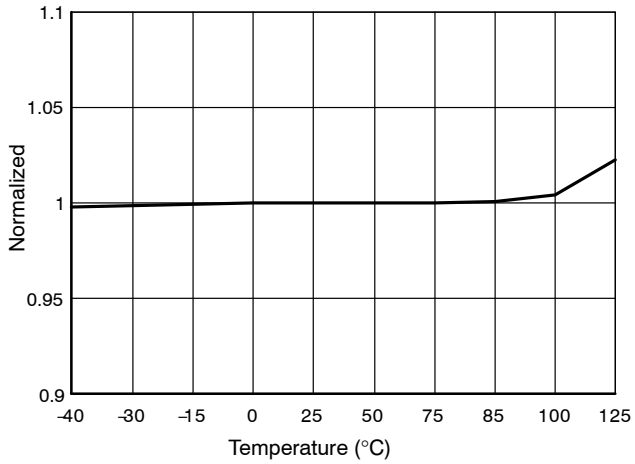


Figure 15. Output Over−Voltage-Protection (V_{VS-OVP}) vs. Temperature

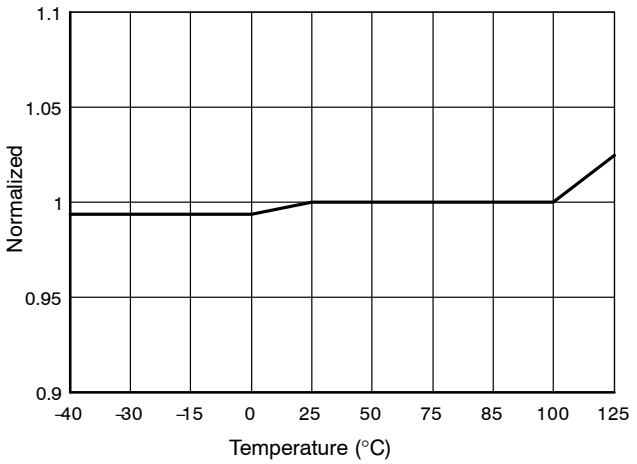


Figure 16. Output Under-Voltage Protection (V_{VS-UVP}) vs. Temperature

TYPICAL CHARACTERISTICS (continued)

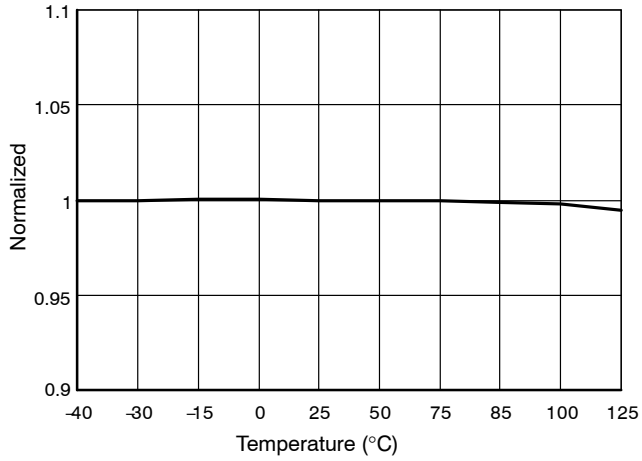


Figure 17. Current Limit Threshold Voltage (V_{CS-LIM}) vs. Temperature

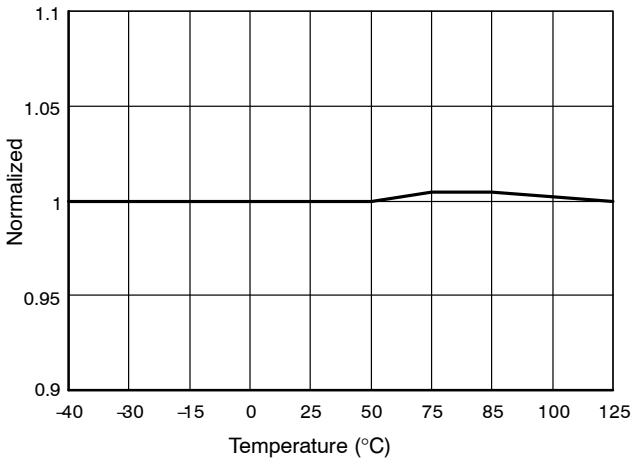


Figure 18. Figure 19 High Threshold Voltage of Current Sense ($V_{CS-IMIN}$) vs. Temperature

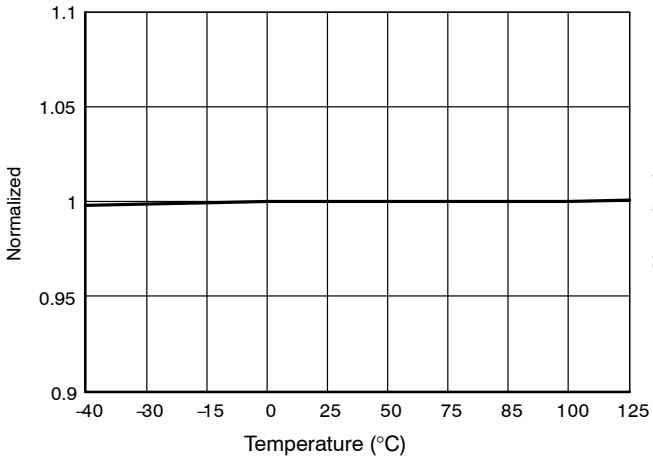


Figure 20. V_{DD} Over−Voltage Protection Level ($V_{VDD-OVP}$) vs. Temperature

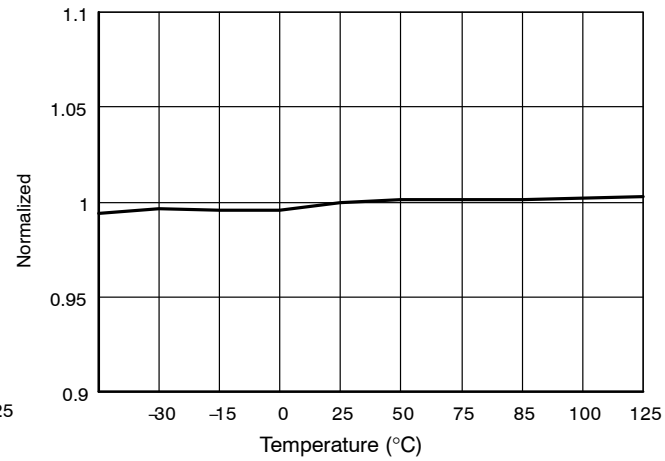


Figure 21. Cable Drop Compensation Voltage (ΔV_{CDC}) vs. Temperature

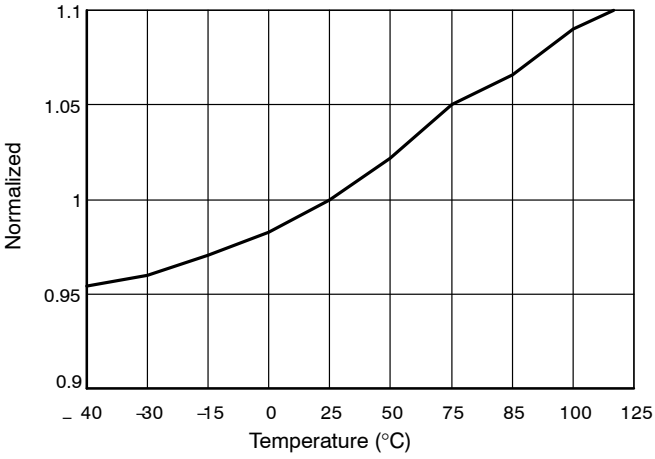


Figure 22. Leading−Edge Blanking Time (t_{LEB}) vs. Temperature

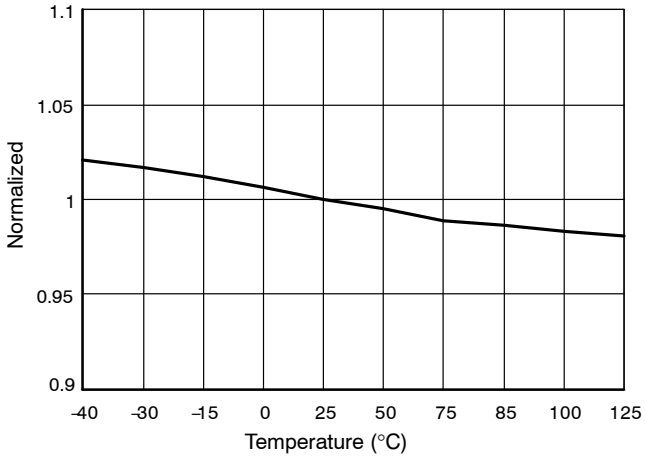


Figure 23. Maximum On Time (t_{ON-MAX}) vs. Temperature

APPLICATIONS INFORMATION

FAN108 is a flyback power supply controller providing a means to implement primary side constant−voltage (CV) and constant−current (CC) regulation. This technique can simplify feedback circuit and secondary side circuit compare to traditional flyback converter. FAN108 implements a current−mode architecture operation in quasi−resonant mode. The quasi−resonant mode operation is able to minimize the switching loss to optimize the power supply efficiency and get better EMI performance.

FAN108 quasi−resonance operation in peak current mode control is monitor the auxiliary winding voltage on primary side via the resistor divider to voltage sense pin (VS) and current sense pin (CS). Extremely accurately constant voltage (CV) mode and constant current (CC) mode could meet strict requirement from market.

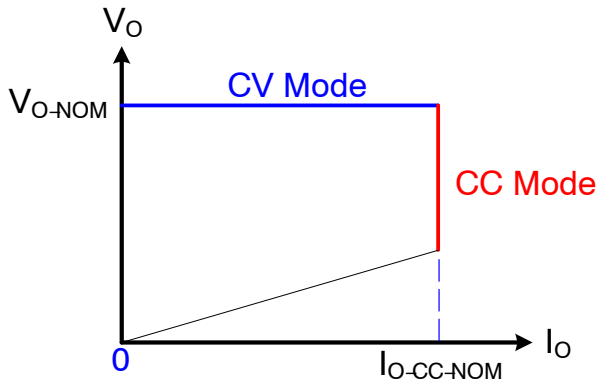


Figure 24. CV and CC Mode

FAN108 implements deep green mode (DPGN) with lowest switching frequency, limits IC current consumption (460 μA) for excellent system standby power performance. Furthermore, the system design allows two kinds of startup circuit one is with startup resistor the other is with high voltage FET.

Protections such as over−voltage protection (VS−OVP), under−voltage protection (VS−UVP), internal over−temperature protection (OTP), brown−in and brown−out protection, cycle by cycle current limit, current sense resistor short protection and secondary rectifier short protection.

Startup Operation

FAN108 supports high voltage start up with depletion FET that can make better standby power and shorter start up time. Figure 23 shows startup sequence with AUX controlling. The initial AUX pin status should be defined by resistor of R_D. At system power on moment, the initial V_{DD} voltage is zero, internal switch S1 is turn−on and external depletion FET also is turn−on, the C_{VDD} is charged through depletion FET till V_{DD} reach V_{DD-ON}. While internal switch S1is turn−off and V_{GS} of depletion FET will close to internal clamping voltage (V_{CLAMP}) which less than depletion FET V_{GS} turn−on threshold. Meanwhile V_{DD} energy supplement is turn to auxiliary winding. The voltage gap between V_{DD} and V_{AUX} is kept at ΔV_{CLAMP} till controller shut−down by protection or V_{DD} touching V_{DD-OFF}.

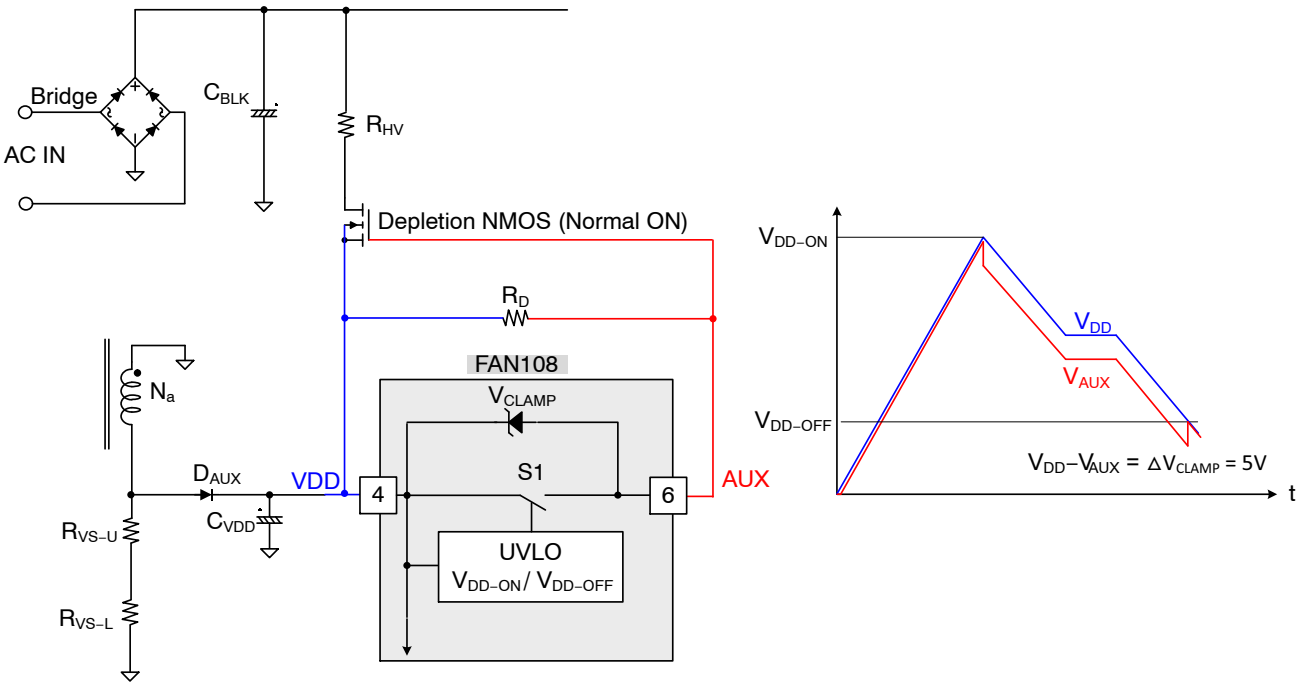


Figure 25. Startup Sequence with AUX Controlling

Primary Side Regulation: Constant Voltage Operation

As illustrated by Figure 26, the voltage of auxiliary winding (V_{WAUX}) is reflected to output voltage scaled by the auxiliary and secondary turns ratio minus the drain voltage of synchronous rectifier (SR) FET.

To reach an accurate primary−side constant−voltage regulation, the controller detects the end of the demagnetization time and precisely sample output voltage level seen on the auxiliary winding.

Therefore, when the secondary current I_{SEC} reaches zero ampere, the voltage of auxiliary winding is sensed as

$$V_{WAUX} = V_O \times \frac{N_a}{N_s} \qquad \text{(eq. 1)}$$

where N_a and N_S are respectively the turns of secondary and auxiliary.

Figure 27 shows how the constant voltage feedback has been built. The auxiliary winding voltage must be scaled down via the resistor divider to V_{VR-CV} level before building the constant voltage feedback error.

$$V_{VR-CV} = \frac{R_{VS-L}}{R_{VS-U} + R_{VS-L}} \times V_{WAUX} \qquad \text{(eq. 2)}$$

By inserting Equation 1 into Equation 2 we obtain the following equation:

$$V_{VR-CV} = \frac{R_{VS-L}}{R_{VS-U} + R_{VS-L}} \times V_O \times \frac{N_a}{N_s} \qquad \text{(eq. 3)}$$

A VS blanking time (t_{VS-BNK}) start from primary switch turned off. Most of TA design has VS oscillation after primary switch turned off that is caused by the resonance of leakage inductance and parasitic capacitance at transformer. In order to avoid VS sampling procedure get impacted by that ringing, after t_{VS-BNK} the oscillation should be settled down. Figure 27 shows feedback signal sampling timing, after the VS blanking time, the controller samples the VS pin voltage as V_{SD}. Once VS is lower than the threshold voltage of V_{TDIS} (VS−200 mV), the V_{SD} signal will be held as V_{S-SH}.

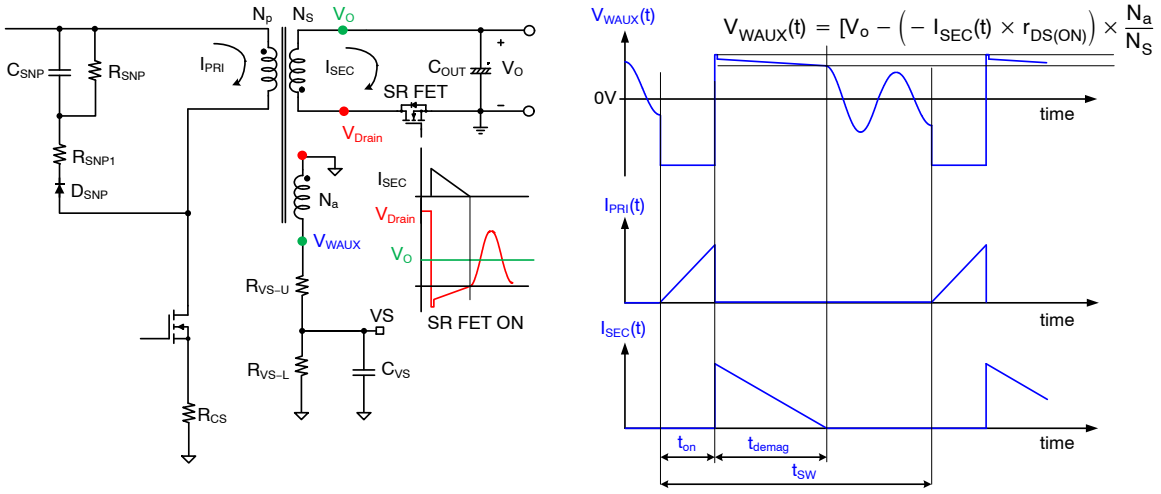


Figure 26. Typical Idealized Waveforms of a Flyback Transformer in DCM

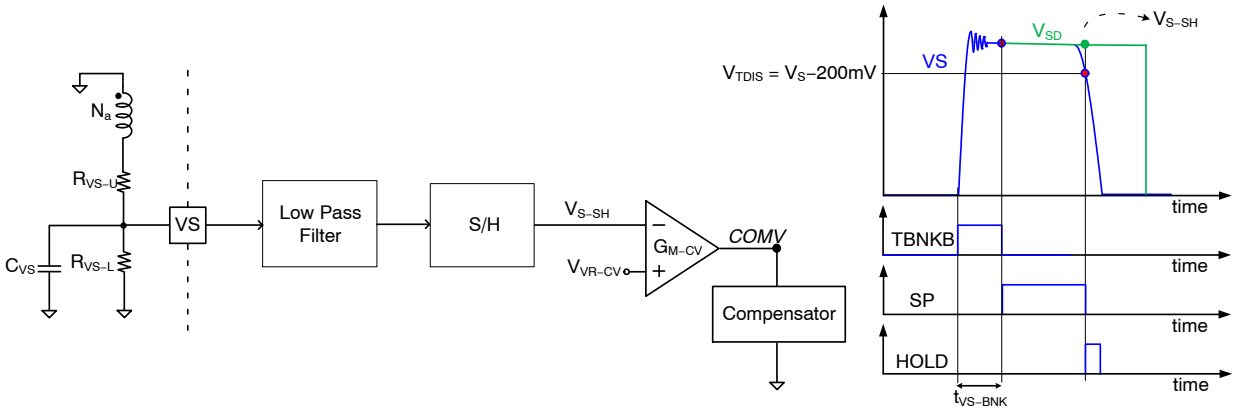


Figure 27. Constant Voltage Feedback Circuit and VS signal Sampling Timing

Primary Side Regulation: Constant Current Operation

Figure 28 shows the key waveforms of a flyback converter operation in DCM. The output current (I_O) is estimated by calculating the average of secondary current (I_{SEC}) in one switching cycle. The output current (I_O) can be calculated as

$$I_O = \frac{1}{2}\frac{1}{R_{CS}}\frac{V_{CS-PK}\cdot T_{DIS}}{T_{SW}}\frac{N_p}{N_S}\eta = \frac{1}{2}\frac{1}{R_{CS}}\frac{V_{VR-CC}}{A_{PK}}\frac{N_p}{N_S}\eta \quad \text{(eq. 4)}$$

When the secondary current reaches zero, the transformer winding voltage begins to drop sharply, and VS pin voltage drops as well. When VS pin voltage drops below the V_S by more than 200 mV, zero current point of secondary current is obtained.

The output current can be programmed by setting the current sensing resistor as:

$$R_{CS} = \frac{1}{2}\cdot\frac{1}{I_O}\cdot\frac{V_{VR-CC}}{A_{PK}}\cdot\frac{N_P}{N_S}\cdot\eta \quad \text{(eq. 5)}$$

where $V_{VR\text{-}CC}$ is the internal voltage for constant current control, η is efficiency of flyback and A_{PK} is the IC design parameter, 3.6 for FAN108.

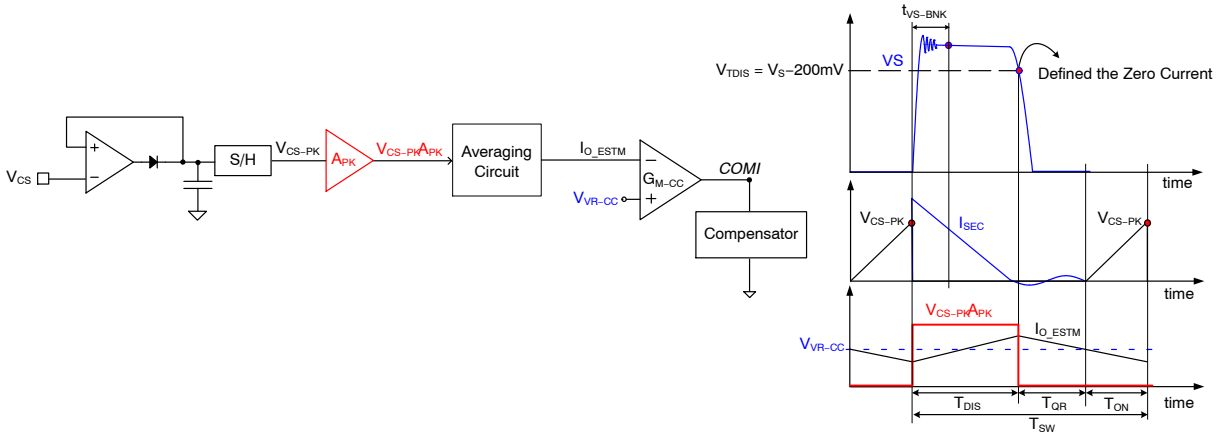


Figure 28. Constant Current Feedback Circuit and Control Sequence

Line Voltage Compensation

The output current estimation is also affected by the turn−off delay of the power FET as shown in Figure 29. The actual power FET's turn−off time is delayed due to the FET gate charge and gate driver's capability, resulting in peak current detection error as

$$\Delta I_{DS}^{PK} = \frac{V_{BLK}}{L_m} \times t_{OFF,FLY} \quad \text{(eq. 6)}$$

where L_m is the transformer's primary side magnetizing inductance and V_{BLK} is bulk voltage. Since the output current error is proportional to the line voltage, the FAN108 incorporates line voltage compensation to improve output current estimation accuracy.

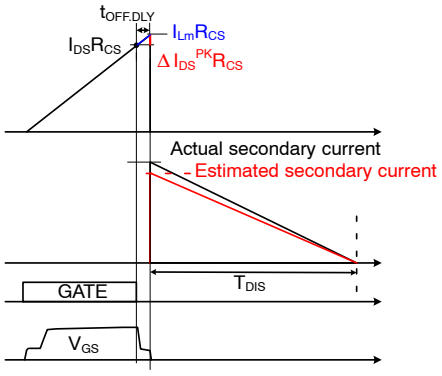


Figure 29. MOSFET Turn-off Delay

Line information is obtained through the line voltage detector as shown in Figure 31. I_{COMP} is an internal current source which is proportional to line voltage. The line compensation gain is programmed by using CS pin series resistor, R_{CS_COMP}, depending on the power FET turn−off delay ($t_{OFF.DLY}$). I_{COMP} creates a voltage drop (V_{OFFSET}) across R_{CS_COMP}. This line compensation offset is proportional to the DC link capacitor voltage (V_{BLK}) and turn−off delay ($t_{OFF.DLY}$). Figure 30 demonstrates the effect of the line compensation.

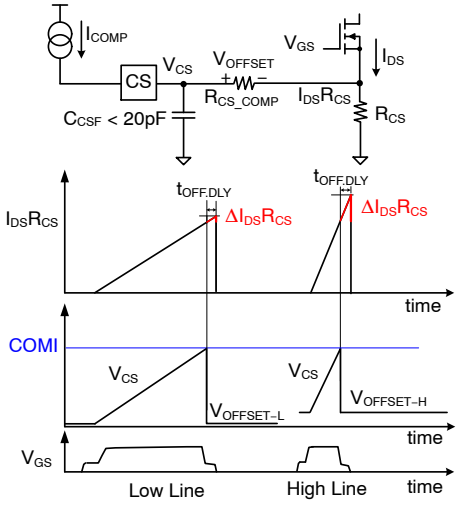


Figure 30. Line Voltage Compensation

CV / CC PWM Control Principle

Figure 31 shows a simplified CV / CC PWM control circuit of the FAN108. The Constant Voltage (CV) regulation is implemented internally with primary−side control. The output signal of compensation (COMV) is scaled down by attenuator A_{V-CV} to generate a V_{FB-CV} signal. This V_{FB-CV} signal is applied to the PWM comparator to determine the duty cycle.

The Constant Current (CC) regulation is implemented internally with primary−side control. The output current estimator calculates the output current using the transformer primary−side current and secondary current discharge time (T_{DIS}). By comparing the estimated output current with internal reference signal, a COMI signal is generated. The COMI signal is scaled down by attenuator A_{V-CC} to generate a V_{FB-CC} signal. This V_{FB-CC} signal is applied to the PWM comparator to determine the duty cycle.

These two control signals, V_{FB-CV} and V_{FB-CC} are compared with a voltage of current sense (V_{CS}) by two PWM comparators to determine the duty cycle. Figure 31 illustrates the outputs of two comparators combined with an OR gate, to determine the power FET turn−off instant. Either of V_{FB-CV} or V_{FB-CC}, the lower signal determines the duty cycle. During CV regulation, V_{FB-CV} determines the duty cycle while V_{FB-CC} is saturated to HIGH level. During CC regulation, V_{FB-CC} determines the duty cycle while V_{FB-CV} is saturated to HIGH level.

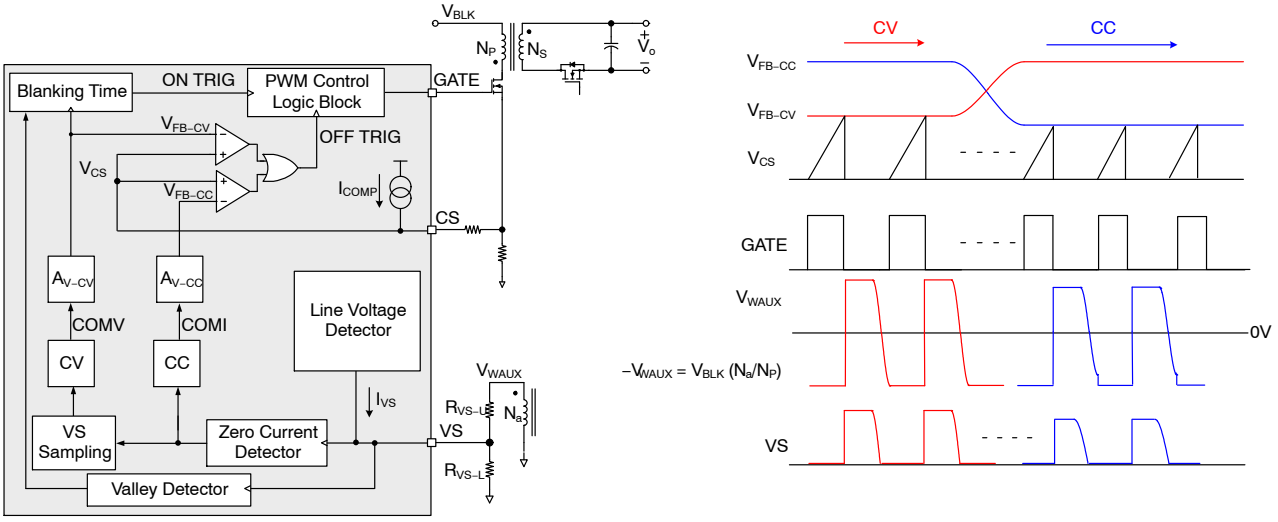


Figure 31. Simplified PSR Flyback Converter Circuit

Valley Detection and Frequency Fold−back

The quasi−resonant (QR) switching is a method to reduce primary side switching losses. To perform QR turn−on of the power FET, the valley of the resonance occurring between transformer magnetizing inductance (L_m) and effective output capacitance ($C_{oss-eff}$) must be detected.

The resonant period is detected by monitoring the time of 1/4 resonant period from end of secondary current discharge time (T_{DIS}) to VS signal reaches zero. FAN108 will turn on the power FET at 1/2 resonant period after the blanking frequency as shown in Figure 32.

For heavy load condition, the blanking time for the valley detection is fixed and primary side peak current will be modulated by voltage level of feedback (V_{FB-CV}). For the medium load condition, the blanking time is modulated as a function of load current such that the upper limit of the blanking frequency varies from $f_{BNK-MAX}$ as load decreases where the blanking frequency reduction stop point is $f_{BNK-MIN}$. For the light load condition, the peak of V_{CS} is fixed by $V_{CS-IMIN}$ (0.175 V) and the energy will be modulated by the function of Pulse Frequency Modulation (PFM), as shown in Figure 31.

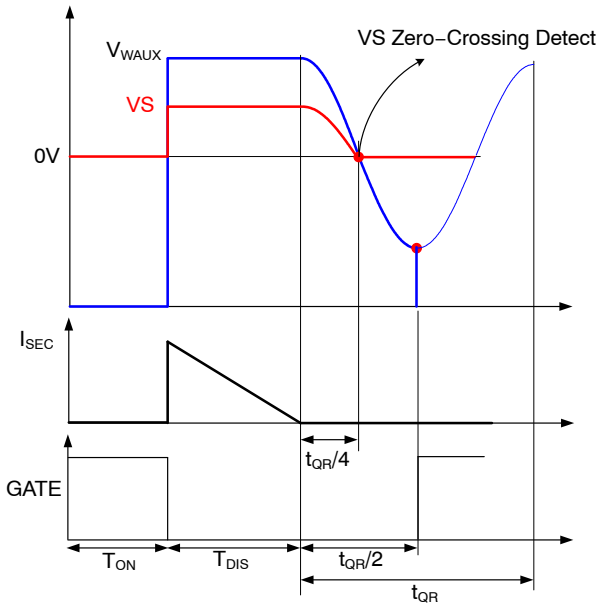


Figure 32. Valley Detection

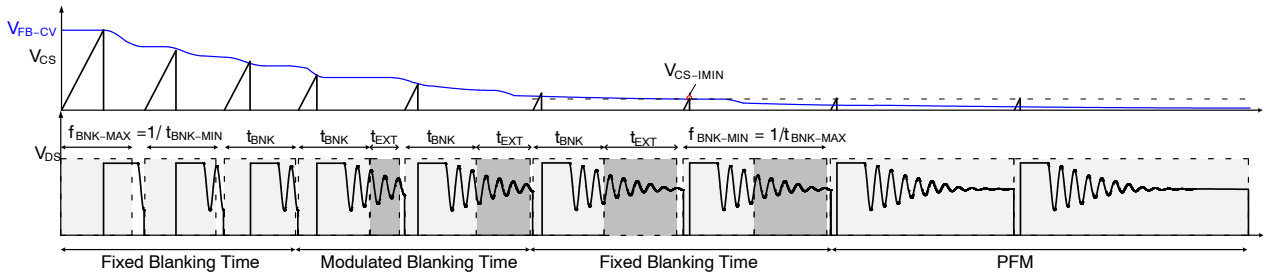


Figure 33. Frequency Fold−back Function

Cable Drop Compensation (CDC)

FAN108 integrates cable drop compensation function; this circuitry compensates the drop due to the cable connected between the PCB output of the charger and the final equipment. As the drop is linearly varying with the output current level, this level can be compensated by accounting for the load output current.

The weighting of CDC provides a constant output voltage at the end of the cable over the entire load range in CV mode. The voltage of cable drop compensation at output is proportional to VS compensation weighting that is internal reference voltage with CDC compensation as

$$V_O = \frac{N_S}{N_a}\left(1 + \frac{R_{VS-U}}{R_{VS-L}}\right) \times \left(V_{VR-CV} + \Delta V_{CDC} \times \frac{I_O}{I_{O-CC-NOM}}\right) \quad \text{(eq. 7)}$$

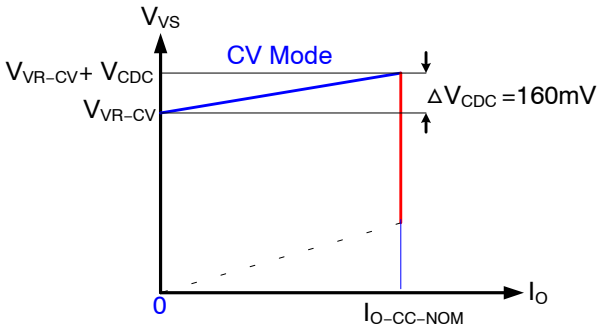


Figure 34. CV−CC Curve with CDC

Protections

The FAN108 self−protection includes VDD Over−Voltage−Protection (VDD−OVP), Internal Chip Over−Temperature−Protection (OTP), VS Over−Voltage Protection (VS−OVP), VS Under−Voltage Protection (VS−UVP), CS pin Protection (CSP), Brown−out and Brown−In protection, and all of protection are implemented as Auto Restart (AR) mode. When the Auto−Restart Mode protection is triggered, switching is terminated and the power FET remains off, causing VDD to drop because of IC operating current I_{DD-OP} (1.2 mA). When VDD drops to the VDD turn−off voltage V_{DD-OFF} (6.5 V), operation current reduces to I_{DD-ST} (20 μA) and the protection is reset and the supply current drawn from bulk capacitor begins to charge the VDD hold−up capacitor. When VDD reaches the turn−on voltage V_{DD-ON} (17.5 V), the FAN108 resumes normal operation. In this manner, the Auto−Restart mode alternately enables and disables the switching of the power FET until the abnormal condition is eliminated as shown in Figure 35.

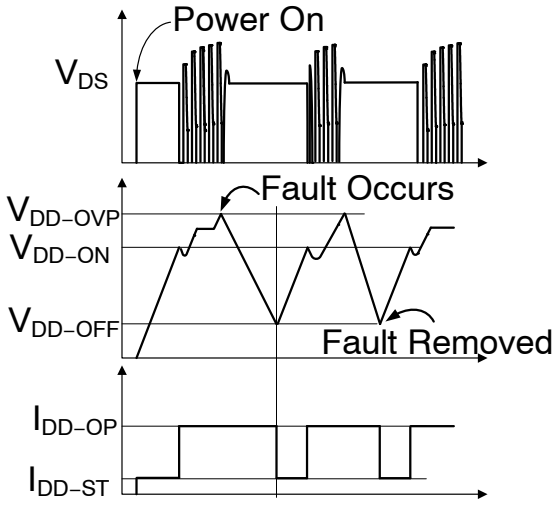


Figure 35. Auto−Restart Mode Operation

VDD Over−Voltage−Protection (VDD−OVP)

VDD over−voltage protection prevents IC damage from over−voltage stress. It is operated in Auto−Restart mode. When the VDD voltage exceeds V_{DD-OVP} (28 V) for the de−bounce time, $t_{D-VDDOVP}$ (120 μs), due to abnormal condition, the protection is triggered. This protection is typically caused by the auxiliary winding turns are too many, load regulation is not good between transformer winding, VS information is not available anyhow and so on.

Brown−In and Brown−Out

Line voltage information is used for brown−out and brown−in protection. When the I_{VS} current out of the VS pin during the power FET conduction time is less than $I_{VS-Brown-OUT}$ (320 μA) for longer than 17 ms, the brown−out is triggered. The brown−out is set to around 20% margin of the minimum voltage on the bulk capacitor to allow adapter deliver maximum power under the low line full load condition. The input bulk capacitor voltage to trigger brown−out protection is given as

$$V_{BO} = \frac{V_{BLK\cdot MIN}}{1.2} = I_{VS-Brown-OUT} \times \frac{R_{VS-U}}{\frac{N_a}{N_p}} \quad \text{(eq. 8)}$$

where $V_{BLK.MIN}$ is the minimum voltage on the bulk capacitor.

For the brown−in protection, when the I_{VS} current out of the VS pin during the power FET conduction time is over than $I_{VS-Brown-OUT}$ (465 μA) for more than 4 consecutive switching cycles, the brown−in is triggered. The input bulk capacitor voltage to trigger brown−in protection is given as

$$V_{BI} = I_{VS-Brown-IN} \times \frac{R_{VS-U}}{\frac{N_a}{N_p}} \quad \text{(eq. 9)}$$

VS Over−Voltage Protection (VS−OVP)

VS over−voltage protection prevents damage caused by output over−voltage condition. It is operated in Auto−Restart mode. Figure 36 shows the internal circuit of VS−OVP protection. When abnormal system conditions occur, which cause VS sampling voltage to exceed V_{VS-OVP} (2.95 V) for more than de−bounce cycles (N_{VS-OVP}), PWM pulses are disabled and FAN108 enters Auto−Restart protection. VS over−voltage conditions are usually caused by open circuit of the feedback network or a fault condition in the VS pin voltage divider resistors. For VS pin voltage divider design, R_{VS-U} is obtained from Equation 8 and 9 and R_{VS-L} is determined by Equation 3. V_{O-OVP} can be determined by Equation 10

$$V_{O-OVP} = \frac{N_s}{N_a}\left(1 + \frac{R_{VS-U}}{R_{VS-L}}\right) \times V_{VS-OVP} \quad \text{(eq. 10)}$$

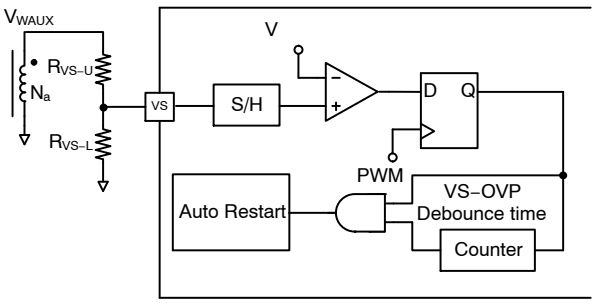


Figure 36. VS−OVP Protection Circuit

VS Under−Voltage Protection (VS−UVP)

In the event of an output short, output voltage will drop and the primary peak current will increase. To prevent operation for a long time in this condition, FAN108 incorporates under−voltage protection through VS pin. Figure 37 shows the internal circuit for VS−UVP. By sampling the auxiliary winding voltage on the VS pin at the end of SR FET conduction time, the output voltage is indirectly sensed. When VS sampling voltage is less than V_{VS-UVP} (1.6 V) and longer than de−bounce cycles N_{VS-UVP}, VS−UVP is triggered and the FAN108 enters Auto−Restart Mode.

To avoid VS−UVP triggering during the startup sequence a startup blanking time, $t_{VS-UVP-BLANK}$ (40 ms), is included when system is power−on. For VS pin voltage divider design, R_{VS-U} is obtained from Equation 8, 9 and R_{VS-L} is determined by Equation 3. V_{O-UVP} can be determined by Equation 11.

$$V_{O-UVP} = \frac{N_s}{N_a}\left(1 + \frac{R_{VS-U}}{R_{VS-L}}\right) \times V_{VS-UVP} \quad \text{(eq. 11)}$$

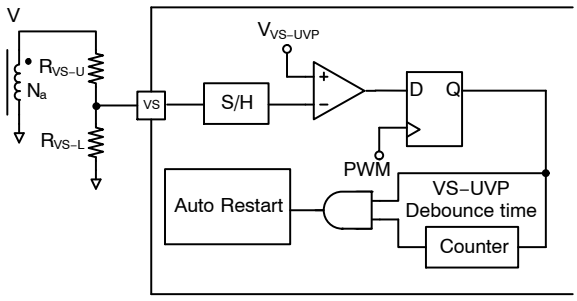


Figure 37. VS−UVP Protection Circuit

Cycle−by−Cycle Current Limit

During startup or overload condition, the feedback loop is saturated to high and is unable to control the primary peak current. To limit the current during such conditions, FAN108 has cycle−by−cycle current limit protection which forces the GATE to turn off when the CS pin voltage reaches the current limit threshold, V_{CS-LIM} (0.7 V).

Secondary−Side Diode Shot Protection

When the secondary−side diode is damaged, the slope of the primary−side peak current will be sharp within leading−edge blanking time. To limit the current during such conditions, FAN108 has secondary−side diode short protection which forces the GATE to turn off when the CS pin voltage reaches 1.6 V. After one switching cycle, it will operate in Auto−Restart mode as shown in Figure 38.

Current Sense Short Protection

Current sense short protection prevents damage caused by CS pin open or short to ground. After four switching cycle, it will operate in Auto−Restart mode. Figure 38 shows the internal circuit of current sense short protection. When abnormal system conditions occur, which cause CS pin voltage lower than 0.2 V after de−bounce time ($t_{CS-short}$) for more than 4 consecutive switching cycles, PWM pulses are disabled and FAN108 enters Auto−Restart protection. The $I_{CS-Short}$ is an internal current source, which is proportional to line voltage. The de−bounce time ($t_{CS-short}$) is created by $I_{CS-short}$, capacitor (2 pF) and threshold voltage (3.0 V). This de−bounce time ($t_{CS-short}$) is inversely proportional to the DC link capacitor voltage, V_{BLK}.

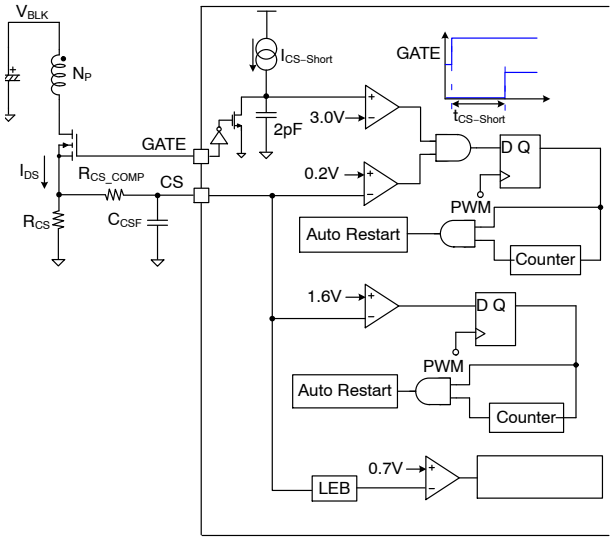


Figure 38. Current Sense Protection Circuit

Dynamic Response Enhancement (DRE)

PSR flyback converter regulates output voltage within requirement specification through detects VS signal which proportional to output voltage, However VS signal can only detect when power FET is switched. To get better standby power performance, the switching frequency is decreases to quite low frequency, the output voltage cannot be maintained as load suddenly increases from extremely light load to heavy load during such conditions. Therefore, FAN108 build in a Dynamic Response Enhancement (DRE) function to detect output voltage dropping immediately when FAN108 pair with FAN6250. Figure 39 shows DRE function relative signal working sequence. In the light load to no load condition, when the time of switching period is longer than time t_{HIZ-EN} (67 μs), the Hi−Z mode will be enabled which is let GATE pin become high impedance. Therefore, the GATE pin is changed from output to input and the signal on the GATE pin can be received.

FAN6250 VIN pin can detect the output voltage (V_O). When V_O is lower than the threshold of V_{DRE}, the FAN6250 drain pin will sink a current (I_{DRE}) from the secondary winding to ground and this current is via the transformer to primary side. Because of the transformer leakage inductance and the drain lumped capacitance, some voltage ringing appears on the drain node. The FAN108 GATE pin can receive the voltage ringing via C_{DS} and C_{GS}, is given as

$$V_{GATE} = \frac{C_{GD}}{C_{GD} + C_{GS}} \times V_{Drain} \qquad \text{(eq. 12)}$$

Once GATE pin received the signal of voltage ringing, FAN108 will turn on the power FET immediately and get output voltage information via VS pin. If the voltage of VS pin is lower than the threshold of $V_{VS-DNY-EN}$, the switching frequency increases immediately.

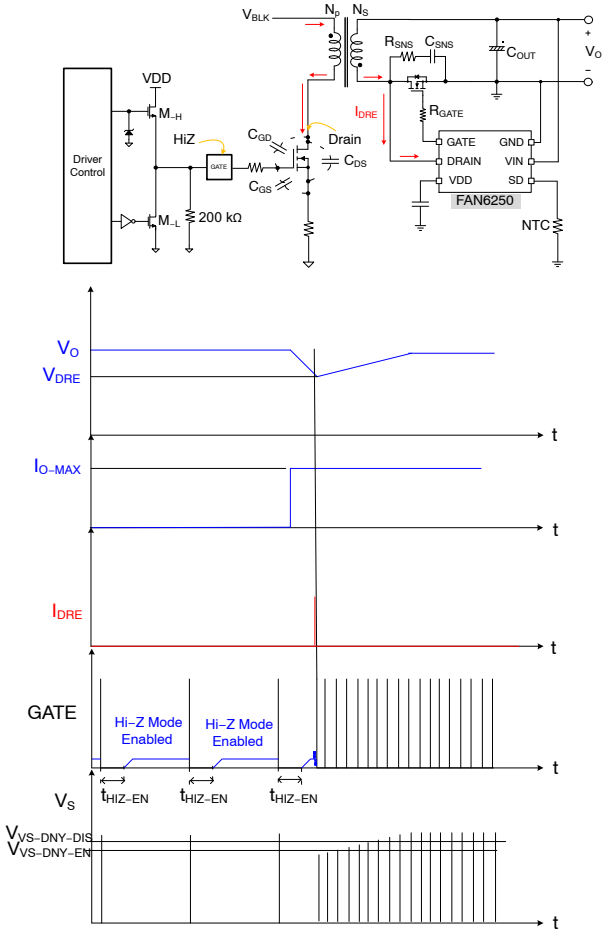


Figure 39. DRE Function Detecting Sequence

Secondary side Shut−Down Inform Protection

When Shut−Down function of FAN6250 is triggered, the SR controller will turn off the GATE intentionally as shown in Figure 40 and keep this status until VIN−OFF is touched When SR FET turns off intentionally, the secondary current I_{SEC} goes through the SR FET from source to drain diode and to generate the forward diode voltage V_{SD} (t_A) as

$$V_{SD}(t_A) = -I_{SEC}(t_A) \times r_D - V_f \qquad \text{(eq. 13)}$$

Where r_D is resistance of the diode and V_f is forward voltage. Usually the forward diode voltage (V_{SD}) is around 0.7 V to 1.3 V. The forward diode voltage (V_{SD}) will be reflected to VS pin by turns ratio and VS divider resistor as

$$V_{VS}(t_A) = (V_O - V_{SD}) \times \frac{N_a}{N_S} \times \frac{R_{VS-L}}{R_{VS-U} + R_{VS-L}} \qquad \text{(eq. 14)}$$

After the VS blanking time (t_{VS-BNK}), FAN108 samples the VS pin voltage and plus 100 mV as V_{SO}. During the discharge time, once VS is larger than V_{SO} and more than 15 consecutive switching cycles, PWM pulses are disabled and FAN108 enters Auto−Restart protection.

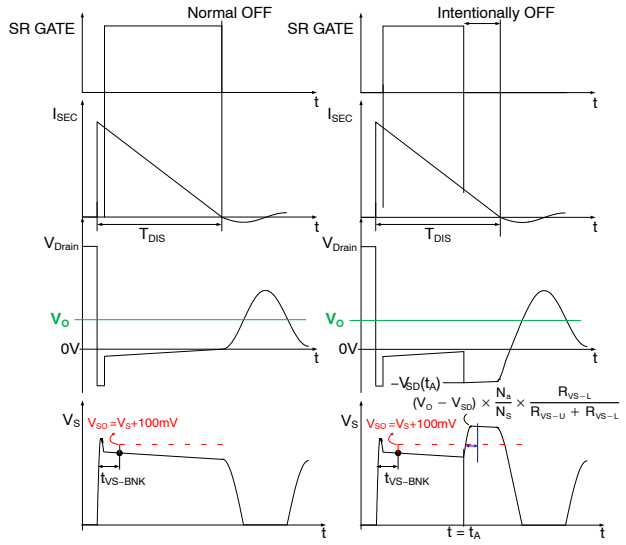


Figure 40. SR FET Normal OFF and Intentionally OFF

PCB Layout Guideline

Print circuit board (PCB) layout and design are very import for switching power supplies where the voltage and current change with high dv/dt and di/dt. A good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge/ESD tests. The following guidelines are recommended for layout designs.

- To improve EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitors C_{BLK1} and C_{BLK2} first, then to the transformer and MOSFET
- The primary−side high−voltage current loop is **C_{BLK2} − Transformer − MOSFET − R_{CS} − C_{BLK2}.** The area enclosed by this current loop should be as small as possible. The trace for the control signal (CS, VS and GATE) should not go across this primary high−voltage current loop to avoid interference
- Place R_{HV} for protection against the inrush spike on the drain pin of depletion FET (200 kΩ is recommended).R_{CS} should be connected to the ground of C_{BLK2} directly. Keep the trace short and wide (Trace **4** to **1**) and place it close to the CS pin to reduce switching noise. High−voltage traces related to the drain of MOSFET and RCD snubber should be away from control circuits to prevent unnecessary interference. If a heat sink is used for the MOSFET, connect this heat sink to ground
- As indicated by **2**, the area enclosed by the transformer auxiliary winding, D_{AUX} and C_{VDD}, should also be small
- Place C_{VDD}, C_{VS}, R_{VS-L}, R_{CS_COMP} and C_{CSF} close to the controller for good decoupling and low switching noise
- As indicated by **3**, the ground of the control circuits should be connected as a single point first, then to other circuitry
- Connect ground by **3** to **2** to **4** to **1** sequence. This helps to avoid common impedance interference for the sense signal
- Regarding the ESD discharge path, use the shortcut pad between AC line and DC output (most recommended). Another method is to discharge the ESD energy to the AC line through the primary−side main ground **1**. Because ESD energy is delivered from the secondary side to the primary side through the transformer stray capacitor or the Y capacitor, the controller circuit should not be placed on the discharge path. **5** shows where the point−discharge route can be placed to effectively bypass the static electricity energy
- For the surge path, select fusible resistor of wire wound type to reduce inrush current and surge energy and use π input filter (two bulk capacitors and one inductance) to share the surge energy

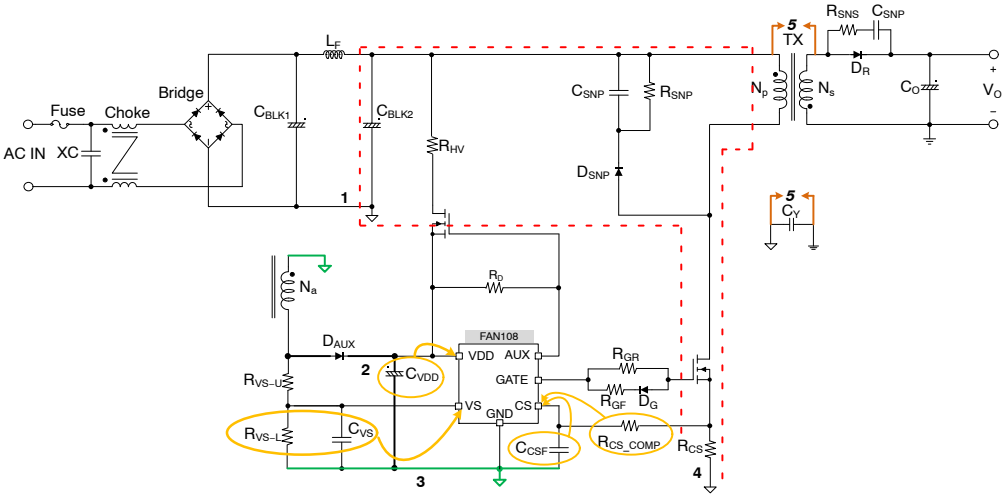


Figure 41. Recommended Layout for FAN108

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping †
FAN108M6X	−40°C to +125°C	6−Lead, SOT23	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

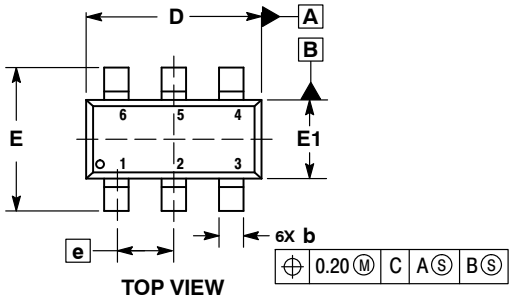
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

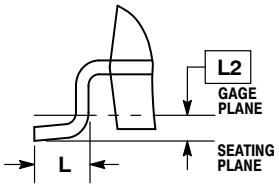
ON Semiconductor®

SOT−23, 6 Lead
CASE 527AJ
ISSUE B

DATE 29 FEB 2012

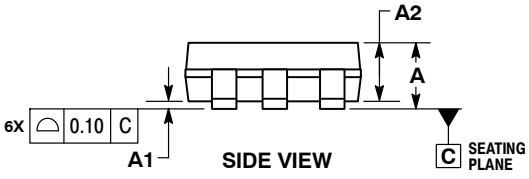
SCALE 2:1

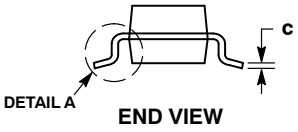




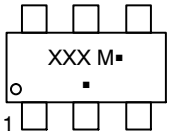
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.20	0.50
c	0.08	0.26
D	2.70	3.00
E	2.50	3.10
E1	1.30	1.80
e	0.95 BSC	
L	0.20	0.60
L2	0.25 BSC	





GENERIC MARKING DIAGRAM*

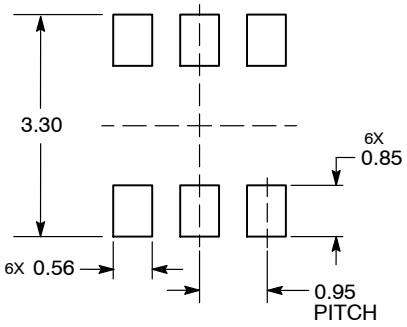


XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM POD #SOT236−029−01 TO ON SEMICONDUCTOR. REQ. BY B. BERGMAN.	19 DEC 2008
A	REDRAWN TO JEDEC STANDARDS. REQ. BY D. TRUHITTE.	12 JAN 2011
B	CORRECTED LABEL FOR MOLDED BODY DIMENSION OF TOP VIEW TO E1. REQ. BY D. TRUHITTE.	29 FEB 2012

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