NCD9812

Multichannel ADC, DACs and Temperature Sensors with I²C & SPI Interface

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Introduction

The NCD9812 is a serially programmable voltage and temperature monitor. It can monitor its on chip temperature via its local sensor, and two remotely connected diodes and also voltage, via 16 analog inputs. Four of these analog inputs can be programmed to be differential type inputs. By default, they are all single ended inputs. Multiple 12 bit DACs allow for voltage control on 12 pins. Eight GPIO pins allow digital control and monitoring. An /ALERT output is also available to signal out−of−limit conditions.

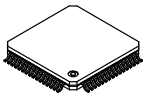
Communication with the NCD9812 is accomplished via an I²C interface which is compatible with industry standard protocols or a 4 wire SPI interface. Both interfaces are available on this part. Through these interfaces the NCD9812s internal registers may be accessed. These registers allow the user to read the current temperature and input voltages, change the configuration settings, adjust each channels limits and set set the output DAC voltages on each of the 12 channels available.

The NCD9812 is available in a 64−lead QFN package and 64−lead TQFP operates over a temperature range of –40 to +125°C.

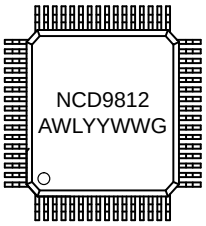
Features

- On−chip Temperature Sensor (±2.5°C Accuracy)
- 2 Remote Temperature Sensors (±3.5°C Accuracy)
- 16 Analog Voltage Inputs (12 bit). 2 Differential and 12 Single Ended
- 12, 12 bit DAC Output Channels
  - 0 V to 5 V
- 8 Digital GPIO Pins
- 2.5 V Internal Reference
- Power Saving Shutdown Mode
- SPI and I²C Interface
- Package Type:
  - 64−lead QFN
  - 64−lead TQFP

MARKING DIAGRAMS



TQFP64 EP, 10x10
CASE 136AC



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

QFN64 9x9, 0.5P
CASE 485CT

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCD9812FBR2G	TQFP64	1000 / Tape & Reel
NCD9812MNTXG	QFN64	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

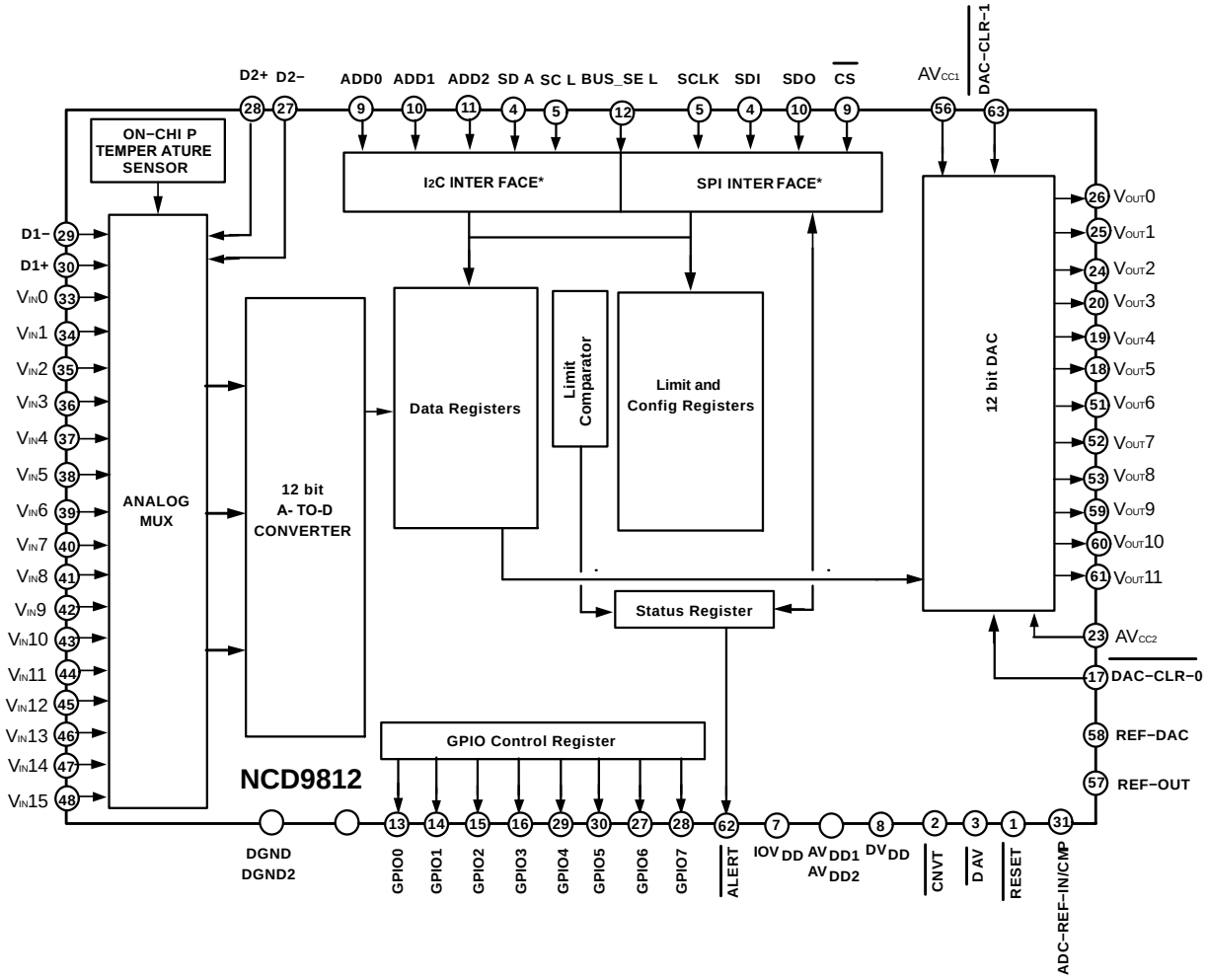


Figure 1. Functional Block Diagram of NCD9812

Pin Connections

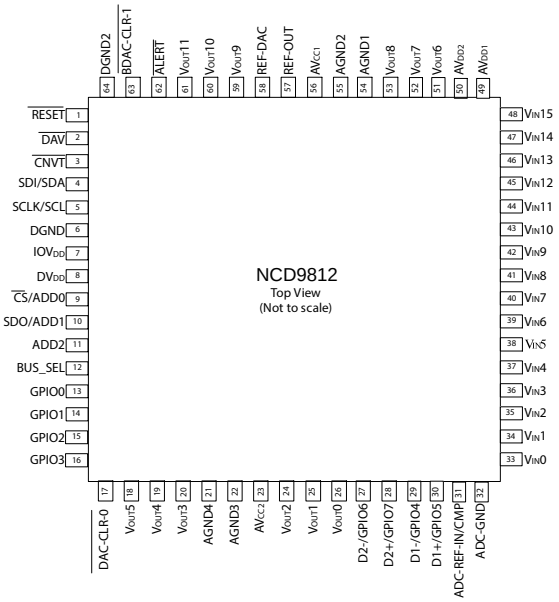


Figure 2. Pin Connections (Top View)

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	/RESET	Active low reset input. A hardware reset is performed when a logic low is seen on this pin.
2	/DAV	Data available. Active low output. In direct mode, this pin goes low when the conversion ends. In auto mode, a 1 μs pulse appears on this pin when the conversion cycle finishes. /DAV stays high when inactive.
3	/CNVT	External Conversion Trigger. Active Low. The falling edge starts the sampling and conversion of the ADC.
4	SDI / SDA	Serial Data Input in SPI mode. Serial Data Input/Output in I^2C mode.
5	SCLK / SCL	Serial Clock Input for SPI and I^2C interfaces
6	DGND	Digital Ground. This is the ground pin for all the digital circuitry.
7	IOV_{DD}	Interface supply rail.
8	DV_{DD}	Power Supply. Can be powered from a supply in the range 3V to 5V.
9	/CS/ADD0	Chip Select. Slave transmit enable in SPI mode – active low. Address selection pin for I^2C mode. Can be tied high or low to give multiple address options.
10	SDO/ADD1	Serial Data Out in SPI mode. Address selection pin for I^2C mode. Can be tied high or low to give multiple address options.
11	ADD2	Address selection pin for I^2C mode. Can be tied high or low to give multiple address options.
12	BUS_SEL	Selects I^2C or SPI interface. BUS_SEL = DGND selects I^2C; BUS_SEL = V_{DD} selects SPI.
13	GPIO0	Programmable general purpose digital input or output. Requires pull up resistor.
14	GPIO1	Programmable general purpose digital input or output. Requires pull up resistor.
15	GPIO2	Programmable general purpose digital input or output. Requires pull up resistor.
16	GPIO3	Programmable general purpose digital input or output. Requires pull up resistor.
17	/DAC−CLR−0	DAC clear control signal, digital input, active low. When low, all DACs associated with the DAC−CLR−0 pin enter a clear state, the DAC Latch is loaded with predefined code, and the output is set to the corresponding level. However, the DAC−Data Register does not change. When the DAC goes back to normal operation, the DAC Latch is loaded with the previous data from the DAC−Data Register and the output returns to the previous level, regardless of the status of the SLDAC−n bit. When this pin is high, the DACs are in normal operation.
18	$V_{OUT}5$	Analog Output.
19	$V_{OUT}4$	Analog Output.
20	$V_{OUT}3$	Analog Output.
21	AGND4	Analog Ground
22	AGND3	Analog Ground
23	AV_{CC2}	Power rail for $V_{OUT}0$, $V_{OUT}1$, $V_{OUT}2$, $V_{OUT}3$, $V_{OUT}4$, $V_{OUT}5$. Must be tied to AV_{CC1}.
24	$V_{OUT}2$	Analog Output.
25	$V_{OUT}1$	Analog Output.
26	$V_{OUT}0$	Analog Output.
27	D1−/GPIO6	Negative Connection to Remote Temperature Sensor. Can be re−configured as a bi−directional GPIO pin (requires pull up resistor).
28	D1+/GPIO7	Positive Connection to Remote Temperature Sensor. Can be re−configured as a bi−directional GPIO pin (requires pull up resistor).
29	D2−/GPIO4	Negative Connection to Remote Temperature Sensor. Can be re−configured as a bi−directional GPIO pin (requires pull up resistor).
30	D2+/GPIO5	Positive Connection to Remote Temperature Sensor. Can be re−configured as a bi−directional GPIO pin (requires pull up resistor).
31	ADC−REF−IN/CMP	External ADC reference input when external V_{REF} is used to drive ADC. Compensation capacitor connection when internal V_{REF} is used to drive ADC.
32	ADC−GND	ADC ground. Must be connected to AGND.
33	$V_{IN}0$	Analog Input. Programmable as single ended or differential input.

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
34	$V_{IN}1$	Analog Input. Programmable as single ended or differential input.
35	$V_{IN}2$	Analog Input. Programmable as single ended or differential input.
36	$V_{IN}3$	Analog Input. Programmable as single ended or differential input.
37	$V_{IN}4$	Analog Input. Single Ended input.
38	$V_{IN}5$	Analog Input. Single Ended input.
39	$V_{IN}6$	Analog Input. Single Ended input.
40	$V_{IN}7$	Analog Input. Single Ended input.
41	$V_{IN}8$	Analog Input. Single Ended input.
42	$V_{IN}9$	Analog Input. Single Ended input.
43	$V_{IN}10$	Analog Input. Single Ended input.
44	$V_{IN}11$	Analog Input. Single Ended input.
45	$V_{IN}12$	Analog Input. Single Ended input.
46	$V_{IN}13$	Analog Input. Single Ended input.
47	$V_{IN}14$	Analog Input. Single Ended input.
48	$V_{IN}15$	Analog Input. Single Ended input.
49	AV_{DD1}	Analog Power Supply.
50	AV_{DD2}	Analog Power Supply.(Must be connected to AVDD1)
51	$V_{OUT}6$	Analog Output.
52	$V_{OUT}7$	Analog Output.
53	$V_{OUT}8$	Analog Output.
54	AGND1	Analog Ground.
55	AGND2	Analog Ground.
56	AV_{CC1}	Power rail for $V_{OUT}6$, $V_{OUT}7$, $V_{OUT}8$, $V_{OUT}9$, $V_{OUT}10$, $V_{OUT}11$. Must be tied to AV_{CC2}.
57	REF−OUT	Internal Reference Output which is internally shorted with REF−DAC pin
58	REF−DAC	DAC reference is internally supplied through ADC internal reference.
59	$V_{OUT}9$	Analog Output.
60	$V_{OUT}10$	Analog Output.
61	$V_{OUT}11$	Analog Output.
62	/ALERT	Open−Drain Logic Output Used as Interrupt. Active low output. Pulled low when one or more of the measurement channels are out of range.
63	/DAC−CLR−1	DAC clear control signal, digital input, active low. When low, all DACs associated with the DAC−CLR−1 pin enter a clear state, the DAC Latch is loaded with predefined code, and the output is set to the corresponding level. However, the DAC−Data Register does not change. When the DAC goes back to normal operation, the DAC Latch is loaded with the previous data from the DAC−Data Register and the output returns to the previous level, regardless of the status of the SLDAC−n bit. When this pin is high, the DACs are in normal operation.
64	DGND2	Digital Ground.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Value	Units
AV_{DD} to GND	−0.3 to +6	V
DV_{DD} to GND	−0.3 to +6	V
IOV_{DD} to GND	−0.3 to +6	V
AV_{CC} to GND	−0.3 to +6	V
DV_{DD} to DGND	−0.3 to +6	V
Analog input voltage to GND	−0.3 to AV_{DD} + 0.3	V
/ALERT, GPIO0−3. SCLK/SCL, and SDI/SDA to GND	−0.3 to +6	V
D1+/GPIO4, D1−/GPIO5, D2+/GPIO6, D2−/GPIO7 to GND	−0.3 V to AV_{DD} + 0.3	V
Digital input voltage to DGND	−0.3 V to IOV_{DD} + 0.3	V
SDO and /DAV to GND	−0.3 V to IOV_{DD} + 0.3	V
Operating Temperature Range	−40 to +125	°C
Storage Temperature Range	−40 to 150	°C
Junction Temperature Range	+150	°C
ESD Capability, Human Body Model (Note 2)	2500	V
ESD Capability, Charged Device Model (Note 2)	1000	V
ESD Capability, Machine Model (Note 2)	150	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Units
Thermal Characteristics, QFN−64 (Note 3)			°C/W
Thermal Resistance, Junction−to−Air (Note 4)	$R_{\theta JA}$	TBD	
Thermal Reference, Junction−to−Lead2 (Note 4)	$R_{\mu JA}$	TBD	

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. As measured using a copper heat spreading area of 650 mm^2 (or 1 in^2), of 1 oz copper thickness.

Table 4. ELECTRICAL CHARACTERISTICS

All specifications for −40°C to +105°C, AV_{DD} = DV_{DD} = 4.5V to 5.5V, AV_{CC} = +5V, AGND = DGND = 0V, IOV_{DD} = 2.7V to 5.5V, DAC output = 0V to 5V, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Units
DAC Performance					
DAC DC Accuracy					
Resolution	Guaranteed by design	12			Bits
INL (Relative Accuracy)	Measured by line passing through codes 020h and FFFh. T_A = 25°C			±5	LSB
DNL (Differential Nonlinearity)	12−bit monotonic, measured by line passing through codes 020h and FFFh		±0.3	±5	LSB
TUE (Total Unadjusted Error)	T_A = +25°C, DAC output = 5.0V			±10	mV
	T_A = +25°C, DAC output = 12.5V			±30	mV
Offset error	T_A = +25°C, DAC output = 5.0V code 020h			±5	mV
	T_A = +25°C, DAC output = 12.5V code 020h			±10	mV
Offset error temperature coefficient			±1		ppm/°C
Gain error	External reference, output = 0 V to +5 V T_A = 25°C		±0.025	±0.15	%FSR
Gain temperature coefficient			±2		ppm/°C
DAC Output Characteristics					
Output voltage range	V_{REF} = 2.5V, gain = 2	0		5	V
Output voltage settling time	DAC output = 0V to +5V, code 400h to code C00h, to 1/2 LSB, from /CS rising edge, R_L = 2kΩ, C_L = 200pF		10		μs
Slew rate			2.3		V/μs
Short−circuit current	Full−scale current shorted to ground		30		mA
Load current	Source and/or sink within 200mV of supply		±10		mA
Capacitive load stability	R_L = ∞	50			nF
DC output impedance	Code 800h		10		Ω
Power−on overshoot	AV_{CC} 0 to 5V, 2ms ramp		5		mV
Digital−to−analog glitch energy	Code changes from 7FFh to 800h, 800h to 7FFh		18		nV−s
Digital feedthrough	Device is not accessed		0.15		nV−s
Output noise	T_A = +25°C, at 1kHz, code 800h, gain = 2, excludes reference		93		nV/√Hz
	F = 0.1Hz to 10Hz, excludes reference		61		μV_{PP}
Internal Reference					
Output voltage	T_A = +25°C, REF−OUT pin	2.495	2.5	2.505	V
Output Impedance			600		Ω
Reference temperature coefficient			10	25	ppm/°C
ADC Performance					
ADC DC Accuracy (for AV_{DD} = 5V)					
Resolution	Guaranteed by design		12		Bits
INL (Integral nonlinearity)			±0.5	±1	LSB
DNL (Differential nonlinearity)			±0.5	±1	LSB
Single Ended Mode					
Offset error			±1	±5	LSB

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Parameter	Test Conditions	Min	Typ	Max	Units
Offset error match			±1		LSB
Gain error	External reference		±3.5	±7.5	LSB
Gain error match			±2		LSB
Differential Mode					
Gain error	External reference, 0V to ($2xV_{REF}$) mode, V_{CM} = 2.5V		±3	±13	LSB
	External reference, 0V to V_{REF} mode, V_{CM} = 1.25V		±3	±11	LSB
Gain error match			±3		LSB
Zero code error	0V to ($2xV_{REF}$) mode, V_{CM} = 2.5V		±1	±3	LSB
	External reference, 0V to V_{REF} mode, V_{CM} = 1.25V		±1	±3	LSB
Zero code error match			±1.5		LSB
Common mode rejection	DC, 0V to ($2xV_{REF}$) mode		67		dB
Sampling Dynamics					
Conversion rate	External single analog channel, auto mode		500		kSPS
	External single analog channel, direct mode		167		kSPS
Conversioin time	External single analog channel		2		μs
Autocycle update rate	All 16 single ended inputs enabled		32		μs
Throughput rate	SPI clock 12 MHz or greater, single analog channel			500	kSPS
Analog Input					
Full scale input voltage	Single ended, 0V to V_{REF} mode	0		V_{REF}	V
	Single ended, 0V to ($2xV_{REF}$) mode	0		$2xV_{REF}$	V
	V_{IN+} − $V_{IN−}$, fully differential, 0V to V_{REF} mode	$−V_{REF}$		$+V_{REF}$	V
	V_{IN+} − $V_{IN−}$, fully differential, 0V to ($2xV_{REF}$) mode	$−2xV_{REF}$		$+2xV_{REF}$	V
Absolute input voltage	0V to V_{REF} mode	GND – 0.2		AV_{DD} + 0.2	V
Input capacitance			40		pF
DC input leakage current	Unselected ADC input			±10	μA
ADC Reference Input					
Reference input voltage range		1.2		AV_{DD}	V
Input current	V_{REF} = 2.5V		10		μA
Internal ADC Reference Buffer					
Offset	T_A = +25°C			±5	mV
Internal Temperature Sensor					
Operating range		−40		+125	°C
Accuracy	AV_{DD} = 5V, T_A = −40°C to +125°C		±1.25	±2.5	°C
	AV_{DD} = 5V, T_A = 0°C to +100°C			±1.5	°C
Resolution	Per LSB, Guaranteed by design		0.125		°C
Conversion rate	External temperature sensors are disabled		15		ms

Table 4. ELECTRICAL CHARACTERISTICS

All specifications for −40°C to +105°C, AV_{DD} = DV_{DD} = 4.5V to 5.5V, AV_{CC} = +5V, AGND = DGND = 0V, IOV_{DD} = 2.7V to 5.5V, DAC output = 0V to 5V, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Units
External Temperature Sensor (using 2N3906 external transistor)					
Operating range		−40		+150	°C
Accuracy	AV_{DD} = 5V, T_A = 0°C to +100°C, T_D = −40°C to +150°C			±2	°C
	AV_{DD} = 5V, T_A = −40°C to +100°C, T_D = −40°C to +150°C			±3.5	°C
Resolution	Per LSB, Guaranteed by design		0.125		°C
Conversion rate per sensor	With resistance cancellation (RC=1)	72	93	100	ms
	With resistance cancellation (RC=0)	33	44	47	ms
Digital Logic: /ALERT, /CS, ADD and GPIO					
V_{IH} (Input high voltage)	IOV_{DD} = +5V	2.1		0.3 + IOV_{DD}	V
	IOV_{DD} = +3.3V	2.1		0.3 + IOV_{DD}	V
V_{IL} (Input low voltage)	IOV_{DD} = +5V/3.3V, all other pins	−0.3		0.8	V
	IOV_{DD} = +5V/3.3V, $\overline{CS}$ pin only	−0.3		0.6	V
V_{OL} (Output low voltage)	IOV_{DD} = +5V, sinking 5 mA			0.8	V
	IOV_{DD} = +3.3V, sinking 2 mA			0.8	V
High impedance leakage				7	μA
High impedance output capacitance				10	pF
Digital Logic: All except SCL, SDA, /ALERT, /CS, ADD and GPIO					
V_{IH} (Input high voltage)	IOV_{DD} = +5V	2.3		0.3 + IOV_{DD}	V
	IOV_{DD} = +3.3V	2.3		0.3 + IOV_{DD}	V
V_{IL} (Input low voltage)	IOV_{DD} = +5V	−0.3		0.8	V
	IOV_{DD} = +3.3V	−0.3		0.8	V
Input current				±1	μA
Input capacitance				5	pF
V_{OH} (Output high voltage)	IOV_{DD} = +5V, sourcing 3 mA	4.8			V
	IOV_{DD} = +3.3V, sourcing 3 mA	2.9			V
V_{OL} (Output low voltage)	IOV_{DD} = +5V, sinking 3 mA			0.4	V
	IOV_{DD} = +3.3V, sinking 3 mA			0.4	V
High impedance leakage				±5	μA
High impedance output capacitance				10	pF
Digital Logic: SDA, SCL					
V_{IH} (Input high voltage)	IOV_{DD} = +5V	2.1		0.3 + IOV_{DD}	V
	IOV_{DD} = +3.3V	2.1		0.3 + IOV_{DD}	V
V_{IL} (Input low voltage)	IOV_{DD} = +5V	−0.3		0.8	V
	IOV_{DD} = +3.3V	−0.3		0.8	V

Table 4. ELECTRICAL CHARACTERISTICS

All specifications for −40°C to +105°C, AV_{DD} = DV_{DD} = 4.5V to 5.5V, AV_{CC} = +5V, AGND = DGND = 0V, IOV_{DD} = 2.7V to 5.5V, DAC output = 0V to 5V, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Units
Input current				±5	μA
Input capacitance				5	pF
V_{OL} (Output low voltage)	IOV_{DD} = +5V, sinking 3mA	0		0.4	V
	IOV_{DD} = +3.3V, sinking 3mA	0		0.4	V
High impedance leakage				±5	μA
High impedance output capacitance				10	pF
Power on delay	From AV_{DD}, DV_{DD} ≥ 2.7V and AV_{CC} ≥ 4.5V		100	250	μs
Power down recovery time	From /CS rising time			70	μs
Convert pulse width		20			ns
Reset pulse width		20			ns
POWER REQUIREMENTS					
AV_{DD}	AV_{DD} must be ≥ (V_{REF} + 1.2V)	+2.7		+5.5	V
AI_{DD}	AV_{DD} and DV_{DD} combined, normal operation, no DAC load		7.9	12.5	mA
	AV_{DD} and DV_{DD} combined, all blocks in power down		2.8		mA
AV_{CC}		+4.5		+5.5	V
AI_{CC}	AV_{CC}, no load, DACs at code 800h			7.5	mA
Power dissipation	Normal operation, AV_{DD} = DV_{DD} = 5V, AV_{CC} = 15V		50	120	mW
DV_{DD}		+2.7		+5.5	V
IOV_{DD}		+2.7		+5.5	V
GENERAL INTERFACE INFORMATION					
Bit Rate	SPI			20	MHz
	I^2C Standard Mode			100	kHz
	I^2C Fast Mode			400	kHz
	I^2C High Speed Mode			3.4	MHz

I²C TIMING SPECIFICATION

Table 5. I²C TIMING CHARACTERISTICS PARAMETERS

T_A = −40°C to +125°C, V_{DD} = 3.3 V unless otherwise noted.

Parameter[1]	Symbol	Conditions	Min	Max	Units
Clock Frequency	f_{SCL}	Standard Mode	10	100	kHz
		Fast Mode		400	kHz
		High speed Mode (100pF)		3.4	MHz
		High speed Mode (400pF)		1.7	MHz
Bus Free Time	t_{BUF}	Standard Mode	4.7		s
		Fast Mode	1.3		μs
Start Hold Time[2]	$t_{HD;STA}$	Standard Mode	4.0		μs
		Fast Mode	600		ns
		High speed Mode	160		ns
SCL Low Time	t_{LOW}	Standard Mode	4.7		μs
		Fast Mode	1.3		μs
		High speed Mode (100pF)	160		ns
		High speed Mode (400pF)	320		ns
SCL High Time	t_{HIGH}	Standard Mode	4.0		μs
		Fast Mode	600		ns
		High speed Mode (100pF)	60		ns
		High speed Mode (400pF)	120		ns
Start Setup Time	$t_{SU;STA}$	Standard Mode	4.7		μs
		Fast Mode	600		ns
		High speed Mode	160		ns
Data Setup Time[3]	$t_{SU;DAT}$	Standard Mode	250	250	ns
		Fast Mode	100	100	
		High speed Mode	10	10	
Data Hold Time[4]	$t_{HD;DAT}$	Standard Mode	0	3.45	μs
		Fast Mode	0	0.9	μs
		High speed Mode (100pF)	0	70	ns
		High speed Mode (400pF)	0	150	ns
SCL Rise Time	t_{RCL}	Standard Mode		1000	ns
		Fast Mode	$20+0.1C_B$	300	ns
		High speed Mode (100pF)	10	40	ns
		High speed Mode (400pF)	20	80	ns
SCL Rise Time (after repeated start)	t_{RCL1}	Standard Mode		1000	ns
		Fast Mode	$20+0.1C_B$	300	ns
		High speed Mode (100pF)	10	80	ns
		High speed Mode (400pF)	20	160	ns
SCL Fall Time	t_{FCL}	Standard Mode		300	ns
		Fast Mode	$20+0.1C_B$	300	ns
		High speed Mode (100pF)	10	40	ns
		High speed Mode (400pF)	20	80	ns
SDA Rise Time	t_{RDA}	Standard Mode		1000	ns
		Fast Mode	$20+0.1C_B$	300	ns
		High speed Mode (100pF)	10	80	ns
		High speed Mode (400pF)	20	160	ns

1. Guaranteed by design, but not production tested.
2. Time from 10% of SDA to 90% of SCL.
3. Time for 10% or 90% of SDA to 10% of SCL.
4. A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

Table 5. I²C TIMING CHARACTERISTICS PARAMETERS

T_A = −40°C to +125°C, V_{DD} = 3.3 V unless otherwise noted.

Parameter[1]	Symbol	Conditions	Min	Max	Units
SDA Fall Time	t_{FDA}	Standard Mode Fast Mode High speed Mode (100pF) High speed Mode (400pF)	 20+0.1C_B 10 20	300 300 80 160	ns ns ns ns
Stop Setup Time	$t_{SU;STO}$	Standard Mode Fast Mode High speed Mode	4.0 600 160		µs ns ns
Capacitive load	C_B			400	pF
Glitch Immunity	t_{SP}	Fast Mode High−speed Mode		50 10	ns ns
Noise margin at high level	V_{NH}	Standard Mode Fast Mode High speed Mode	0.2V_{DD}		V
Noise margin at low level	V_{NL}	Standard Mode Fast Mode High speed Mode	0.1V_{DD}		V

1. Guaranteed by design, but not production tested.
2. Time from 10% of SDA to 90% of SCL.
3. Time for 10% or 90% of SDA to 10% of SCL.
4. A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

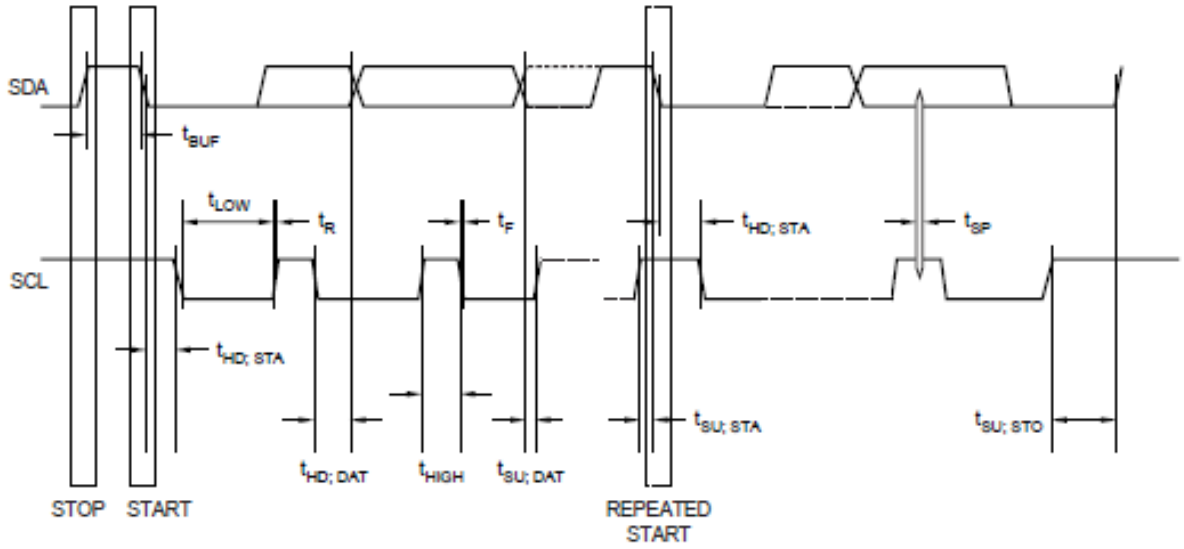


Figure 3. I²C Serial Interface Timing

SPI TIMING SPECIFICATION

Table 6. SPI TIMING CHARACTERISTICS PARAMETERS

Parameter	Symbol	Min	Max	Units
SPI Clock Freq	f_{SCLK}		20	MHz
SCLK cycle time	T_1	20		ns
SCLK High time	T_2	8		ns
SCLK Low time	T_3	8		ns
/CS falling edge to SCLK rising edge setup time	T_4	5		ns
Input data setup time	T_5	5		ns
Input data hold time	T_6	4		ns
SCLK falling edge to /CS rising edge	T_7	10		ns
Minimum /CS high time	T_8	30		ns
Output data valid time	T_9	3	20	ns
/CS rising to next /SCLK rising edge	T_{10}	3		ns

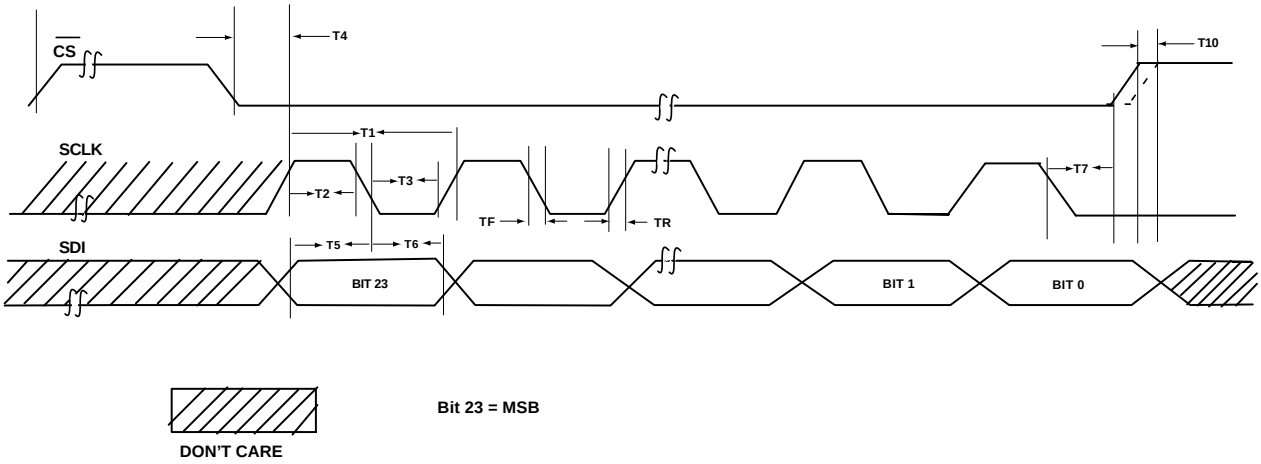


Figure 4. SPI Single Chip Write Operation

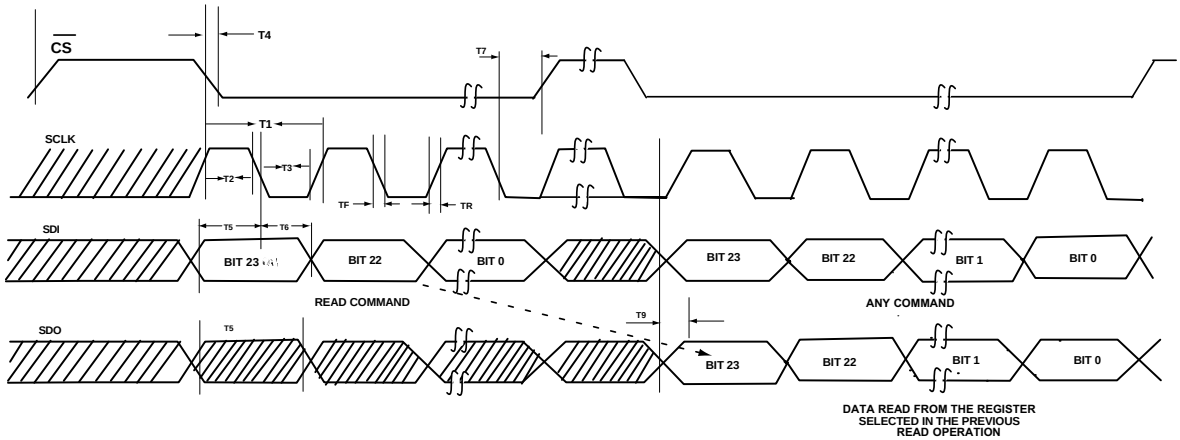


Figure 5. SPI Single Chip Read Operation

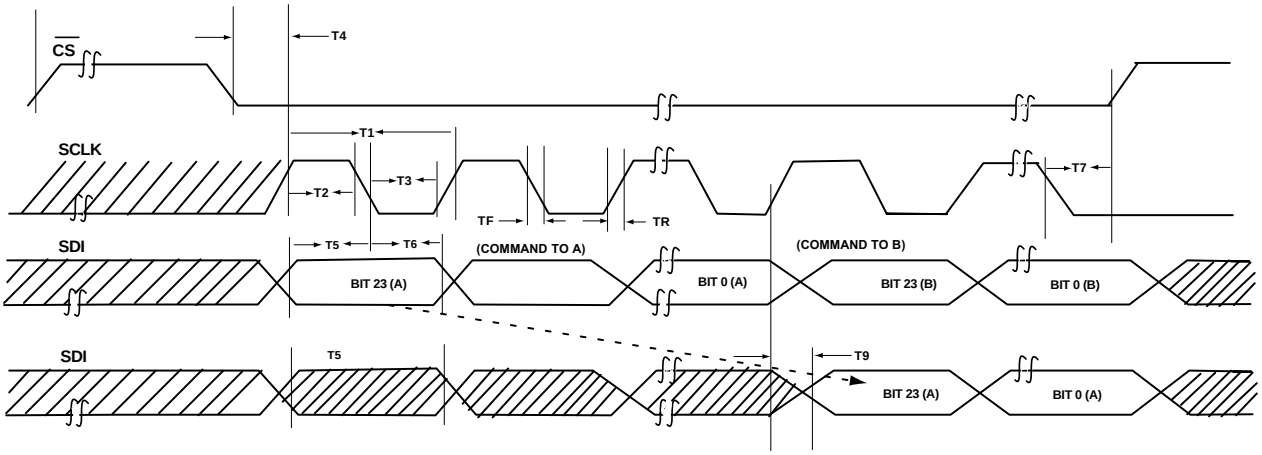


Figure 6. Daisy−Chain Operation of Two Devices

THEORY OVERVIEW

NCD9812 encompasses full analog monitoring, local and remote temperature sensing along with general purpose I/Os. The operational details of these functions are discussed below.

Power Supply Sequencing

All registers initialize to the default values after these supplies are established in the following (preferable not mandatory) order:

1. IOV_{DD}
2. DV_{DD}/AV_{DD}
3. AV_{CC}

If DV_{DD} falls below 2.7, the minimum supply value, either a hardware or power on reset should be issued to resume proper operation. GPIO4−7 inputs should not be applied until the AV_{DD} is established. This will avoid the activation of protection diodes of NCD9812. Similarly external reference should not be applied before AV_{DD} to ensure proper operation of the device. All the communication with the device will be valid after 250 μs maximum power−on reset delay.

RESET Options

Power ON Reset

When powered on the internal power on reset circuitry initiates a power−on−reset which perform the equivalent function of the /RESET pin. To ensure a power on reset, DV_{DD} must start from a level below 750 mV.

Hardware Reset

Hardware reset can be initiated by pulling the /RESET pin low. It should only be issued when DVDD has reached the minimum specification of 2.7 V or above. A hardware reset does the following:

- All registers (including Power−Down) set to default values
- All function Blocks are in power down state.
- Internal temperature sensor remains active.

A rising edge of /RESET returns the device back to normal operating mode. However, after the reset, it is important to properly write to the power−down register to activate the device.

Software Reset

Software reset can be initiated by writing to the software reset Register. In I^2C communication mode any values written to this register results in a reset. However, in case of SPI, only writing the specific value of 0x6600 to this register resets the device. Software reset returns all registers to their default values.

After issuing a software reset the user should wait at least 30 μs before attempting to resume communication as during reset all communication is blocked.

Analog to Digital Converters

The NCD9812 has two ADCs. A primary successive approximation ADC and a secondary sigma delta ADC.

Primary ADC

The primary ADC is a low power successive approximation ADC with a built in 16 analog channel multiplexer and 12 bit resolution. The 12 bit resolution assures high noise immunity and fast digitization that makes this device suitable for medium to high speed applications. The device internal circuiry operates at speed higher than the conversion time of the device because of the binary algorithm used. The algorithm is based on approximating the input signal by comparing with successive analog signal generated from the builtin DAC.

The value of each output bit is evalutaed on the basis of output of the comparator. The converter requires N conversion periods to give N bit digital output of the input analog signal. The SAR register stores the digital equivalent bits of the input analog signal and can be read by the master device using an I^2C interface. The main buiding block of the device are

- Digital to Analog Converter
- Comparator
- Digital Logic

Digital to Analog Converter

A charge scaling DAC is used due to its comaptibility with the switch capacitor circuits. The DAC operation consists of two phases called acquistion phase and the conversion phase. The acquistion phase is analogous to sample and hold circuit while the conversion phase is the process of conversion of the internal digital word in to an analog output.

Acquisition phase: The top plates of all the capacitors on the array are connected to the ground and the bottom plates are connected to the applied voltage Vin. Thus there is a charge proportional to input voltage on the capacitor array. After acquisition the top and bottom plates are disconnetd from their respective connections.

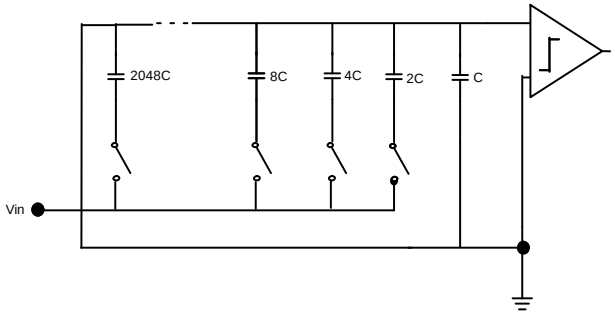


Figure 7. The Acquisition Phase of a Typical ADC

Conversion Phase*:* The converison phase is administered by a two phase non overlapping clock with phases ϕ_1 and ϕ_2 respectively. During ϕ_1 the bottom plates of all the capacitors are grounded i.e the top plates of all the capacitors are now Vin times higher than the ground. As the conversion process starts the digital control sets all the bits zero

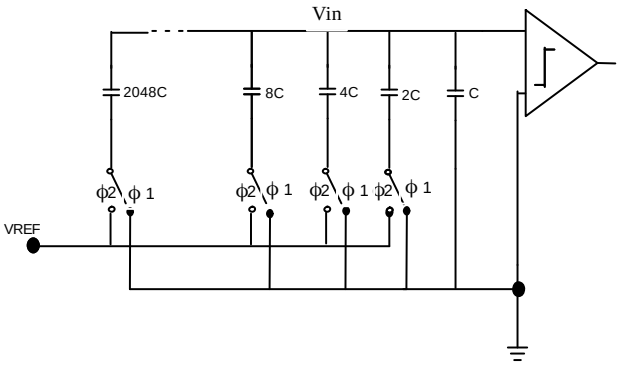


Figure 8. The Conversion Phase of a Typical ADC

except the MSB in the SAR register. During the ϕ_2 the capacitors associated with MSB is connected to V_{REF} while others are connected to ground. In this way the DAC generates analog voltage of magnitude $V_{REF}/2$. The analog output of DAC is compared with the input analog signal. The digital control logic sets the MSB to 1 if comparator output is high and 0 otherwise. Thus the first step of SAR algorithm decides whether the input signal is greater or less than $V_{REF}/2$. The approximation process is then run again with the MSB in its proven value and the next lower bit is set to 1. This gives a general direction path and the remaining approximations will converge the output in this direction.

Comparator

A switch capacitor comparator is used to alleviate the effects of input offset voltage. The issue of charge injection is controlled by using fully differential topology.

Digital Logic

The funcion of the digital logic is to generate the binary word to be compared with the input analog signal in each approximaiton cycle. The result of each approximation cycle is stored in the SAR register. In short the digital logic determines the value of each output bit in a sequential manner base don the output of the comparator.

Analog Channels

The analog inputs (CH0−CH15) are multiplexed into the on−chip successive approximation, analog−digital converter. The analog channels CH0−CH3 can be implemented as either four single ended channels or two fully differential channels depending upon the settings of registers ADC Channel Register 0 and ADC Channel Register 1. See the register section for details.

The internal 2.5 V reference will still be sufficient to provide full dynamic range for the 0 to V_{DD} analog input channels. In single ended applications it is recommended to buffer the analog input before applying to ADC where the signal source has high impedance. The analog input range is from 0 V − V_{ref} or 0 V − 2*V_{ref} which can be programmed through register settings.

When CH0−CH3 is configured as differential inputs only the differential voltage is converted and the common mode voltage is rejected. This shows that CH0−CH3 is fully differential in this mode. This corresponds to a noise free signal where the maximum allowed amplitude of input signal depends on the selected value of V_{ref} as follows

Vref Selection	Allowed Signal Amplitude
0 V − V_{ref}	$-V_{ref}$ to $+V_{ref}$
0 V − 2*V_{ref}	$-2*V_{ref}$ to $+2V_{ref}$

Full scale range of the analog channel is programmable through the Gain bit in the ADC Gain Register. In Single ended mode the full scale range is Vref when ADGN = 0 and 2*V_{ref} when ADGN = 1. In differential operation the corresponding channels input ranges are either ±V_{ref} or ±2*V_{ref}.

The analog inputs CH0−CH3 and the temperature inputs are implemented with out−of−range detection. Any out of range input sets the corresponding Alarm Flag in the Status Register. If any of the inputs are out of range, the global ALARM pin goes low. Device is also protected by a false Alarm protection mechanism. See the Alarm Operation section for more details.

Primary ADC Operation

Conversion Mode

NCD9812 primary ADC can be used in two operational modes. These are named as the Direct Mode and the Auto Mode. The CMODE (Conversion mode) bit of the Configuration Register 0 selects the active conversion mode.

In Direct Mode each analog channel within the specified group is converted once. After all the channels in the group are converted the ADC goes in to the idle state and waits for a new trigger. In Auto Mode each analog channel within the specified group is converted sequentially and repeatedly.

Triggering (external & internal CNVT)

An ADC conversion is initiated by the phenomenon called triggering. NCD9812 can be triggered externally by the falling edge of the external trigger pin /CNVT or internally through Configuration Register's bit ICONV setting.

When a new trigger activates the ADC stops any existing conversion immediately and waits for another trigger to start a new conversion cycle.

The internal trigger should not be issued at the same time the conversion mode is changed. If they occur simultaneously the current conversion stops and returns to the wait for ADC trigger state.

The conversion cycle stops immediately if any of the following events occur:

- A new trigger is issued.
- The conversion mode changes.
- Either ADC channel is rewritten.
- Any of the analog input threshold registers is rewritten.

The flow chart of the ADC conversion process is shown the figure below.

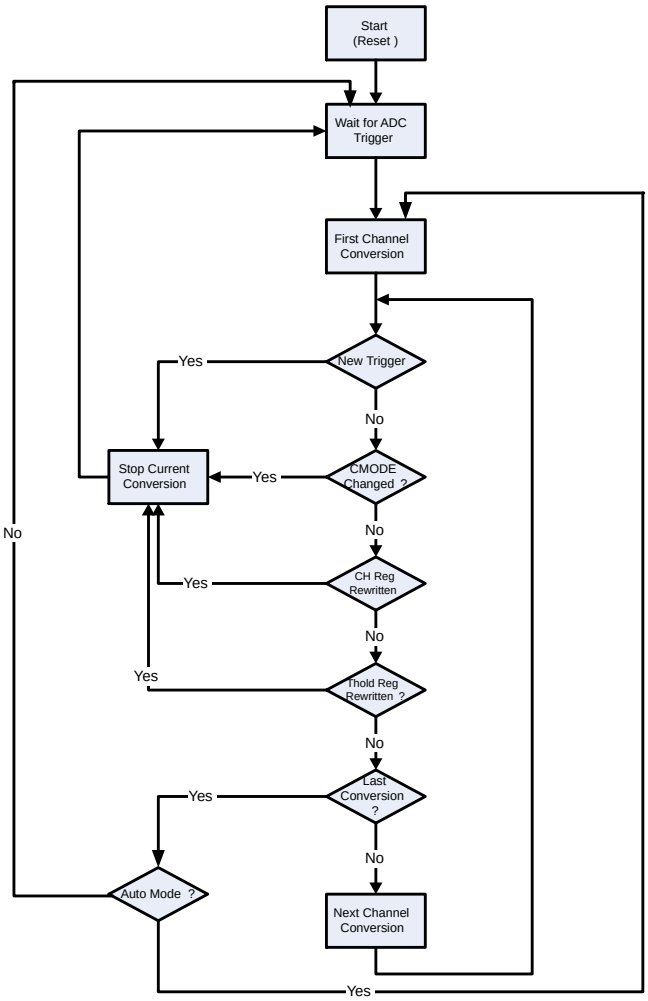


Figure 9. ADC Conversion Sequence

ADC Data Registers

The ADC data registers are used to store the digital converted data. There are 16 double buffered data registers. Each channel is associated with an ADC−n−TMPRY Register and an ADC−n− Data Register. During a conversion cycle when the conversion of an individual channel is completed, the data is immediately transferred to corresponding ADC−n−TMPRY Register. When the conversion of all the channels in a conversion cycle completes, all data in the ADC−n−TMPRY Registers are simultaneously transferred in to the corresponding ADC−n Data Registers. The results from channel 0 are stored in the ADC−0−Data Register and the result from channel 1 is stored in the ADC−1−Data Register and so on.

For a single ended input the conversion result is stored in straight binary format. For a differential input the results are stored in the 2’s complement format.

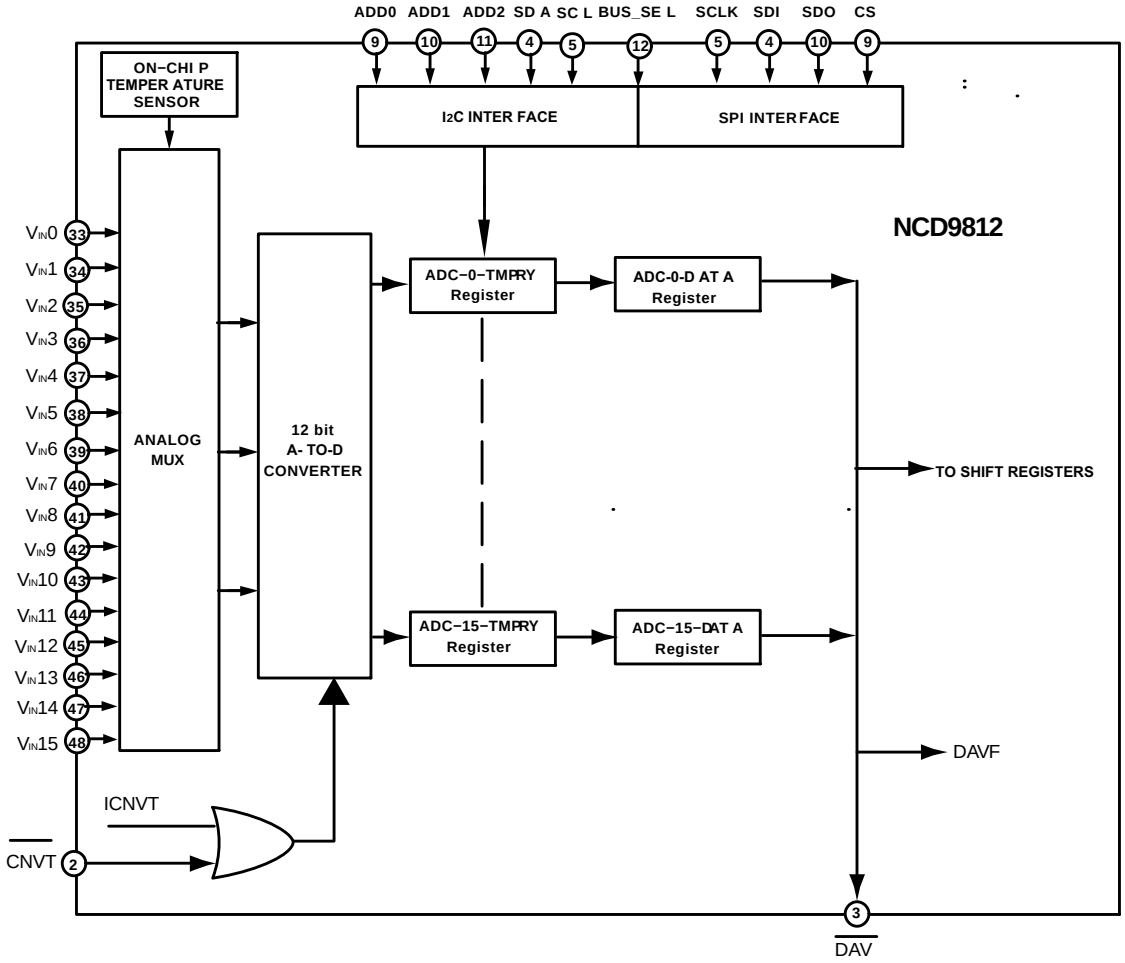


Figure 10. ADC Conversion Sequence

Handshaking protocol

The handshaking protocol is provided by the /DAV, /CNVT pins and the DAVF bit in the configuration Register 0. The function of /DAV & /CNVT pins are explained below:

External Convert Pin (/CNVT)

/CNVT is an input pin for external ADC trigger signal. Conversions begin on the falling edge of the /CNVT pulse. If a pulse occurs when the ADC is already converting, then the ADC continues the conversion of the current channel. After the conversion of current channel the existing conversion cycle finishes and ADC goes in to the wait state for new trigger pulse to start a new conversion.

Data Available Pin (/DAV)

/DAV is an output pin that indicates the completion of ADC conversion. The DAVF bit in the Configuration Register 0 determines the status of /DAV pin.

During handshaking with the host the pin and bit status of /DAV, /CNVT and DAVF depends on the conversion mode of the ADC as explained below:

Direct Mode:

In direct mode after ADC−n−Data Registers of all of the selected channels are updated, the DAVF bit in the Configuration Register 0 is set immediately to ‘1’ and the /DAV pin goes low to signify that new data is available.

The ADC clears the DAVF bit to 0 and deactivates the /DAV pin high when

- Reading of ADC−n−data register takes place.
- /CNVT pin is used to initiate an external trigger.

If ICONV bit is used to initiate a new ADC conversion, in order to reset the DAV status, an ADC−n−Data Register must be read after the current conversion finishes before a new conversion can be started.

Auto Mode:

In Auto Mode after the ADC−n−Data Registers of the selected channels are updated, a pulse of 1 μs (low) appears on the /DAV pin to signify that new data are available. The DAVF bit is always cleared to 0 in Auto Mode.

Conversion Rate Programming

The conversion rate is programmable through the CONV−RATE−[1:0] bits of Configuration Register 1. The maximum conversion rate is 500 KSPS for a single channel in auto mode. However, when more than one channel is selected the conversion rate is divided by the number of channels selected. The conversion rate programming for Auto and Direct conversions modes is explained below:

Direct Mode:

In Direct Mode the CONV−RATE−[1:0] bits limit the maximum possible conversion rate. The conversion rate in Direct Mode is determined by the rate of the conversion trigger. When a trigger is issued, there may be a delay of up to 4 μs to internally synchronize and initiate the start of the sequential conversion process.

Auto Mode:

In Auto Mode the CONV−RATE−[1:0] bits determine the actual conversion rate

In both the modes when the CONV−RATE−[1:0] bits are set to a value other than maximum rate (00), NAP Mode is activated between conversions. This mode reduces the AI_{DD} supply current.

CONV−RATE−1	CONV−RATE−0	t_{ACQ} (μs)	t_{CONV} (μs)	NAP	RATE(KSPS) (Single channel Auto Mode)
0	0	0.375	1.625	No	500
0	1	2.375	1.625	Yes	250
1	0	6.375	1.625	Yes	125
1	1	14.375	1.625	Yes	62.5

Secondary ADC

The secondary ADC runs at a lower speed in the background. The main function of this ADC is to digitize the analog temperature information received from two remote and one local (on chip) temperature sensors. The temperature sensors continuously monitor the three temperature inputs and new readings are automatically available every cycle.

Remote Sensing Diodes

The NCD9812 is designed to work with either substrate transistors built into processors or discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base−shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter is connected to D−. If a PNP transistor is used, the collector and base are connected to D− and the emitter is connected to D+.

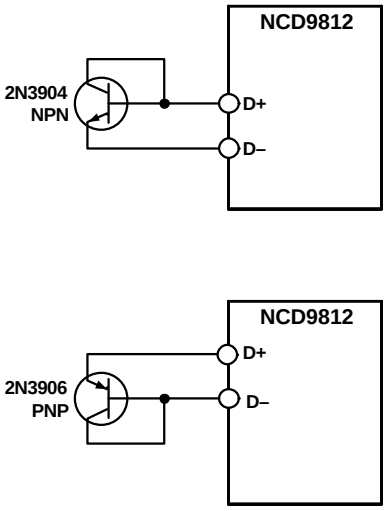


Figure 11. Remote Diode Connections Example

If a discrete transistor is used with the NCD9812, the best accuracy is obtained by choosing devices according to the following criteria:

- Base−emitter voltage is greater than 0.25 V at 6 μA with the highest operating temperature.
- Base−emitter voltage is less than 0.95 V at 100 μA with the lowest operating temperature.
- Base resistance is less than 100 Ω.
- There is a small variation in h_{FE} (for example, 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors such as 2N3904, 2N3906, or equivalents in SOT−23 packages are suitable devices to use. If alternative transistor is used the device operates as specified as long as the above condition are met.

Ideality Factor:

The ideality factor, η_f, of the transistor is a measure of the deviation of the thermal diode from ideal behaviour. The NCD9812 is trimmed for a power−on−reset value of $\eta = 1.008$. If ideality factor is different then the η−Factor Correction Register can be used. The value N_{adjust} written in this register must in 2's complement format. This value is used to adjust the effective η−factor according to Equations shown below

$$\eta_{eff} = \frac{1.008 \times 300}{300 - N_{adjust}}$$

$$N_{adjust} = 300 - \left(\frac{300 \times 1.008}{\eta_{eff}}\right)$$

- η_{eff} is the actual ideality factor f the transistor being used
- N_{adjust} is the corrected idealtiy factor being used in the calculation

N_{adjust}			η_{eff}
Binary	**Hex**	**Decimal**	
0111 1111	7F	127	1.747977
0000 1010	0A	10	1.042759
0000 1000	08	8	1.035616
0000 0110	06	6	1.028571
0000 0100	04	4	1.021622
0000 0010	02	2	1.014765
0000 0001	01	1	1.011371
0000 0000	00	0	1.008
1111 1111	FF	−1	1.004651
1111 1110	FE	−2	1.001325
1111 1100	FC	−4	0.994737
1111 1010	FA	−6	0.988235
1111 1000	F8	−8	0.981818
1111 0110	F6	−10	0.975484
1111 0000	80	−128	0.706542

Analog Temperature Measurement

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base emitter voltage (V_{BE}) of a transistor operated at constant current. However, this technique requires calibration to null the effect of the absolute value of V_{BE}, which varies from device to device.

The technique used in the NCD9812 measures the change in V_{BE} when the device operates at three different currents. Previous devices used only two operating currents, but it is the use of a third current that allows automatic cancellation of resistances in series with the external temperature sensor. Figure 12 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it can equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded but is linked to the base. To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal resistor at the D− input. C1 may be added as a noise filter (a recommended maximum value of 1000 pF).

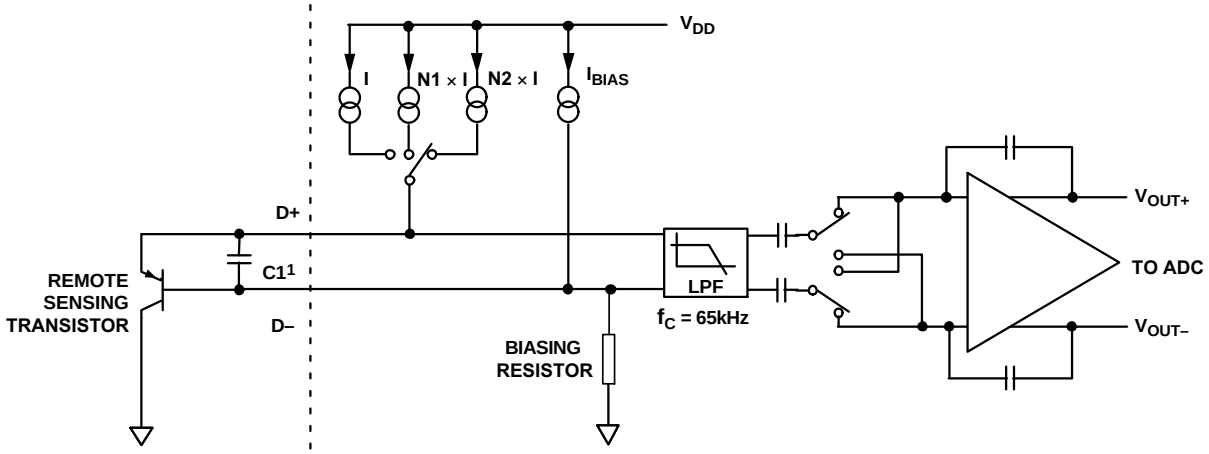
However, a better option in noisy environments is to add a filter, as described in the Noise Filtering section. See the Layout Considerations section for more information on C1.

Series Resistance Cancellation

To measure ΔV_{BE}, the operating current through the sensor is switched among three related currents. As shown in Figure 12, N1 x I and N2 x I are different multiples of the current, I. The currents through the temperature diode are switched between I and N1 x I, giving ΔV_{BE1}; and then between I and N2 x I, giving ΔV_{BE2}. The temperature is then calculated using the two ΔV_{BE} measurements. This method also cancels the effect of any series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low−pass filter to remove noise and then to a chopper−stabilized amplifier. This amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. The ADC digitizes this voltage producing a temperature measurement. To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles for low conversion rates. At rates of 16−, 32− and 64−conversions/second, no digital averaging occurs.

Signal conditioning and measurement of the internal temperature sensor is performed in the same manner.



[1]CAPACITOR C1 IS OPTIONAL. IT IS ONLY NECESSARY IN NOISY ENVIRONMENTS. C1 = 1000pF MAX.

Figure 12. Input Signal Conditioning

Diode Fault Conditions

Diode Short Condition

Shorting D+ to D− will cause that temperature channel to return 0xE000 and simultaneously set both “Dn−Low−ALR” and “Dn−High−ALR” bits of that channel in register 0x4F. “Dn−Fail−ALR” bits are not set.

Diode Open Condition

When there is no diode, the “Dn−Fail−ALR” bits are set and the temperature value register goes to a random value; however, when the diode is replaced temperature updates to the register is not resumed and the “Dn−Fail−ALR” bit remains set. The temperature sensor can be restarted by either toggling the “test pd fault detection” bit

Reading Temperature

The host reads the temperature data as 12 bit information. After digitization the data bits are sent to the corresponding Temp−Data Register. The temp−Data Register remains frozen while a transfer is in progress between itself and the Shift Register to ensure the validity of the read data. The conversion time of the ADC depends on the number of active temperature sensors and the configuration bit RC status set by the user. NCD9812 has two remote and one local temperature sensors. Any combinations of these sensors can be active at one time giving varying conversion times as shown in the Table below:

Active Sensors & Bit RC status	Cycle time (ms)	Programmable Delay Range (s)
Only local sensor	15	0.48 to 3.84
One remote sensor & RC = 0	44	1.40 to 11.2
One remote sensor & RC = 1	93	2.97 to 23.8
One remote sensor and local sensor & RC = 0	59	1.89 to 15.1
One remote sensor and local sensor & RC = 1	108	3.45 to 27.65
Two remote sensors & RC = 0	88	2.81 to 22.5
Two remote sensors & RC = 1	186	5.95 to 47.6
All sensors & RC = 0	103	3.92 to 26.38
All sensors & RC = 1	201	6.43 to 51.45

NOTE: Series resistance cancellation is always ON independent of the status of RC bit.

Reference Operation

NCD9812 can be used in conjunction with an internally generated reference or an externally supplied reference input. The selection of either can be made by using the ADC−REF−INT bit in the Configuration Register 0. In order to use the internal reference this bit must be set to 1 to turn ON the ADC reference buffer. The use of internal and external reference is explained below:

Internal Reference

The internal circuitry generates a 2.5 V reference. The internal reference drives all temperature sensors. Externally this reference is available at REF−OUT pin.

The REF−OUT pin is connected to the REF−DAC pin internally and the internal reference is always used as the DAC reference. A 100 pF − 10 nF capacitor is recommended between the reference output and GND for noise filtering. The figure opposite shows the use of internal reference for ADC and DAC in NCD9812.

The internal reference is available externally at REF−OUT and REF−DAC pins however; it should only be used to drive capacitive loads.

External Reference

ADC−REF−IN/CMP pin is used to supply the external reference. This pin has a dual function. When an external

reference is connected to this pin and ADC−REF−INT bit is set to 0, the external reference is used as the ADC reference. When a compensation capacitor (4.7 μF typical) is connected between this pin and the AGND and the ADC−REF−INT bit is set to 1, the internal reference is used as the ADC reference. The figure opposite shows the use of external reference for ADC and DAC in NCD9812.It should be noted that external reference cannot be used for the DAC reference.

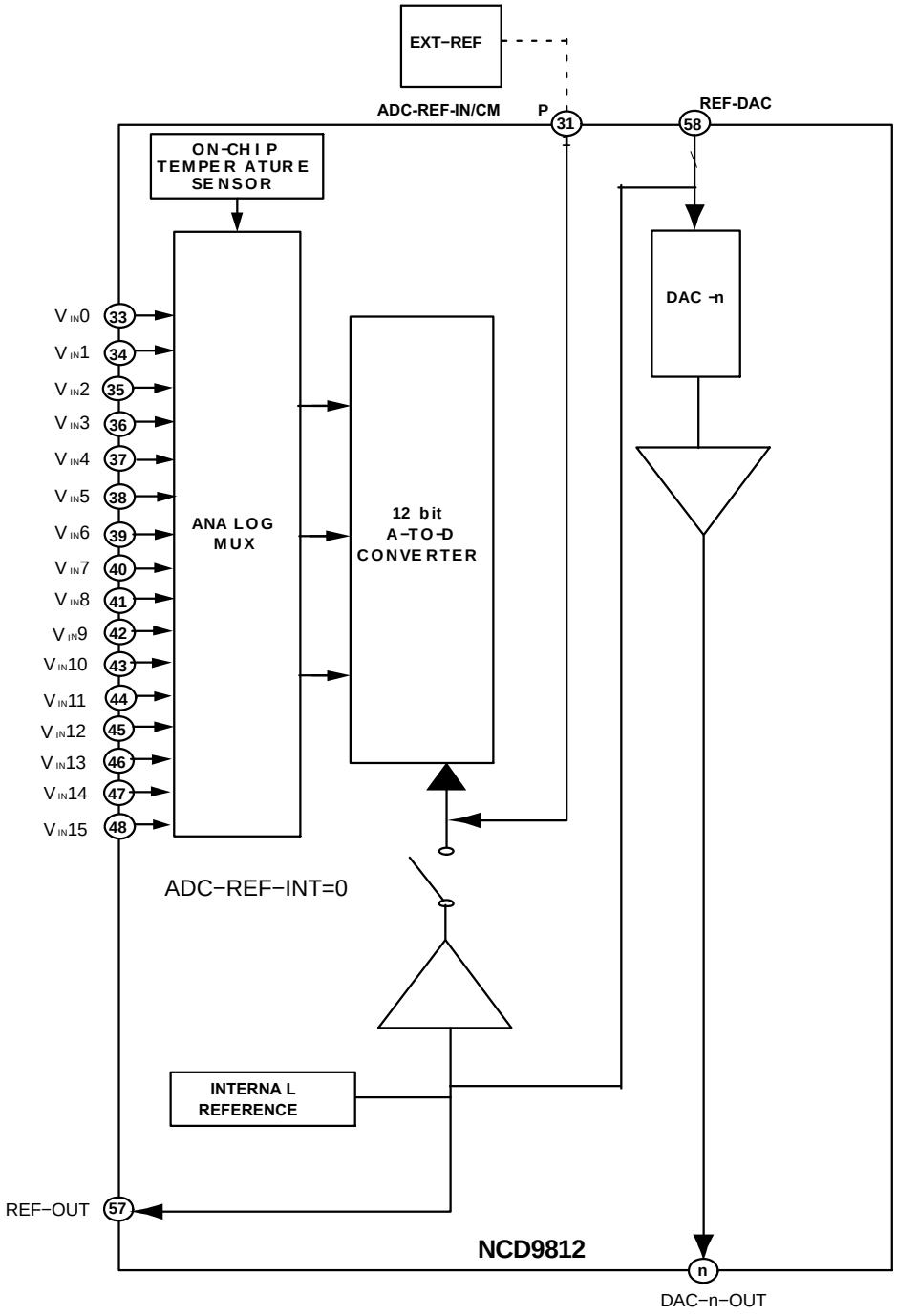


Figure 13. External Reference Operation

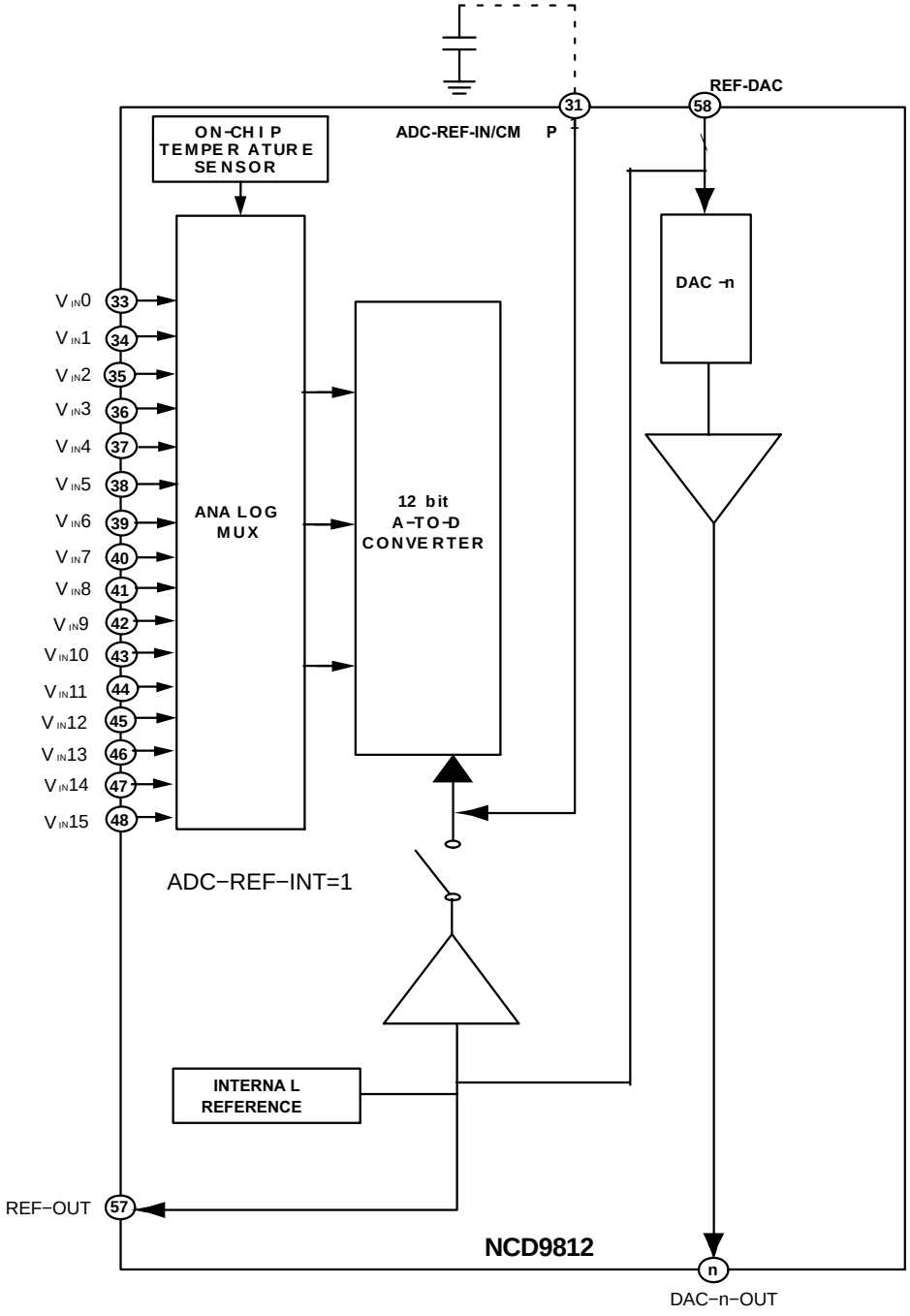


Figure 14. Internal Reference Operation

DAC OPERATION

There are 12 DACS output that can be programmed with 12 bits resolution. This is a decoder type based Resistor String converter where N bits are used to create 2^N value output using an external or internal reference.

Resistor String DAC

A resistor string in connected to a switch network. The switch network is connected like a tree as shown in the figure below. Depending on the bits there will be only one low impedance path between the resistor string and the input of the amplifier. Figure 15 shows the block diagram of resistor string DAC architecture.

The resistor string consists of resistors, each with value R. The code loaded to the DAC Latch determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The output of the DAC is set from 0 to $2*V_{ref}$. The DAC output is limited by the analog power supply and the maximum DAC output value is AVCC.

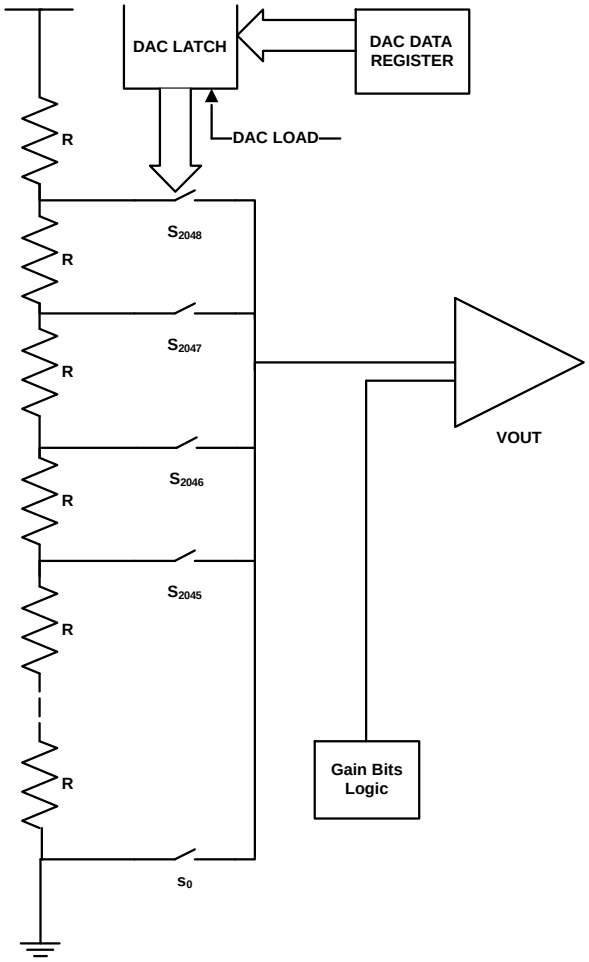


Figure 15. DAC Resistor String

DAC DATA REGISTERS

Double buffered data registers are associated with each DAC. Each DAC has a latch register preceded by a data register. Data is initially written to the DAC−n−Data Register and then transferred to its corresponding DAC−n−Latch Register. When the latch is updated, the output of the DAC−n−Data changes to the newly value. Host reads the data from the DAC−n−Latch and not from DAC−n−Data Register.

DAC Latch updating modes:

There are two modes by which the DAC−n−Latch can be updated. These modes are explained below:

Synchronous Mode

Synchronous load DAC (SLDAC−n) bit in the DAC Configuration Register (0x58) decides the operating mode of the DACs. When the SLDAC−n bit is set to 1, synchronous mode is selected. In this mode the DAC−n−Latch is updated only when the internal DAC loading signal occurs. Writing 1 to ILDAC bit in the Configuration Register 0 generates an internal load trigger signal that updates the DAC−n Latches and DAC−n outputs with the contents of the corresponding DAC−n−Data Register. Several DACs can be updated simultaneously provided that DAC−n−Data registers contain the required data and SLDAC−n bits of the corresponding DACs are set to 1 prior to the setting of ILDAC bit.

Asynchronous Mode

When the SLDAC−n bit is set to 0, asynchronous mode is selected. In this mode the DAC−n−Latch is updated immediately after the write operation on the DAC−n−Data Register.

The device updates the DAC latches only if has been read by the Host since the last ILDAC was issued. This is to avoid any unnecessary glitch. This mean any DAC channels that have not been read are not reloaded again.

Clearing of DACs

DAC−n outputs can be cleared using hardware or software methods.

Hardware Clear Pins

NCD9812 contains two external control lines, /DAC−CLR−0 and /DAC−CLR−1 pins to clear the DAC outputs. When either pin goes low, the corresponding user−selected DACs are in cleared state. HW_DAC_CLR_0 register determines which DAC outputs are cleared when /DAC−CLR−0 pin is low. Similarly HW_DAC_CLR_1 register determines which DAC outputs are cleared when /DAC−CLR−1 pin is low. These registers contain 12 CLR−n bits, one for every DAC. Setting any of the CLR−n bits to 1 in any of the HW−DAC_CLR register determines which DAC is cleared when the corresponding pin is low. For example if the CLR−2 bit is set to 1 in HW−DAC_CLR_0 register, the DAC2 output will be cleared when the /DAC−CLR−0 pin is lowered. Similarly if the CLR−4 bit is set to 1 in HW−DAC_CLR_1 register, the DAC4 output will be cleared when the /DAC−CLR−1 pin is lowered.

Software Clear

DACs can be cleared using software by

- Writing the SW_DAC−CLR register.
- By ALARM events.

The selected DACs can be cleared by writing directly to the SW−DAC−CLR (0x55) Register. DACs can also be forced to clear by alarm events. The AUTO−DAC−CLR−SOURCE Register determines which alarm events force the DACS in to clear state, while the AUTO−DAC−CLR−EN Register defines which DACs will be cleared by the specified alarm events.

When DAC−n goes to clear state, it is immediately loaded with predefined code in the DAC−n−CLR−SETTING Register. The output is set to the corresponding level to shutdown the external LDMOS device. However, the DAC−n−DATA Register does not change. When the DAC goes back to normal operation, DAC−n is immediately loaded with the previous data from the DAC−n−DATA Register and the output of the DAC−n is set back to previous

level to restore LDMOS to the status before shutdown, regardless of SLDAC−n bit status.

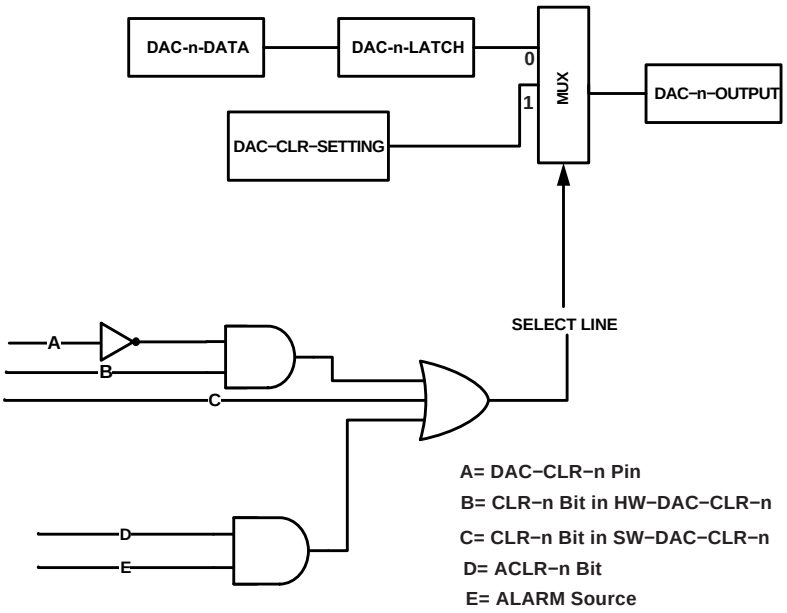


Figure 16. Clearing of DACs

DAC Thermal Management

DAC outputs are prone to dissipate a significant amount of power. A thermal protection circuit is present in NCD9812 that sets the THERM−ALR bit in the Status Register if the die temperature exceeds 150°C.

ALARM Operation

The NCD9812 continuously monitors all analog inputs and temperatures in normal operation. When any input is out of the specified range, an alarm triggers and the corresponding individual alarm bit in the Status Register is set (‘1’). Global alarm bit GALR in Configuration Register 0 is the OR of individual Alarms.

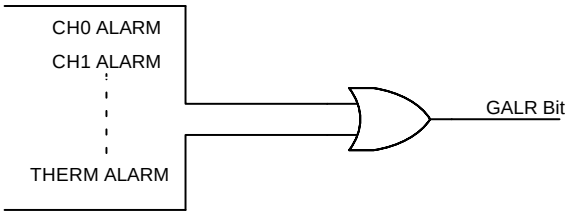


Figure 17. Global Alarm Bit

When the ALARM−LATCH−DIS bit in the Alarm Control Register is cleared (‘0’), the alarm is latched. The global alarm bit (GALR) maintains ‘1’ until the corresponding error condition[s] subsides and the alarm status is read. The alarm bits are referred to as being *latched* because they remain set until read by software. All bits are cleared when reading the Status Register, and all bits are reasserted if the out−of limit condition still exists on the next monitoring cycle, unless otherwise noted. When the ALARM−LATCH−DIS bit in the Alarm Control Register is set (’1’), the alarm bit is not latched. The alarm bit in the Status Register goes to ‘0’ when the error condition subsides, regardless of whether the bit is read or not. When GALR = ‘1’, the ALARM pin goes low. When the GALR bit = ‘0’, the ALARM is high (inactive).

The NCD9812 provides out−of−range detection for four individual analog inputs (CH0, CH1, CH2, and CH3). When the measurement is out−of−range, the corresponding alarm bit in the Status Register is set to ‘1’ to flag the out−of−range condition. The value in the High−Threshold Register defines the upper bound threshold of the nth analog input, while the value in Low−Threshold defines the lower bound. These two bounds specify a window for the out−of−range detection.

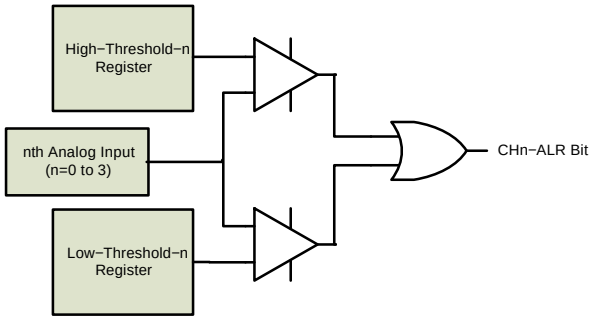


Figure 18. CHn Out−of−Range Alarm

The NCD9812 also has high−limit or low−limit detection for the temperature sensors (D1, D2, and LT. To implement single, upper−bound threshold detection for analog input CH*n*, the host processor can set the upper−bound threshold to the desired value and the lower−bound threshold to the default value. For lower bound threshold detection, the host processor can set the lower−bound threshold to the desired value and the upper−bound threshold to the default value. Note that the value of the High−Threshold Register must not be less than the value of the Low−Threshold Register; otherwise, ALR−*n* is always set to ‘1’ and the alarm indicator is always active. Each temperature sensor has two alarm bits: High−ALR (high−limit alarm) and Low−ALR (low−limit alarm).

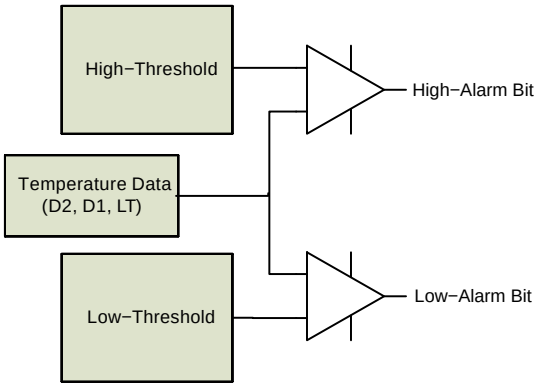


Figure 19. Temperature Out−of−Range Alarm

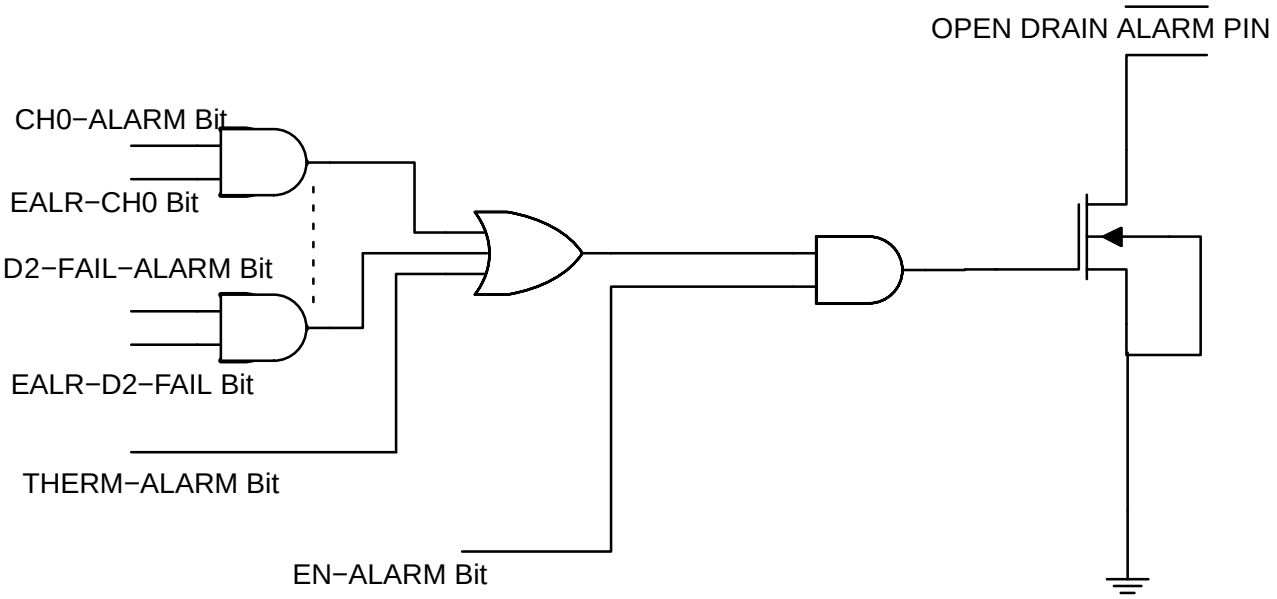


Figure 20. /ALARM Pin

The /ALARM pin is a global alarm indicator. ALARM is an open−drain pin. When the pin is activated, it goes low. When the pin is inactive, it is in Hi−Z status. The /ALARM pin works as an interrupt to the host so that it may query the Status Register to determine the alarm source. Any alarm event (including analog inputs, temperatures, diode status, and device thermal condition) activates the pin if the alarm is not masked (the corresponding EALR bit in the Alarm Control Register = ‘1’). When the alarm pin is masked (EN−ALARM bit = ‘0’), the occurrence of the event sets the corresponding status bit in Status Register to ‘1’, but does not activate the /ALARM pin.

When the ALARM−LATCH−DIS bit in the Alarm Control Register is cleared (‘0’), the alarm is latched. Reading the Status Register clears the alarm status bit. Whenever an alarm status bit is set, indicating an alarm condition, it remains set until the event that caused it is resolved and the Status Register is read. The alarm bit can only be cleared by reading the Status Register after the event is resolved, or by hardware reset, software reset, or power−on reset (POR). All bits are cleared when reading the Status

Register, and all bits are reasserted if the out−of limit condition still exists after the next conversion cycle, unless otherwise noted. When the ALARMLATCH−DIS bit in the Alarm Control Register is set (‘1’), the ALARM pin is not latched. The alarm bit clears to ‘0’ when the error condition subsides, regardless of whether the bit is read or not.

Hysteresis & False Alarm Protection

The NCD9812 continuously monitors the analog input channels and temperatures. If any of the alarms are out of range and the alarm is enabled, its alarm bit is set (‘1’). However, the alarm condition is cleared only when the conversion result returns to a value of at least hysteresis below the value of High Threshold Register, or hys above the value of Low Threshold Register. The Hysteresis Registers store the value for each analog input (CH0, CH1, CH2, and CH3) and temperature (D1, D2, and LT). Hys is the value of hysteresis that is programmable: 0 LSB to 127

LSB for analog input, and 0°C to +31°C for temperatures. For the THERM−ALR bit, the hysteresis is fixed at 8°C.

When any input is out of the specified range in N consecutive conversions, the corresponding alarm bit is set (‘1’). If the input returns to the normal range before N consecutive times, the alarm bit remains clear (‘0’). This design avoids false alarms. The number N is programmable by the CH−FALR−CT−[2:0] bits in AMC Configuration Register 1 for analog input CH−n as shown in Table 7, or by the TEMP−FALR−CT−[1:0] bits for temperature monitors as shown in Table 8.

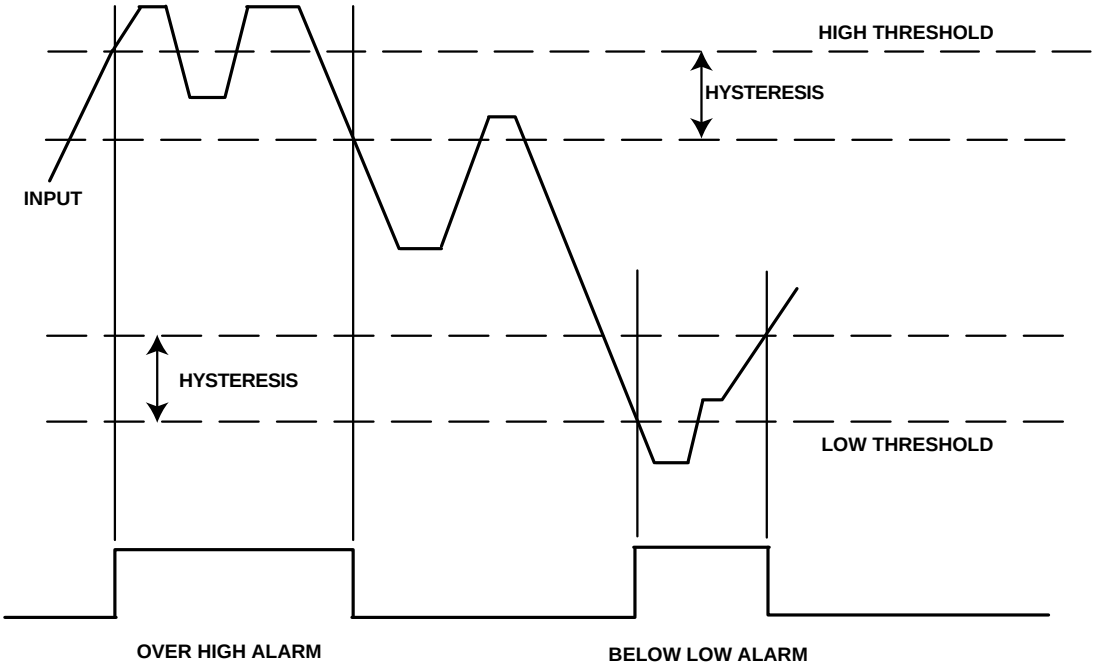


Figure 21. Hysteresis

Table 7. N FOR FALSE ALARM PROTECTION OF CH−n

CH−FALR−CT−2	CH−FALR−CT−1	CH−FALR−CT−0	N
0	0	0	1
0	0	1	4
0	1	0	8
0	1	1	16 (default)
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Table 8. N FOR FALSE ALARM PROTECTION OF TEMPERATURE CHANNELS

CH−FALR−CT−2	CH−FALR−CT−1	CH−FALR−CT−0	N
0	0	0	1
0	1	1	2
1	0	0	8 (default)
1	1	1	8

GPIOs Handling

The NCD9812 has eight GPIO pins. The GPIO−0, −1, −2 and −3 pins are dedicated to general, bidirectional, digital I/O signals. GPIO−4, GPIO−5, GPIO−6 and GPIO−7 are dual−function pins and can be programmed as either bidirectional digital I/O pins or remote temperature sensors D1 and D2. When D1 or D2 is disabled, the pins work as a GPIO. Disabling D1 enables GPIO6−7 and disabling D2 enables GPIO4−5.

These pins can receive an input or produce an output. When the GPIO−*n* pin acts as an output, it has an open−drain, and the status is determined by the corresponding GPIO−*n* bit of the GPIO Register. The output state is high impedance when the GPIO−*n* bit is set to '1', and is logic low when the GPIO−*n* bit is cleared ('0').

Note that a 10 kΩ pull−up resistor is required when using the GPIO−*n* pin as an output. The dual function GPIO−4, −5, −6 and −7 pins should not be tied to a pull−up voltage that exceeds the AVDD supply. The dedicated GPIO−0, −1, −2 and −3 pins are only restricted by the absolute maximum voltage. To use the GPIO−*n* pin as an input, the corresponding GPIO−*n* bits in the GPIO Register must be set to '1'. When the GPIO−*n* pin acts as input, the digital value on the pin is acquired by reading the corresponding GPIO−*n* bit. After a power−on reset or any forced hardware or software reset, all GPIO−*n* bits are set to '1', and the GPIO−*n* pin goes to a high impedance state.

Communication

There are two communication interfaces on the NCD9812. On power−up you must select which interface you intend on using. This is done via the BUS_SEL pin. Grounding this pin selects the I^2C interface while setting it to V_{DD} will select the SPI interface. The table below shows the pins related to each interface.

Table 9. COMMUNICATION PIN CONFIGURATION

BUS_SEL State	GND	V_{DD}
Pin no.	**I^2C**	**SPI**
4	SDA	SDI
5	SCL	SCLK
9	ADD1	/CS
10	ADD0	SDO
11	ADD2	ADD2

Serial Bus Interface – I^2C

Control of the NCD9812 is carried out via the I^2C bus. The NCD9812 is connected to this bus as a slave device, under the control of a master device. The NCD9812 has a 7−bit serial bus address. The upper 3 bits of the device address are fixed at '010'. The lower four bits are set by the state of pins 9, 10 and 11. The address pins are sampled only at power−up, so any changes made while power is on will have no effect.

Table 10. ADDRESS SELECTION

ADD0	ADD1	ADD2	Device Address
0	0	0	110 0001 (0x61)
0	0	1	110 0010 (0x2C)
0	1	0	110 0100 (0x64)
0	1	1	110 0101 (0x2E)
1	0	0	010 1100 (0x62)
1	0	1	010 1101 (0x2D)
1	1	0	010 1110 (0x65)
1	1	1	010 1111 (0x2F)

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high−to−low transition on the serial data line SDA while the serial clock line, SCL, remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next eight bits, consisting of a 7−bit address (MSB first) plus an R/W bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0, the master will write to the slave device. If the R/W bit is a 1, the master will read from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low−to−high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is

determined at the beginning and cannot subsequently be changed without starting a new operation. In the case of the NCD9812, write operations contain two bytes, and read operations contain two bytes and perform the following functions. To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed, and then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register. The device address is sent over the bus followed by R/W set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.

Read a Single Word

The master device asserts the start condition. The master then sends the 7−bit NCD9812 slave address. It is followed by an R/W bit that indicates the direction of operation, which will be a write operation in this case. The slave whose address is on the bus acknowledges it by an ACK signal on the bus (by holding SDA line low). The master then sends register address on the bus. The NCD9812 accepts it by an ACK. The master then asserts a repeated start condition followed by a 7−bit slave address. The master then sends a direction bit R/W which is Read for this case. NCD9812 acknowledges it by an ACK signal on the bus. This will start the read operation and NCD9812 sends the high byte of the register on the bus. Master reads the high byte and asserts an ACK on the SDA line. NCD9812 now sends the low byte of the register on the SDA line. The master acknowledges it by a no acknowledge NACK on the SDA line. The master then asserts the stop condition to end the transaction.

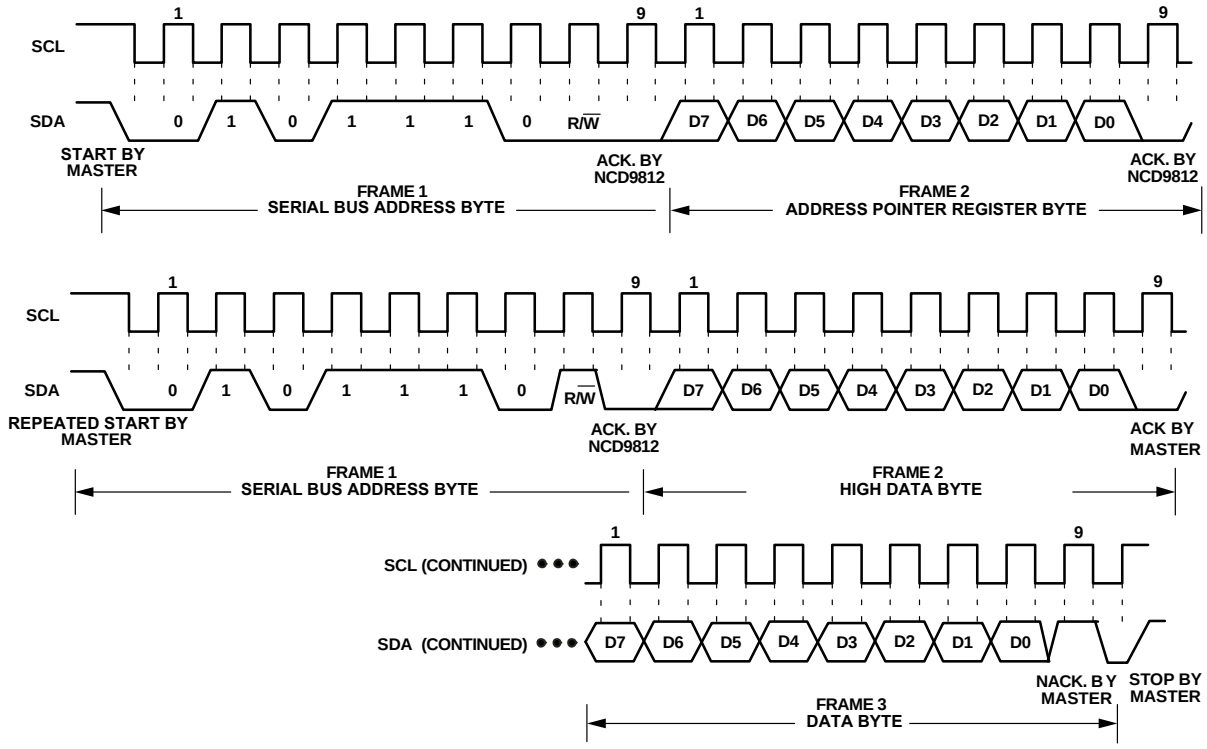


Figure 22. Read a Single Word

Reading the Same Register Multiple Times

The master device asserts the start condition. The master then sends the 7−bit NCD9812 slave address. It is followed by an R/W bit that indicates the direction of operation, which will be a write operation in this case. The slave whose address is on the bus acknowledges it by an ACK signal on the bus (by holding SDA line low). The master then sends register address on the bus. The NCD9812 accepts it by an ACK. The master then asserts a repeated start condition followed by a 7−bit slave address. The master then sends a direction bit R/W which is Read for this case. NCD9812 acknowledges it by an ACK signal on the bus. This will start the read operation

1. The NCD9812 sends the high byte of the register on the bus.
2. The master reads the high byte and asserts an ACK on the SDA line.
3. The NCD9812 now sends the low byte of the register on the SDA line.
4. The master acknowledges it by an ACK signal on the SDA line.

The master and NCD9812 keeps on repeating the steps 1−4 until the low byte of the last reading is transferred. After receiving the low byte of the last register, the master asserts a not acknowledge NACK on the SDA. The master then asserts a stop condition to end the transaction.

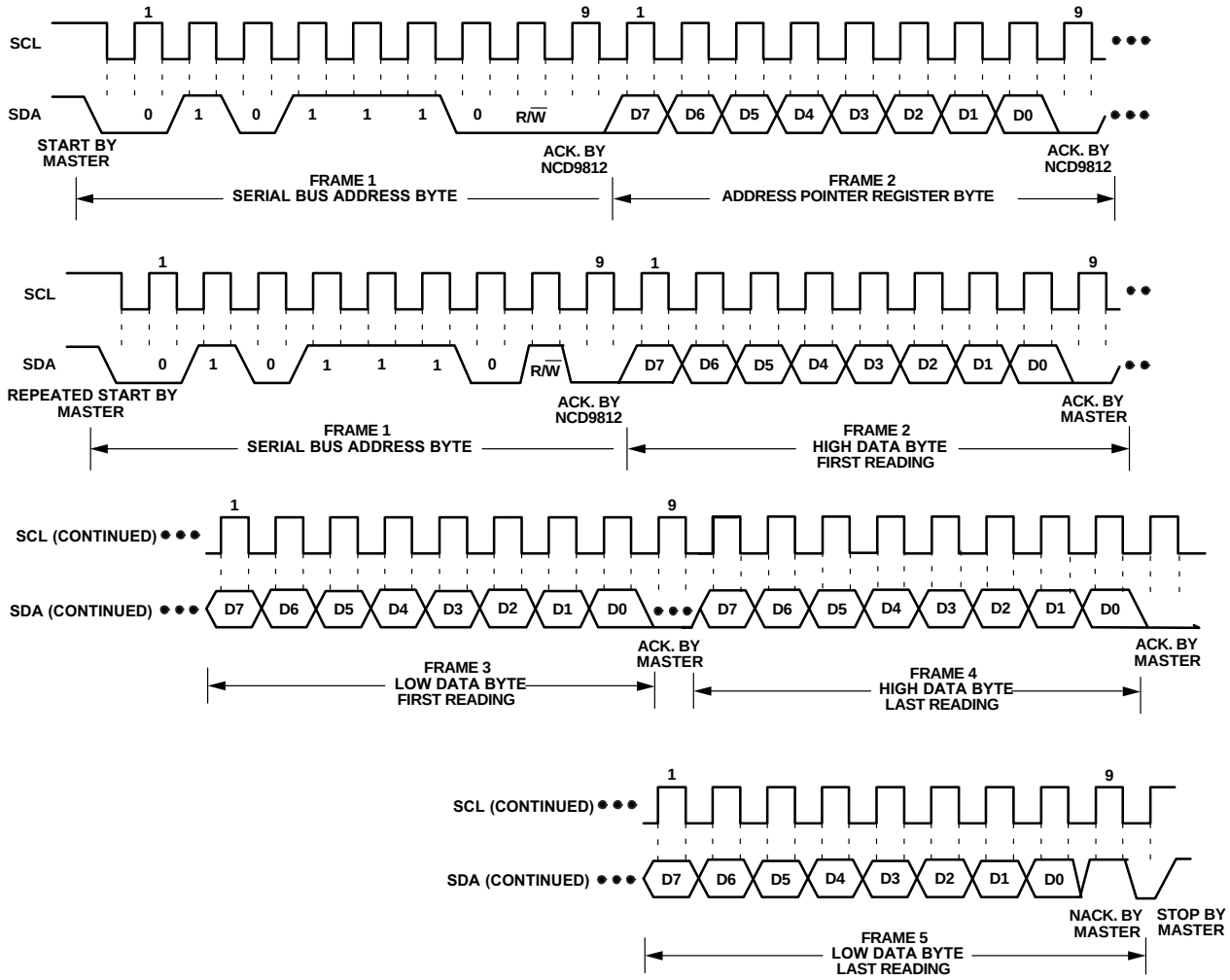


Figure 23. Read Multiple Words

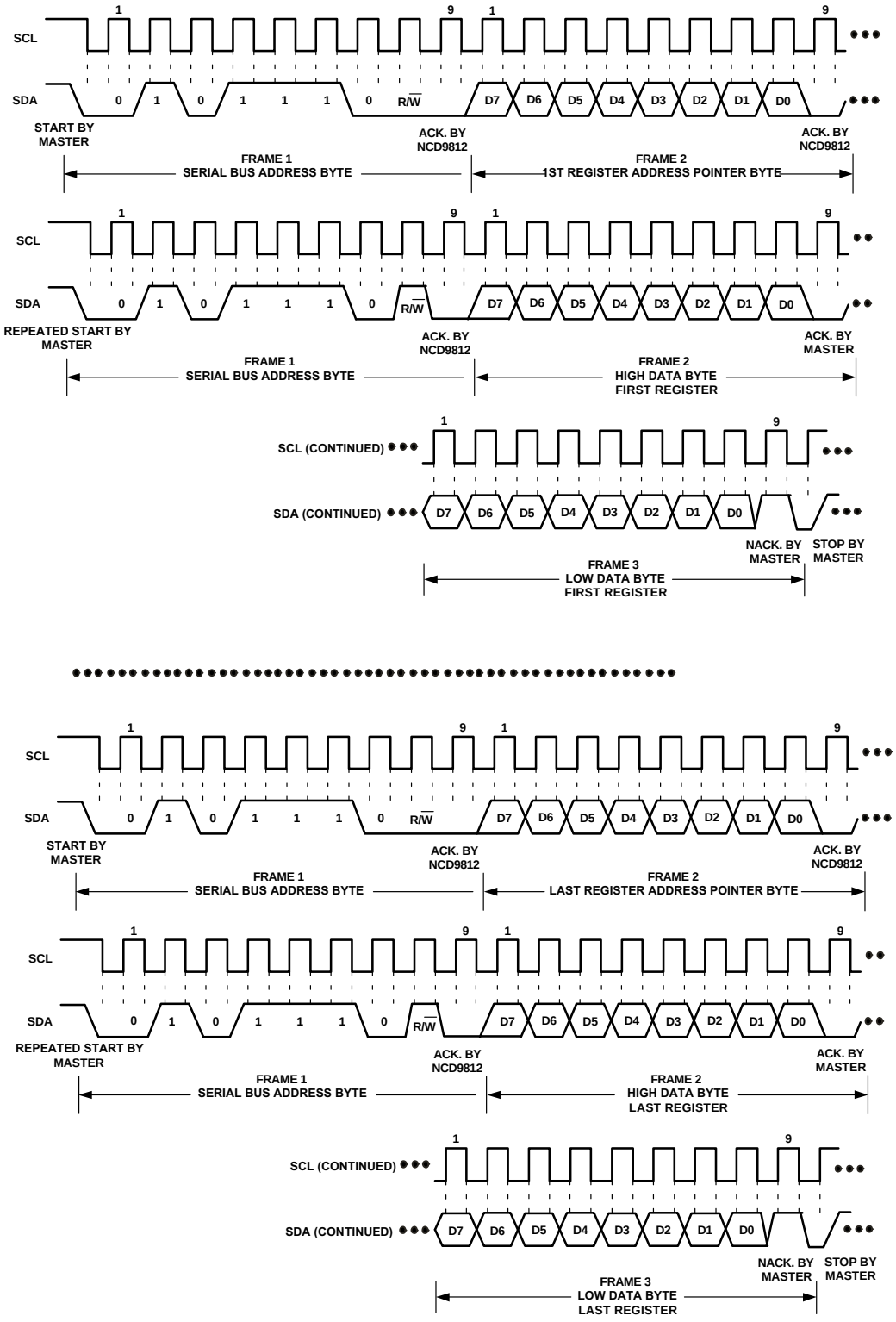


Figure 24. Read Multiple Registers Using the Reading Single Word from any Register Method

Writing a Single Word

The master device asserts the start condition. The master then sends the 7−bit NCD9812 slave address. It is followed by an R/W bit that indicates the direction of operation, which will be a write operation in this case. The slave whose address is on the bus acknowledges it by an ACK signal on the bus (by holding SDA line low). The master then sends register address on the bus. The NCD9812 accepts it by an ACK. The master then sends a data byte of the high byte of the register. The NCD9812 asserts an acknowledge ACK on the SDA line. The master then sends a data byte of the low byte of the register. The NCD9812 asserts an acknowledge ACK on the SDA line. The master asserts a stop condition to end the transaction.

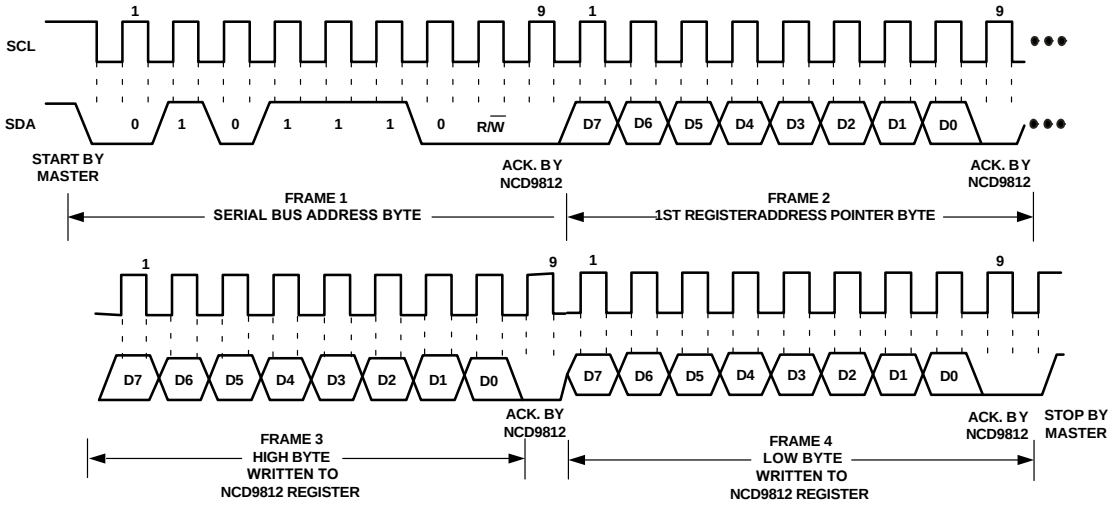


Figure 25. Writing a Single Byte

Writing Multiple Words to Different Registers

The master device asserts the start condition. The master then sends the 7−bit NCD9812 slave address. It is followed by an R/W bit that indicates the direction of operation, which will be a write operation in this case. The slave whose address is on the bus acknowledges it by an ACK signal on the bus (by holding SDA line low).

1. The master then sends first register address on the bus. The NCD9812 accepts it by an ACK. The master then sends a data byte of the high byte of the first register. The NCD9812 asserts an acknowledge ACK on the SDA line. The master then sends a data byte of the low byte of the first register. The NCD9812 asserts an acknowledge ACK on the SDA line.
2. The master then sends the second register address on the bus. The NCD9812 accepts it by an ACK. The master then sends a data byte of the high byte of the second register. The NCD9812 asserts an acknowledge ACK on the SDA line. The master then sends a data byte of the low byte of the second register. The NCD9812 asserts an acknowledge ACK on the SDA line.

A complete word must be written to a register for proper operation. It means that both high and low bytes must be written.

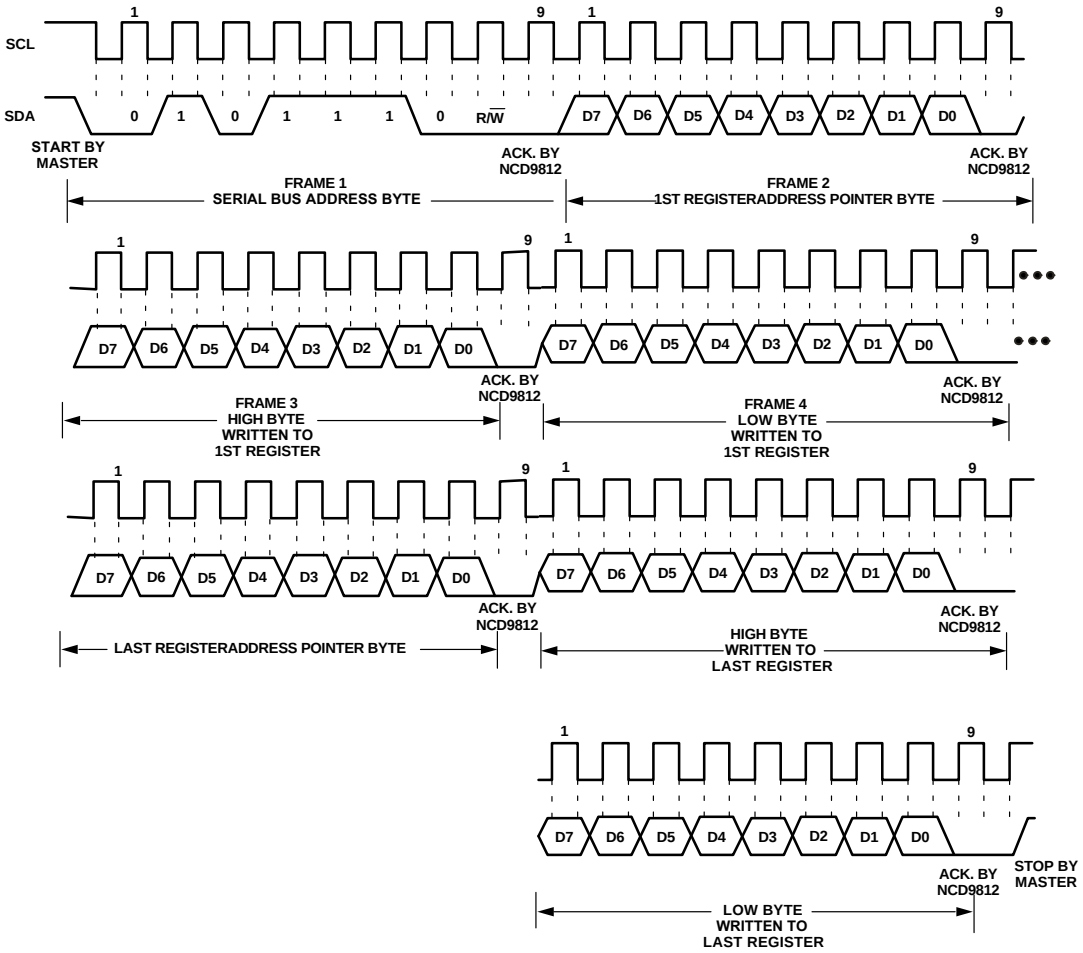


Figure 26. Writing to Multiple 16−bit Registers

Serial Peripheral Interface − SPI

The SPI interface is capable of faster communication as compared to I2C. The faster data speed is achieved at the expense of two additional data lines that can make the circuit denser.

The SPI interface consists of 4 wires:

/CS: Chip select input of the device. A slave device is selected for communicaiton by a high to low transition on this line.

SCLK: Clock input to synchronize data transfer on the SPI bus. NCD9812 is capable of clock speeds of up to 50 MHz. The clock polarity is configured by the host.

SDI and SDO: The data is received on the SDI line where as data is transmitted from SDO line simultaneously.

When /CS is high, the SCLK and SDI signals are blocked out and the SDO line is in a high−impedance state.

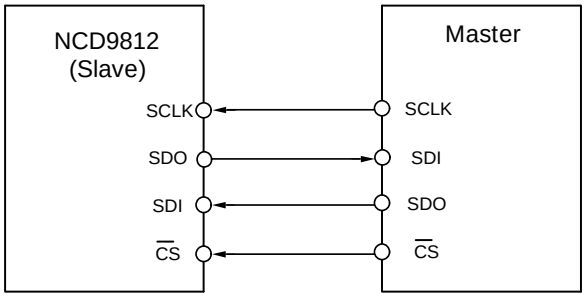


Figure 27. SPI Interface between Master and NCD9812 (Slave)

Shift Register

A 24 bit shift register is available for SPI interface communication. NCD9812 is selected by the host producing a high to low transition on /CS input. This transition starts the transfer of 24 bit data in to the device shift register which is synchronized with the serial clock input SCLK. The clock signal can be either continuous or discontinuous depending on the requirement of the communication cycle. NCD9812 needs to be selected by the host (/CS remains low) for correct number of clock cycles during a continuous SCLK operation. Failing to do so will violate the communication protocol and corrupt the data. Similarly the /CS signal must have a low to high transition after the final clock cycle. This will transfers the contents of shift register in to the corresponding internal registers of the device.

A 24 bit communication cycle is required for Read and Write operation on the SPI interface. The bit structures of these operations are shown in Table 11.

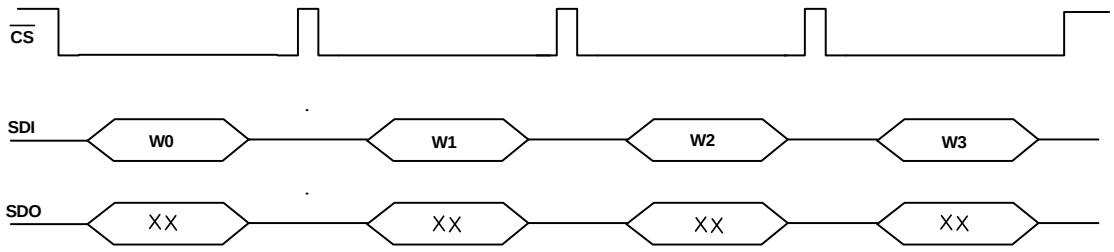
Table 11. 24−BIT WORD STRUCTURE FOR R/W OPERATION

Operation	I/O	Bit 23 (R/W)	NCD9812 Register Address [22:16]	Data Byte
Write	SDI	0	7 bit register address [6:0]	Data to be written [15:0]
	SDO	U	U	U
Read frame 1	SDI	1	7 bit register address [6:0]	x
	SDO	U	Data is undefined	U
Read frame 2	SDI	1	7 bit register address [6:0]	x
	SDO	U	U	Data for address in frame 1

NOTE: x = Don't care
U = Undefined or data depending on previous frame

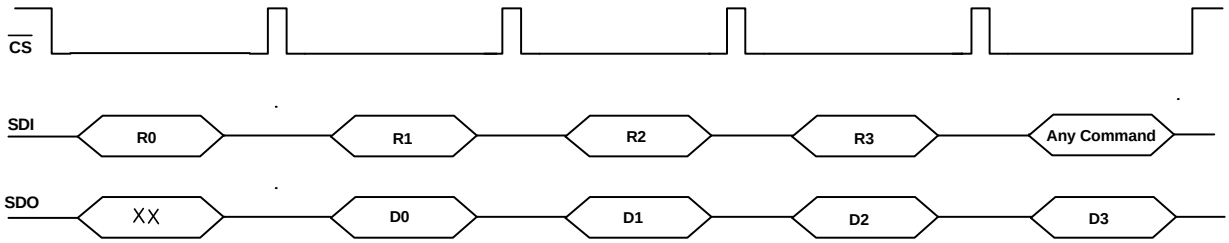
Single NCD9812 on SPI Bus

As discussed above the communication is triggered by a high to low transition on /CS input. The /CS needs to be low for exactly 24 clock cycles for correct data operation. The /CS must go high after the falling edge of 24th clock cycle to transfer the data from the shift register in to device's internal registers. The said transfer is initiated at the rising edge of /CS.



XX = Don't care
Wn = Write Command for Register n

Figure 28. Single NCD9812 Write Operation



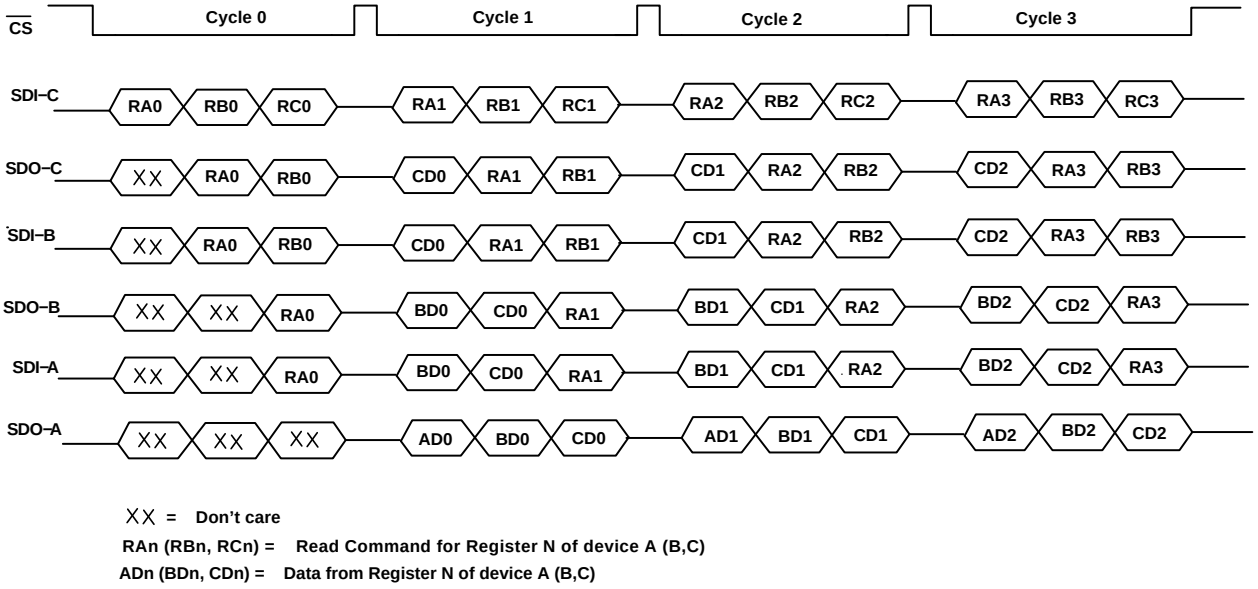
XX = Don't care
Rn = Read Command for Register n
Dn = Data from Register n

Figure 29. Single NCD9812 Read Operation

Multiple NCD9812 on SPI Bus

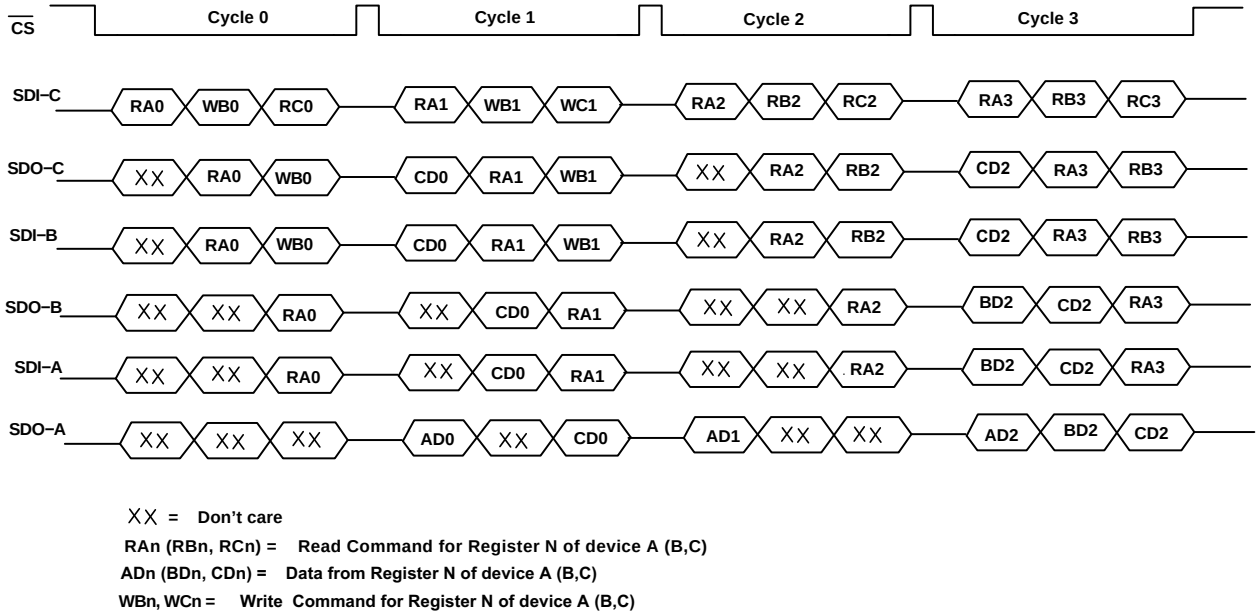
When multiple NCD9812 are used on the same SPI bus then the interface lines can be reduced by connecting the SDO output of the first device to the SDI input of the next device. In this way a chain of multiple NCD9812 is made where each device requires 24 clock pulses for data transfer. The total number of the required clock cycles is equal to 24**N*, where *N* is the number of devices in the chain.

The clock can be continuous or discontinuous. If a continuous clock operation is selected then the /CS input must be low for the exact number of clock cycles for proper data transfer. A discontinuous clock on the other hand comprises of exact number of clocks required to complete the data transfer to all the devices in the chain. Communication is triggered by a high to low transition on /CS input. All the devices on the bus are selected as every device shares a common /CS line. The data is transferred in to the first NCD9812 at the falling edge of /CS. After 24 clock cycles the data transferred to the first device is completed. However, as the clock keeps coming therefore, the data is rippled out of the shift register at the rising edge of the 25th clock and appear on the SDO line at the falling edge. The SDO of the first device is connected to SDI line of the next NCD9812. In this way data is transferred to all the devices on the bus. The /CS must go high after the data transfer is completed to latch the data from the shift registers in to the device's internal registers.



XX = Don't care
RAn (RBn, RCn) = Read Command for Register N of device A (B,C)
ADn (BDn, CDn) = Data from Register N of device A (B,C)

Figure 30. Reading Multiple Registers



XX = Don't care
RAn (RBn, RCn) = Read Command for Register N of device A (B,C)
ADn (BDn, CDn) = Data from Register N of device A (B,C)
WBn, WCn = Write Command for Register N of device A (B,C)

Figure 31. Mixed Operation: Reading Devices A and C, and Writing to Device B; then Reading A, and Writing to B and C; then Reading A, B and C Twice

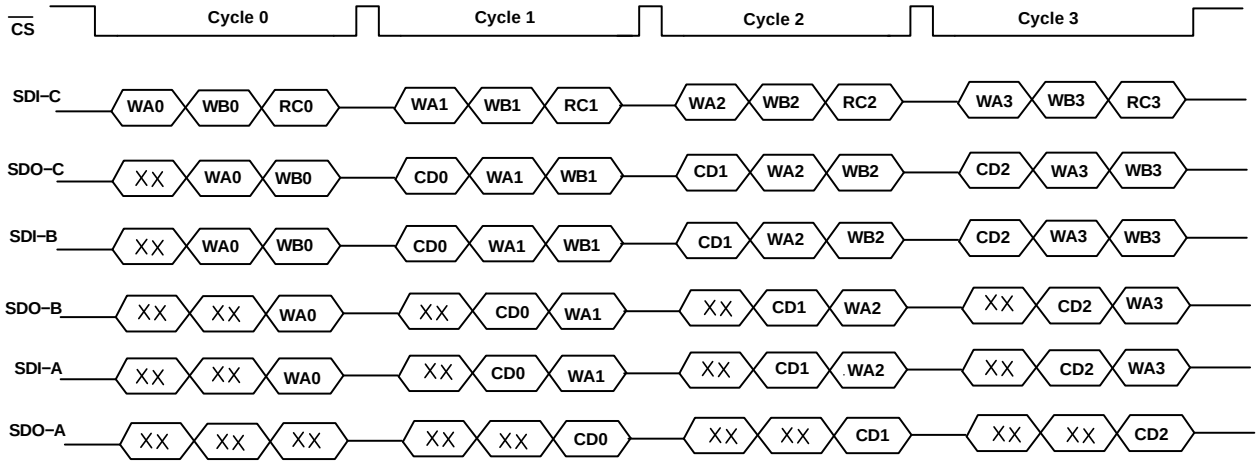


Figure 32. Writing to Devices A and B, and Reading Device C

Table 12. NCD9812 REGISTER MAP

Register Name	Type	Width	Reset Value	Address Offset
Local−Temperature−Data	R	16	0x0000	0x00
Remote1−Temperature−Data	R	16	0x0000	0x01
Remote2−Temperature−Data	R	16	0x0000	0x02
Temperature Configuration	RW	16	0x003C	0x0A
Temperature Conversion Rate	RW	16	0x0007	0x0B
n-Factor Correction (for Remote1)	RW	16	0x0000	0x21
n-Factor Correction (for Remote2)	RW	16	0x0000	0x22
ADC−0−Data	R	16	0x00	0x23
ADC−1−Data	R	16	0x00	0x24
ADC−2−Data	R	16	0x00	0x25
ADC−3−Data	R	16	0x00	0x26
ADC−4−Data	R	16	0x00	0x27
ADC−5−Data	R	16	0x00	0x28
ADC−6−Data	R	16	0x00	0x29
ADC−7−Data	R	16	0x00	0x2A
ADC−8−Data	R	16	0x00	0x2B
ADC−9−Data	R	16	0x00	0x2C
ADC−10−Data	R	16	0x00	0x2D
ADC−11−Data	R	16	0x00	0x2E
ADC−12−Data	R	16	0x00	0x2F
ADC−13−Data	R	16	0x00	0x30
ADC−14−Data	R	16	0x00	0x31
ADC−15−Data	R	16	0x00	0x32
DAC−0−Data	RW	16	0x00	0x33
DAC−1−Data	RW	16	0x00	0x34
DAC−2−Data	RW	16	0x00	0x35
DAC−3−Data	RW	16	0x00	0x36
DAC−4−Data	RW	16	0x00	0x37
DAC−5−Data	RW	16	0x00	0x38
DAC−6−Data	RW	16	0x00	0x39
DAC−7−Data	RW	16	0x0000	0x3A
DAC−8−Data	RW	16	0x0000	0x3B
DAC−9−Data	RW	16	0x0000	0x3C
DAC−10−Data	RW	16	0x0000	0x3D
DAC−11−Data	RW	16	0x0000	0x3E
DAC−0−CLR−Setting	RW	16	0x0000	0x3F
DAC−1−CLR−Setting	RW	16	0x0000	0x40
DAC−2−CLR−Setting	RW	16	0x0000	0x41
DAC−3−CLR−Setting	RW	16	0x0000	0x42
DAC−4−CLR−Setting	RW	16	0x0000	0x43
DAC−5−CLR−Setting	RW	16	0x0000	0x44
DAC−6−CLR−Setting	RW	16	0x0000	0x45

Table 12. NCD9812 REGISTER MAP

Register Name	Type	Width	Reset Value	Address Offset
DAC−7−CLR−Setting	RW	16	0x0000	0x46
DAC−8−CLR−Setting	RW	16	0x0000	0x47
DAC−9−CLR−Setting	RW	16	0x0000	0x48
DAC−10−CLR−Setting	RW	16	0x0000	0x49
DAC−11−CLR−Setting	RW	16	0x0000	0x4A
GPIO	RW	16	0x000F	0x4B
Configuration 0	RW	16	0x2000	0x4C
Configuration 1	RW	16	0x0070	0x4D
Alarm Control	RW	16	0x0000	0x4E
Status	R	16	0x0000	0x4F
ADC Channel 0	RW	16	0x0000	0x50
ADC Channel 1	RW	16	0x0000	0x51
ADC Gain	RW	16	0xFFFF	0x52
AUTO−DAC−CLR−SOURCE	RW	16	0x0004	0x53
AUTO−DAC−CLR−EN	RW	16	0x0000	0x54
SW−DAC−CLR	RW	16	0x0000	0x55
HW−DAC−CLR−EN−0	RW	16	0x0000	0x56
HW−DAC−CLR−EN−1	RW	16	0x0000	0x57
DAC Configuration	RW	16	0x0000	0x58
DAC Gain	RW	16	0x0000	0x59
Input−0−High−Threshold	RW	16	0x0FFF	0x5A
Input−0−Low−Threshold	RW	16	0x0000	0x5B
Input−1−High−Threshold	RW	16	0x0FFF	0x5C
Input−1−Low−Threshold	RW	16	0x0000	0x5D
Input−2−High−Threshold	RW	16	0x0FFF	0x5E
Input−2−Low−Threshold	RW	16	0x0000	0x5F
Input−3−High−Threshold	RW	16	0x0FFF	0x60
Input−3−Low−Threshold	RW	16	0x0000	0x61
Local−High−Threshold	RW	16	0x07FF	0x62
Local−Low−Threshold	RW	16	0x0800	0x63
Remote1−High−Threshold	RW	16	0x07FF	0x64
Remote1−Low−Threshold	RW	16	0x0800	0x65
Remote2−High−Threshold	RW	16	0x07FF	0x66
Remote2−Low−Threshold	RW	16	0x0800	0x67
Hysteresis−0	RW	16	0x0810	0x68
Hysteresis−1	RW	16	0x0810	0x69
Hysteresis−2	RW	16	0x2108	0x6A
Power−Down	RW	16	0x0000	0x6B
Device ID	R	16	0x1220	0x6C
Software Reset	RW	16	N/A	0x7C
MANUFACTURE_ID	R	16	001A	0x7E

Table 13. LOCAL TEMPERATURE REGISTER

Register Information			
Description	Stores the local temperature sensor readings in 2's complement data format.		
Offset	0x00	**Type:**	R

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:4	Local_15:Local_4	Local temperature bit 15 to bit 4	R	0x00			
3:0	Reserved		R	0x0			

Table 14. REMOTE1 SENSOR TEMPERATURE REGISTER

Register Information			
Description	Stores the Remote1 temperature sensor readings in 2's complement data format.		
Offset	0x01	**Type:**	R

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:4	Remote1_15:Remote1_4	Remote1 temperature bit 15 to bit 4	R	0x000			
3:0	Reserved		R	0x0			

Table 15. REMOTE2 SENSOR TEMPERATURE REGISTER

Register Information			
Description	Stores the Remote2 temperature sensor readings in 2's complement data format.		
Offset	0x02	**Type:**	R

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:4	Remote2_15:Remote2_4	Remote2 temperature bit 15 to bit 4	R	0x00			
3:0	Reserved		R	0x0			

Table 16. TEMPERATURE CONFIGURATION REGISTER (Using Default SPI Value 003Ch)

Register Information			
Description	To configure the Temperature channels		
Offset	0x0A	**Type:**	RW

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:6	Bit_15:Bit_6			0x00			
5	Bit_5	Remote sensor 2 is enabled/disabled (1/0)	R/W	1			
4	Bit_4	Remote sensor 1 is enabled/disabled (1/0)	R/W	1			
3	Bit_3	Local sensor is enabled/disabled (1/0)	R/W	1			
2	Bit_2	RC bit	R/W	1			
1:0	Bit_1:Bit_0			00			

Table 17. TEMPERATURE CONFIGURATION REGISTER (Using I²C Default Value 3CFFh)

Register Information			
Description	To configure the Temperature channels		
Offset	0x0A*	**Type:**	RW

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:14	Bit_15:Bit_14			0x00			
13	Bit_13	Reserved	R/W	1			
12	Bit_12	Reserved	R/W	1			
11	Bit_11	Reserved	R/W	1			
10	Bit_10	RC bit	R/W	1			
9:8	Bit_9:Bit_8		R	00			
7:0	Bit_7:Bit_0		R	0xFF			

*After configuring this register in I²C mode its value changes to 3CFFh

Table 18. TEMPERATURE CONVERSION RATE REGISTER (Using Default SPI Mode)

Register Information			
Description	Register to set the conversion rate of temperature		
Offset	0x0B	**Type:**	RW

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:3	Reserved		R	0x0			
2		Conversion Rate bit 2, R2	R/W	1			
1		Conversion Rate bit 1, R1	R/W	1			
0		Conversion Rate bit 0, R0	R/W	1			

Table 19. TEMPERATURE CONVERSION RATE REGISTER (Using I²C Mode with Default Value of 07FFh)

Register Information			
Description	Register to set the conversion rate of temperature		
Offset	0x0B*	**Type:**	RW

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:11	Reserved		R	0x0			
10		Conversion Rate bit 2, R2	R/W	1			
9		Conversion Rate bit 1, R1	R/W	1			
8		Conversion Rate bit 0, R0	R/W	1			
7:0	Reserved		R	0xFF			

*

Table 20. TEMPERATURE CONVERSION TIME

R2	R1	R0	Conversion Time
0	0	0	128 × Minimum cycle Time
0	0	1	64 × Minimum cycle Time
0	1	0	32 × Minimum cycle Time
0	1	1	16 × Minimum cycle Time
1	0	0	8 × Minimum cycle Time
1	0	1	4 × Minimum cycle Time
1	1	0	2 × Minimum cycle Time
1	1	1	Minimum cycle Time

Table 21. TEMPERATURE MONITORING CYCLE TIME

Temperature Sensor Status	Monitoring Cycle Time
Local sensor is active, remote sensors are disabled or in power−down.	15 ms
One remote sensor is active and RC = ‘0’, local sensor and one remote sensor are disabled or in power−down.	44 ms
One remote sensor is active and RC = ‘1’, local sensor and one remote sensor are disabled or in power−down.	93 ms
One remote sensor and local sensor are active and RC = ‘0’, one remote sensor is disabled or in power−down.	59 ms
One remote sensor and local sensor are active and RC = ‘1’, one remote sensor is disabled or in power−down.	108 ms
Two remote sensors are active and RC = ‘0’, local sensor is disabled or in power−down.	88 ms
Two remote sensors are active and RC = ‘1’, local sensor is disabled or in power−down.	186 ms
All sensors are active and RC = ‘0’.	103 ms
All sensors are active and RC = ‘1’.	201 ms

Table 22. n−FACTOR CORRECTION REGISTERS (SPI Default Value of 0x0000)

Register Information			
Description	Registers for n Factor Correction		
Offset	0x21 and 0x22	**Type:**	RW

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:8	Bit_15:Bit_8	Reserved	RW	0x00			
7:0	Bit_7:Bit_0	Used for n Factor correction	RW	0x00			

Table 23. n−FACTOR CORRECTION REGISTERS (I^2C Default Value of 0x00FF)

Register Information			
Description	Registers for n Factor Correction		
Offset	0x21 and 0x22	**Type:**	RW

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:8	Bit_15:Bit_8	Used for n Factor correction	RW	0x00			
7:0	Bit_7:Bit_0	Reserved	RW	0xFF			

The N_{ADJUST} value for ideality correction is stored as shown in Table 19. n_{EFF} is the actual ideality of the transistor being used. Refer to the *Ideality Factor* section for more details.

Table 24. N_{ADJUST} & n_{EFF} VALUES

N_{ADJUST}			n_{EFF}
BINARY	**HEX**	**DECIMAL**	
0111 1111	7F	127	1.747977
0000 1010	0A	10	1.042759
0000 1000	08	8	1.035616
0000 0110	06	6	1.028571
0000 0100	04	4	1.021622
0000 0010	02	2	1.014765
0000 0001	01	1	1.011371
0000 0000	00	0	1.008 (Default)
1111 1111	FF	–1	1.004651
1111 1110	FE	–2	1.001325
1111 1100	FC	–4	0.994737
1111 1010	FA	–6	0.988235
1111 1000	F8	–8	0.981818
1111 0110	F6	–10	0.975484
1000 0000	80	−128	0.70654

Table 25. ADC−n−DATA REGISTERS

Register Information			
Description	Registers to store ADC data		
Offset	0x23 and 0x32	**Type:**	R

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0x0			
11:0	Bit_11:Bit_0	12 Bit ADC data	R	0x000			

The ADC−n−Data Registers store the conversion results of the corresponding Analog channel−n

Table 26. ADC DATA REGISTER DEFINITIONS

Channel	Input Type	Destination Register	Format
Channel 0	Single Ended	ADC_0_Data Register	Straight Binary
Channel 1	Single Ended	ADC_1_Data Register	Straight Binary
Channel 2	Single Ended	ADC_2_Data Register	Straight Binary
Channel 3	Single Ended	ADC_3_Data Register	Straight Binary
CH0+/CH1−	Differential	ADC_0_Data Register	2's Complement
CH2+/CH3−	Differential	ADC_2_Data Register	2's Complement
Channel 4	Single Ended	ADC_4_Data Register	Straight Binary
Channel 5	Single Ended	ADC_5_Data Register	Straight Binary
Channel 6	Single Ended	ADC_6_Data Register	Straight Binary
Channel 7	Single Ended	ADC_7_Data Register	Straight Binary

Table 26. ADC DATA REGISTER DEFINITIONS

Channel	Input Type	Destination Register	Format
Channel 8	Single Ended	ADC_8_Data Register	Straight Binary
Channel 9	Single Ended	ADC_9_Data Register	Straight Binary
Channel 10	Single Ended	ADC_10_Data Register	Straight Binary
Channel 11	Single Ended	ADC_11_Data Register	Straight Binary
Channel 12	Single Ended	ADC_12_Data Register	Straight Binary
Channel 13	Single Ended	ADC_13_Data Register	Straight Binary
Channel 14	Single Ended	ADC_14_Data Register	Straight Binary
Channel 15	Single Ended	ADC_15_Data Register	Straight Binary

Table 27. DAC−n−DATA REGISTERS

Register Information			
Description	Registers to store DAC input data. Each DAC has a DAC register to store data that is loaded to DAC latches.		
Offset	0x33 and 0x3E	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0x0			
11:0	Bit_11:Bit_0	12 Bit DAC output data	R	0x000			

Table 28. DAC−n−CLR−SETTING REGISTERS

Register Information			
Description	Registers to store data to be loaded in the DAC latch when DAC is cleared.		
Offset	0x3F and 0x4A	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0x0			
11:0	Bit_11:Bit_0	12 Bit DAC latch data	R	0x000			

Table 29. DAC−n−CLR−SETTING REGISTERS

Register Information			
Description	Registers to store data to be loaded in the DAC latch when DAC is cleared.		
Offset	0x3F and 0x4A	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0x0			
11:0	Bit_11:Bit_0	12 Bit DAC latch data	R/W	0x000			

Table 30. GIO REGISTER

Register Information			
Description	For write operations, the GPIO pin operates as an output. Writing a ‘1’ to the GPIO−*n* bit sets the GPIO−*n* pin to high impedance. Writing a ‘0’ sets the GPIO−*n* pin to logic low. An external pull−up resistor is required when using the GPIO pin as an output. For read operations, the GPIO pin operates as an input. Read the GPIO−*n* bit to receive the status of the GPIO−*n* pin. Reading a ‘0’ indicates that the GPIO−*n* pin is low; reading a ‘1’ indicates that the GPIO−*n* pin is high. After power−on reset, or any forced hardware or software reset, the GPIO−*n* bit is set to ‘1’ and is in a high impedance state. When REMOTE2 is enabled, GPIO−4 and GPIO−5 are ignored. When REMOTE1 is enabled, GPIO−6 and GPIO−7 are ignored.		
Offset	0x4B	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:8	Bit_15:Bit_8	Reserved	R	0x00			
7:0	Bit_7:Bit_0	GPIO7:GPIO0	R/W	0x0F			

Table 31. CONFIGURATION REGISTER 0

Register Information			
Description	Configuration Register 0 of NCD9812		
Offset	0x4C	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:14	Bit_15:Bit_12	Reserved	R	0x0			
13	CMODE		R/W	1			ADC Conversion Mode Bit. This bit selects between the two operating conversion modes (direct or auto). CMODE = ‘0’: Direct mode. The analog inputs specified in the ADC Channel Registers are converted sequentially (see the ADC Channel Registers) one time. When one set of conversions is complete, the ADC is idle and waits for a new trigger. CMODE = ‘1’: Auto mode. The analog inputs specified in the Channel Registers are converted sequentially and repeatedly (see the ADC Channel Registers). When one set of conversions is complete, the ADC multiplexer returns to the first channel and repeats the process. Repetitive conversions continue until the CMODE bit is cleared (‘0’).
12	ICONV		R/W	0			Internal conversion bit Set this bit to ‘1’ to start the ADC conversion internally. The bit is automatically cleared (‘0’) after the ADC conversion starts.
11	ILDAC		R/W	0			Load DAC bit. Set this bit to ‘1’ to synchronously load the DAC Data Registers, which are programmed for synchronous update mode (SLDAC−*n* = 1). The NCD9812 updates the DAC Latch only if the ILDAC bit is set (‘1’), thereby eliminating any unnecessary glitch. Any DAC channels that have not been accessed are not reloaded. When the DAC Latch is updated, the corresponding output changes to the new level immediately. This bit is cleared (‘0’) after the DAC Data Register is updated.

Table 31. CONFIGURATION REGISTER 0

Field	Name	Description	Access	Default	Sim	Bench	Functionality
10	ADC−REF−INT		R/W	0			ADC V_{REF} select bit When this bit = ‘0’, the internal reference buffer is off, and the external reference drives the ADC. When this bit = ‘1’, the internal buffer is on and the internal reference drives the ADC. Note that a compensation capacitor is required.
9	EN−ALARM		R/W	0			Enable /ALARM pin bit. When this bit = ‘0’, the /ALARM pin is disabled. When this bit = ‘1’, the /ALARM pin is enabled.
8		Reserved	R	0			
7	DAVF		R				ADC Data available flag bit. For Direct mode only. Always cleared (set to ‘0’) in Auto mode. DAVF = ‘1’: The ADC conversions are complete and new data are available. DAVF = ‘0’: The ADC conversion is in progress (data are not ready) or the ADC is in Auto mode. In Direct mode, the DAVF bit sets the DAV pin. DAV goes low when DAVF = ‘1’, and goes high when DAVF = ‘0’. In Auto mode, DAVF is always cleared to ’0’. However, a 1 μs pulse (active low) appears on the DAV pin when the last input specified in the ADC Channel Registers is converted. DAVF is cleared to ‘0’ in one of two ways: (1) reading the ADC Data Register, (2) starting a new ADC conversion
6	GALR		R	0			Global alarm bit. This bit is the OR function of all individual alarm bits of the Status Register. This bit is set (‘1’) when any alarm condition occurs, and remains ‘1’ until the Status Register is read. This bit is cleared (‘0’) after reading the Status Register.
5:0	Bit_5:Bit_0	Reserved	R	0x0			

Table 32. CONFIGURATION REGISTER 1

Register Information			
Description	Configuration Register 1 of NCD9812		
Offset	0x4D	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:10	Bit_15:Bit_10	Reserved	R	0x0			
9:8	CONV_RATE_1: CONV_RATE_0		R/W	0			ADC Conversion Bit RATE BIT 0 and 1
7−5	CH_FALR_CT_2: CH_FALR_CT_0		R/W	0X3			False Alarm Protection bits for CH0 to CH3
4−3	TEMP_FALR_CT_1: TEMP_FALR_CT_0		R/W	0X2			False Alarm Protection bits for temperature monitor
2:0	Bit_2:Bit_0	Reserved	R	0			

Table 33. CONVERSION RATE BIT SETTING

CONV_RATE_1	CONV_RATE_0	ADC Conversion Rate
0	0	500 Kbps (Default)
0	1	1/2 of default rate
1	0	1/4 of default rate
1	1	1/8 of default rate

Table 34. CH_FALR_CT BIT SETTING

CH_FALR_CT_2	CH_FALR_CT_1	CH_FALR_CT_0	N Consecutive Samples Before Alarm is Set
0	0	0	1
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Table 35. CONVERSION RATE BIT SETTING

TEMP_FALR_CT_1	TEMP_FALR_CT_0	N Consecutive Samples Before Alarm is Set
0	0	1
0	1	2
1	0	4 (Default)
1	1	8

Table 36. ALARM CONTROL REGISTERS

Register Information			
Description	The Alarm Control Register determines whether the ALARM pin is accessed when a corresponding alarm event occurs.		
Offset	0x4E	**Type:**	RW

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved.	R	0			
14:11	EALR_CH0:EALR_CH3	Alarm bits for CH0 to CH3	RW	0x0			If EALR_CHX = ‘1’, the alarm is enabled, the CHX_ALR bit is set, and the ALARM pin goes low (if enabled) when the input of CHX is out of range. If EALR_CHX = ‘0’, the alarm is masked. When the input of CHX is out of range, the ALARM pin does not go low, but the CHX_ALR bit is set.

Table 36. ALARM CONTROL REGISTERS

Field	Name	Description	Access	Default	Sim	Bench	Functionality
10	EALR_Local_Low:	Local sensor low alarm enable Bit	RW	0			If EALR_Local_Low = ‘1’, the Local_Low alarm is enabled. When LT is below the specified range, the Local_Low_ALR bit is set (‘1’) and the ALARM pin goes low (if enabled). If EALR_Local_Low = ‘0’, the Local−Low alarm is masked. When Local is below the specified range, the ALARM pin does not go low, but the Local−Low−ALR bit is set.
9	EALR_Local_High	Local sensor high alarm enable Bit	RW	0			If EALR_Local_High = ‘1’, the Local_High alarm is enabled. When LT is above the specified range, the Local_High_ALR bit is set (‘1’) and the ALARM pin goes low (if enabled). If EALR_Local_High = ‘0’, the Local_High alarm is masked. When LT is above the specified range, the ALARM pin does not go low, but the LT−High−ALR bit is set.
8	EALR−REMOTE1−Low	REMOTE1 low alarm enable Bit	R/W	0			If EALR_REMOTE1_Low = ‘1’, the REMOTE1_Low alarm is enabled. When REMOTE1 is below the specified range, the REMOTE1_Low_ALR bit is set (‘1’), and the ALARM pin goes low (if enabled). If EALR_REMOTE1_Low = ‘0’, the REMOTE1_Low alarm is masked. When REMOTE1 is below the specified range, the ALARM pin does not go low, but the REMOTE1−Low−ALR bit is set.
7	EALR−REMOTE1−high	REMOTE1 high alarm enable Bit	R/W	0			If EALR_REMOTE1_High = ‘1’, the REMOTE1_High alarm is enabled. When REMOTE1 is above the specified range, the REMOTE1_High_ALR bit is set (‘1’), and the ALARM pin goes low (if enabled). If EALR_REMOTE1_High = ‘0’, the REMOTE1_High alarm is masked. When REMOTE1 is above the specified range, the ALARM pin does not go low, but the REMOTE1_High_ALR bit is set.
6	EALR−REMOTE2−Low	REMOTE2 low alarm enable Bit	R/W	0			If EALR_REMOTE2_Low = ‘1’, the REMOTE2_Low alarm is enabled. When REMOTE2 is below the specified range, the REMOTE2_Low_ALR bit is set (‘1’), and the ALARM pin goes low (if enabled). If EALR_REMOTE2_Low = ‘0’, the REMOTE2_Low alarm is masked. When REMOTE2 is below the specified range, the ALARM pin does not go low, but the REMOTE2−Low−ALR bit is set.

Table 36. ALARM CONTROL REGISTERS

Field	Name	Description	Access	Default	Sim	Bench	Functionality
5	EALR−REMOTE2−high	REMOTE2 high alarm enable Bit	R/W	0			If EALR_REMOTE2_High = ‘1’, the REMOTE2_High alarm is enabled. When REMOTE2 is above the specified range, the REMOTE2_High_ALR bit is set (‘1’), and the ALARM pin goes low (if enabled). If EALR_REMOTE2_High = ‘0’, the REMOTE2_High alarm is masked. When REMOTE2 is above the specified range, the ALARM pin does not go low, but the REMOTE2_High_ALR bit is set
4	EALR_REMOTE1_FAIL	REMOTE1 fail alarm enable Bit.	R/W	0			If EALR_REMOTE1_FAIL = ‘1’, the REMOTE1_Fail alarm is enabled. When REMOTE1 fails, the REMOTE1−FAIL−ALR bit is set (‘1’), the ALARM pin goes low (if enabled). If EALR_REMOTE1−FAIL = ‘0’, the REMOTE1_FAIL alarm is masked. When REMOTE1 fails, the ALARM pin does not go low, but the REMOTE1_FAIL_ALR bit is set
3	EALR_REMOTE2_FAIL	REMOTE1 fail alarm enable Bit.	R/W	0			If EALR_REMOTE2_FAIL = ‘1’, the REMOTE2−Fail alarm is enabled. When REMOTE2 fails, the REMOTE2−FAIL−ALR bit is set (‘1’), the ALARM pin goes low (if enabled). If EALR_REMOTE2_FAIL = ‘0’, the REMOTE2_FAIL alarm is masked. When REMOTE2 fails, the ALARM pin does not go low, but the REMOTE2_FAIL_ALR bit is set
2	ALARM_LATCH_DIS	Alarm latch disable Bit.	R/W	0			When ALARM_LATCH_DIS = ‘1’, the Status Register bits are not latched. When the alarm condition subsides, the alarm bits are cleared regardless of whether the Status Register has been read or not. When ALARM_LATCH_DIS = ‘0’, the Status Register bits are latched. When an alarm occurs, the corresponding alarm bit is set (‘1’). The alarm bit remains ‘1’ until the error condition subsides and the Status Register is read. Before reading, the alarm bit is not cleared (‘0’) even if the alarm condition disappears.
1:0	Reserved		R	0x0			

Table 37. STATUS REGISTERS

Register Information			
Description	The NCD9812 continuously monitors all analog inputs and temperatures during normal operation. When any input is out of the specified range *N* consecutive times; the corresponding alarm bit is set (‘1’). If the input returns to the normal range before *N* consecutive times, the corresponding alarm bit remains clear (‘0’). This configurations avoids any false alarms. When an alarm status occurs, the corresponding alarm bit is set (‘1’). When the ALARM−LATCH−DIS bit in the Alarm Control Register is cleared (‘0’), the ALARM pin is latched. Whenever an alarm status bit is set, it remains set until the event that caused it is resolved and the Status Register is read. **Reading the register will not reset the counter which means if the error remains after the status register is read, then the status bit will not be cleared.**		
Offset	0x4F	**Type:**	R

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved.	R	0			
14:11	CH0_ALR:CH3_ALR		R	0x0			CHX_ALR = ‘1’ when single−ended channel X (or differential input pair incase of CH0+/CH1−) is out of the range defined by the corresponding threshold registers. CHX_ALR = ‘0’ when the analog input is not out of the specified range.
10:9	Local_Low_ALR: Local_High_ALR	Local temperatures under range and over range Bits.	R	0X0			These bit are only checked when Local is enabled (EN_Local= ‘1’); it is ignored when EN_Local = ‘0’.
8:7	REMOTE1_Low_ALR: REMOTE1_High_ALR	REMOTE1 remote temperatures under range and over range Bits.	R	0x0			These bit are only checked when REMOTE1 is enabled (EN_REMOTE1 = ‘1’); it is ignored when EN_REMOTE1 = ‘0’.
6:5	REMOTE1_Low_ALR: REMOTE1_High_ALR	REMOTE2 remote temperatures under range and over range Bits.	R	0x0			These bit are only checked when REMOTE2 is enabled (EN_REMOTE2 = ‘1’); it is ignored when EN_REMOTE2 = ‘0’.
4:3	REMOTE1_FAIL_ALR: REMOTE2_FAIL_ALR	Remote sensors REMOTE1 and REMOTE2 failure flags	R	0X0			DX_FAIL_ALR=‘1’ when the sensor is open circuit or short circuit, it is 0 under normal circumstances. These bits are only checked when corresponding sensors (REMOTE1 or REMOTE2) are enabled and ignored otherwise.
2	THERM_ALR	Thermal alarm flag.	R	0			When the die temperature is equal to or greater than +150°C, the bit is set (‘1’) and the THERM_ALR flag activates. The on−chip temperature sensor (LT) monitors the die temperature. If LT is disabled, the THERM_ALR bit is always ‘0’. The hysteresis of this alarm is 8°C.
1:0	Reserved		R	0x0			

Table 38. ADC CHANNEL REGISTER 0

Register Information			
Description	These bits specify the external analog auxiliary input channels (CH0 to CH12) to be converted. The specified channel(s) is accessed sequentially in order from bit 14 to bit 0. The input is converted when the corresponding bit is set (‘1’).		
Offset	0x50	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved.	R	0			
14:13	SE0:SE1	External single−ended analog input for CH0 & CH1.	R/W	0x0			The result is stored in ADC−n−Data register in 2’s complement.
12	DF(CH0+/CH1−)	External analog differential input pair, CH0 and CH1, with CH0 as positive and CH1 as negative	R/W	0			The difference of (CH0 – CH1) is converted and the result is stored in the ADC−0−Data Register in 2’s complement.
11:10	SE2:SE3	External single−ended analog input for CH0 & CH1.	R/W	0x0			The result is stored in ADC−n−Data register in 2’s complement.
9	DF(CH2+/CH3−)	External analog differential input pair, CH2 and CH3, with CH2 as positive and CH3 as negative	R/W	0			The difference of (CH2 – CH3) is converted and the result is stored in the ADC−2−Data Register in 2’s complement.
8:0	SE4:SE12	External single−ended analog inputs for CH4 to CH12.	R/W	0X00			The result is stored in ADC−n−Data register in 2’s complement.

Table 39. CH0 & CH1 BIT SETTINGS

Bit 14	Bit 13	Bit 12	Description
1	1	0	CH0 and CH1 are both accessed as single−ended inputs. Bit 12 is ignored.
1	0	0	CH0 is accessed as a single−ended input. CH1 is not accessed. Bit 12 is ignored.
0	1	0	CH1 is accessed as a singled−ended. CH0 is not accessed. Bit 12 is ignored.
0	0	1	Differential input pair CH0 + and CH1– is accessed as a differential input.
0	0	0	CH0, CH1, and differential pair CH0+/CH1– are not accessed.

Table 40. CH2 & CH3 BIT SETTINGS

Bit 11	Bit 10	Bit 9	Description
1	1	0	CH2 and CH3 are both accessed as single−ended inputs. Bit 9 is ignored.
1	0	0	CH2 is accessed as a single−ended input. CH3 is not accessed. Bit 9 is ignored.
0	1	0	CH3 is accessed as a singled−ended. CH2 is not accessed. Bit 9 is ignored.
0	0	1	Differential input pair CH2 + and CH3– is accessed as a differential input.
0	0	0	CH2, CH3, and differential pair CH2+/CH3– are not accessed.

Table 41. ADC CHANNEL REGISTER 1

Register Information			
Description	These bits specify the external analog auxiliary input channels CH13, CH14 and CH15 to be converted. The specified channel is accessed sequentially in order from bit 14 to bit 0, and then Bit 14 to Bit 12 of ADC Status Register 1. The input is converted when the corresponding bit is set (‘1’).		
Offset	0x51	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved	R	0			
14:12	SE13:SE15	External single−ended analog input for CH13 to CH15.	R/W	0x0			The result is stored in ADC−n−Data register in 2’s complement. (?)
11:0	Reserved		R	0			

Table 42. ADC GAIN REGISTER

Register Information			
Description	ADC Gain Registers		
Offset	0x52	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	ADG0	Analog input range of single ended CH0 or diff pair DF (CH0+/CH1−)	R/W	1			When ADG0 = ‘1’, the analog input range of single−ended input CH0 (SE0) is 0 to (2 · V_{REF}) or differential input pair DF(CH0+/CH1–) is (–2 · V_{REF}) to (+2 · V_{REF}). When ADG0 = ‘0’, the analog input range of single−ended input CH0 (SE0) is 0 to V_{REF} or differential input pair DF(CH0+/CH1–) is –V_{REF} to +V_{REF}.
14	ADG1	Analog input range of single ended CH1	R/W	1			When ADG1 = ‘1’, the analog input range is 0 to (2 · V_{REF}). When ADG1 = ‘0’, the analog input range of single−ended input CH1 (SE1) is 0 to V_{REF}.
13	ADG2	Analog input range of single ended CH2 or diff pair DF (CH2+/CH3−)	R/W	1			When ADG2 = ‘1’, the analog input range of single−ended input CH2 (SE2) is 0 to (2 · V_{REF}) or differential input pair DF(CH2+/CH3–) is (–2 · V_{REF}) to (+2 · V_{REF}). When ADG2 = ‘0’, the analog input range of single−ended input CH2 (SE2) is 0 to V_{REF} or differential input pair DF(CH2+/CH3–) is –V_{REF} to +V_{REF}.
12	ADG3	Analog input range of single ended CH3	R/W	1			When ADG3 = ‘1’, the analog input range is 0 to (2 · V_{REF}). When ADG3 = ‘0’, the analog input range of single−end input CH3 (SE3) is 0 to V_{REF}.
11:0	ADG4:ADG15		R/W	0xFFF			When these bits = ‘1’, the analog input range is 0 to (2 · V_{REF}). When these bits = ‘0’, the analog input range of CH*n* (where n = 4 to 15) is 0 to V_{REF}

Table 43. AUTO_DAC_CLR_SOURCE REGISTER

Register Information			
Description	This register selects which alarm forces the DAC into a *clear* state, regardless of which DAC operation mode is active, auto or manual		
Offset	0x53	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved	R	0			
14:11	CH0_ALR_CLR: CH3_ALR_CLR	CH0 to CH3 alarm clear Bits.	R/W	0X0			If CHX_ALR_CLR = ‘1’, and if both the ACLR*n* bit in the AUTO_DAC_CLR_EN Register and the CHX_ALR bit in the Status Register are set (‘1’), then DAC−*n* is forced to a clear status. If CHX_ALR_CLR = ‘0’, then CHX_ALR goes to ‘1’ and does not force any DAC to a clear status. (X=0,1,2,3)
10	Local_Low_ALR_CLR	Local temperature low alarm clear Bit.	R/W	0			If Local_Low_ALR_CLR = ‘1’, and if both the ACLR*n* bit in the AUTO−DAC−CLR−EN Register and the Local_Low_ALR bit in the Status Register are set (‘1’), then DAC*n* is forced to a clear CLR status. If Local_Low_ALR_CLR = ‘0’, then Local_Low_ALR goes to ‘1’ and does not force any DAC to a clear status
9	Local_High_ALR_CLR	Local temperature high alarm clear Bit.	R/W	0			If Local_High_ALR_CLR = ‘1’, and if both the ACLR*n* bit in the AUTO_DAC_CLREN Register and the Local_High_ALR bit in the Status Register are set (‘1’), then DAC*n* is forced to a clear CLR status. If Local_High_ALR_CLR = ‘0’, then Local_High_ALR goes to ‘1’ and does not force any DAC to a clear status.
8	REMOTE1_Low_ALR_CLR	Remote temperature sensor REMOTE1 Low alarm clear bit.	R/W	0			If REMOTE1_Low_ALR_CLR = ‘1’, and if both the ACLR*n* bit in the AUTO_DAC_CLR_EN Register and the REMOTE1−Low−ALR bit in the Status Register are set (‘1’), then DAC*n* is forced to a clear CLR status. If REMOTE1_Low_ALR_CLR = ‘0’, then REMOTE1_Low_ALR goes to ‘1’ and does not force any DAC to a clear status.
7	REMOTE1_High_ALR_CLR	Remote temperature sensor REMOTE1 High alarm clear bit	R/W	0			If REMOTE1_High_ALR_CLR = ‘1’, and if both the ACLR*n* bit in the AUTO_DAC_CLR_EN Register and the REMOTE1_High_ALR bit in the Status Register are set (‘1’), then DAC*n* is forced to a clear CLR status. If REMOTE1_High_ALR_CLR = ‘0’, then REMOTE1_High_ALR goes to ‘1’ and does not force any DAC to a clear status.

Table 43. AUTO_DAC_CLR_SOURCE REGISTER

Field	Name	Description	Access	Default	Sim	Bench	Functionality
6	REMOTE2_Low_ALR_CLR	Remote temperature sensor REMOTE2 Low alarm clear bit	R/W	0			If REMOTE2_Low_ALR_CLR = '1', and if both the ACLR*n* bit in the AUTO_DAC_CLR_EN Register and the REMOTE2−Low−ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear CLR status. If REMOTE2_Low_ALR_CLR = '0', then REMOTE2_Low_ALR goes to '1' and does not force any DAC to a clear status.
5	REMOTE2_High_ALR_CLR	Remote temperature sensor REMOTE2 High alarm clear bit	R/W	0			If REMOTE2_High_ALR_CLR = '1', and if both the ACLR*n* bit in the AUTO_DAC_CLR_EN Register and the REMOTE2_High_ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear CLR status. If REMOTE2_High_ALR_CLR = '0', then REMOTE2_High_ALR goes to '1' and does not force any DAC to a clear status.
4	REMOTE1_FAIL_CLR	REMOTE1 Fail Alarm clear Bit	R/W	0			If REMOTE1_FAIL_CLR = '1', and if both the ACLR*n* bit in the AUTO_DAC_CLR_EN Register and the REMOTE2_FAIL_ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If REMOTE1_FAIL_ALR_CLR = '0', then REMOTE1_FAIL_ALR goes to '1' and does not force any DAC to a clear status
3	REMOTE2_FAIL_CLR	REMOTE2 Fail Alarm clear Bit	R/W	0			If REMOTE2_FAIL_CLR = '1', and if both the ACLR*n* bit in the AUTO_DAC_CLR_EN Register and the REMOTE2_FAIL_ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If REMOTE2_FAIL_ALR_CLR = '0', then REMOTE2_FAIL_ALR goes to '1' and does not force any DAC to a clear status.
2	THERM_ALR_CLR	Thermal alarm clear Bit.	R/W	1			If THERM_ALR_CLR = '1', and if both the ACLR*n* bit in the AUTO_DAC_CLR_EN Register and the THERM_ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear CLR status. If THERM_ALR_CLR = '0', then THERM−ALR goes to '1' and does not force any DAC to a clear status.
1:0	Bit1:Bit0	Reserved	R	0			

Table 44. AUTO_DAC_CLR_EN REGISTER

Register Information			
Description	This register selects which alarm forces the DAC into a *clear* state, regardless of which DAC operation mode is active, auto or manual. ACLR*n* is always ignored when an alarm occurs for a temperature greater than +150°C (THERM−ALR = ‘1’). If an alarm activates for a temperature greater than +150°C, and if the THERM_ALR_CLR bit in the AUTO_DAC_CLR_SOURCE Register is set (‘1’), all DACs are forced into a clear status. However, if THERM_ALR_CLR is cleared (‘0’), the over +150°C alarm does not force any DAC to a clear status.		
Offset	0x54	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved	R	0			
14:3	ACLR11:ACLR0	Auto clear DAC−*n* enable bit.	R/W	0X0			If ACLR*n* = ‘1’, DAC−*n* is forced into a clear state when the alarm occurs. If ACLR*n* = ‘0’, DAC−*n* is not forced into a clear state when the alarm occurs (default).
2:0	Bit2:Bit0		R	0			

Table 45. SW_DAC_CLR REGISTER

Register Information			
Description	This register uses software to force the DAC into a clear state.		
Offset	0x55	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved	R	0			
14:3	ICLR11:ICLR0	Software clear DAC*n* bit.	R/W	0X0			If ICLR*n* = ‘1’, DAC−*n* is forced into a clear state when the alarm occurs. If ICLR*n* = ‘0’, DAC−*n* is restored to normal operation.
2:0	Bit2:Bit0		R	0			

Table 46. HW_DAC_CLR_EN REGISTER

Register Information			
Description	This register determines which DAC is in a clear state when the \DAC_CLR_0 pin goes low.		
Offset	0x56	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved	R	0			
14:3	H0CLR11: H0CLR0	Hardware clear DAC*n* enable bit.	R/W	0X0			If H0CLR*n* = ‘1’, DAC−*n* is forced into a clear state when the DAC_CLR_0 pin goes low. If H0CLR*n* = ‘0’, pulling the DAC_CLR_0 pin low does not effect the state of DAC−*n.*
2:0	Bit2:Bit0		R	0			

Table 47. HW_DAC_CLR_EN 1 REGISTER

Register Information			
Description	This register determines which DAC is in a clear state when the \DAC_CLR_1 pin goes low.		
Offset	0x57	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved	R	0			
14:3	H1CLR11: H1CLR0	Hardware clear DAC*n* enable 1 bit.	R/W	0X0			If H1CLR*n* = '1', DAC−*n* is forced into a clear state when the DAC_CLR_1 pin goes low. If H1CLR*n* = '0', pulling the DAC_CLR_1 pin low does not effect the state of DAC−*n.*
2:0	Bit2:Bit0		R	0x0			

Table 48. DAC_CONFIGURATION REGISTER

Register Information			
Description	DAC Configuration Register		
Offset	0x58	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0			
11:0	SLDA11: SLDA0	DAC synchronous load enable bit.	R/W	0X0			If SLDA−*n* = '1', synchronous load is enabled. When internal load DAC signal ILDAC occurs, the DAC−*n* Latch is loaded with the value of the corresponding DAC*n*−Data Register, and the output of DAC−*n* is updated immediately. The internal load DAC signal ILDAC is generated by writing a '1' to the ILDAC bit in the Configuration Register. In synchronous Load, a write command to the DAC−*n*−Data Register updates that register only, and does not change the DAC−*n* output. If SLDA−*n* = '0', asynchronous load is enabled. A write command to the DAC−*n*−Data Register immediately updates the DAC−*n* Latch and the output of DAC−*n*. The synchronous load DAC signal (ILDAC) does not affect DAC*n*. the default value of SLDA−*n* = '0'. The NCD9812 updates the DAC Latch only if the ILDAC bit was set ('1'), thereby eliminating unnecessary glitch. Any DAC channels that have not been accessed are not reloaded. When the DAC Latch is updated, the corresponding output changes to the new level immediately. Note that the SLDA−*n* bit is ignored in auto mode (DAC−*n* Mode bits do not equal '00'). In auto mode, the DAC Latch is always updated asynchronously.

NOTE: The DACs can be forced into a clear state immediately by the external DAC−CLR−n signal, by alarm events, and by writing to the W_DAC_CLR Register. In these cases, the SLDA−*n* bit is ignored.

Table 49. DAC GAIN REGISTER

Register Information			
Description	The DAC*n* GAIN bits specify the output range of DAC*n*.		
Offset	0x59	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0			
11:0	DAC11GAIN: DAC0GAIN	DAC*n* gain bit.	R/W	0X0			Always set DAC*n* GAIN = '0' If DAC*n* GAIN = '0', the gain = 2 and the output is 0 to 2 · VREF

Analog Input Channel Threshold Registers (Read/Write, Addresses = 5Ah to 61h)

Four analog auxiliary inputs (CH0, CH1, CH2, and CH3) and three temperature sensors (LT, REMOTE1, and REMOTE2) implement an out_of_range alarm function. Threshold_High_*n* and Threshold_Low_*n* (where n = 0, 1, 2, 3) define the upper bound and lower bound of the *n*th analog input range. This window determines whether the nth input is out_of_range. When the input is outside the window, the corresponding CH_ALR_*n* bit in the Status Register is set to '1'. For normal operation, the value of Threshold_High_*n* must be greater than the value of Threshold_Low_*n*; otherwise, CH_ALR_*n* is always set to '1' and an alarm is always indicated. Note that when the analog channel is accessed as single_ended input, its threshold is in a straight binary format. However, when the channel is accessed as a differential pair, its threshold is in 2's complement format.

Table 50. THRESHOLD CODING

Input Channel	Input Type	Threshold Stored In	Format
Channel 0	Single−Ended	Input−0−Threshold−High−Byte Input−0−Threshold−Low−Byte	Straight Binary
Channel 1	Single−Ended	Input−1−Threshold−High−Byte Input−1−Threshold−Low−Byte	Straight Binary
Channel 2	Single−Ended	Input−2−Threshold−High−Byte Input−2−Threshold−Low−Byte	Straight Binary
Channel 3	Single−Ended	Input−3−Threshold−High−Byte Input−3−Threshold−Low−Byte	Straight Binary
CH0+/CH1−	Differential	Input−0−Threshold−High−Byte Input−0−Threshold−Low−Byte	2's Complement
CH2+/CH3−	Differential	Input−2−Threshold−High−Byte Input−2−Threshold−Low−Byte	2's Complement

Table 51. INPUT−n−HIGH−THRESHOLD REGISTER (where n = 0, 1, 2, 3)

Register Information			
Description			
Offset	0x	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0			
11:0	THRH11: THRH0	Data bits of the upper−bound threshold of the *n*th analog input.	R/W	0XFFF			

Table 52. INPUT−n−LOW−THRESHOLD REGISTER (where n = 0, 1, 2, 3)

Register Information			
Description			
Offset	0x	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0			
11:0	THRL11: THRL0	Data bits of the lower−bound threshold of the *n*th analog input.	R/W	0X000			

Temperature Threshold Registers

Table 53. LT−HIGH THRESHOLD REGISTER

Register Information			
Description			
Offset	0x62	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0x0			
11:0	THRH11: THRH0		R/W	0X7FF			

Table 54. Local−LOW THRESHOLD REGISTER

Register Information			
Description			
Offset	0x63	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0x0			
11:0	THRL11: THRL0		R/W	0X800			

Table 55. REMOTE1−HIGH THRESHOLD REGISTER

Register Information			
Description			
Offset	0x64	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0x0			
11:0	THRH11: THRH0		R/W	0X7FF			

Table 56. REMOTE1−LOW THRESHOLD REGISTER

Register Information			
Description			
Offset	0x65	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0x0			
11:0	THRL11: THRL0		R/W	0X800			

Table 57. REMOTE2−HIGH THRESHOLD REGISTER

Register Information			
Description			
Offset	0x66	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0x0			
11:0	THRH11: THRH0		R/W	0X7FF			

Table 58. REMOTE2−LOW THRESHOLD REGISTER

Register Information			
Description			
Offset	0x67	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15:12	Bit_15:Bit_12	Reserved	R	0x0			
11:0	THRL11: THRL0		R/W	0X800			

Hysteresis Registers

Table 59. HYSTERESIS REGISTER 0

Register Information			
Description	This register contains the hysteresis values for CH0 and CH1, with default value 0x0810		
Offset	0x68	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved	R	0			
14:8	CH0−HYS−6: CH0−HYS−0	Hysteresis of CH0, 1 LSB per step.	R/W				
7:1	CH1−HYS−6: CH1−HYS−0	Hysteresis of CH1, 1 LSB per step.	R/W				
0	Bit_0	Reserved					

Table 60. HYSTERESIS REGISTER 1

Register Information			
Description	This register contains the hysteresis values for CH2 and CH3, with default value 0x0810		
Offset	0x69	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved	R	0			
14:8	CH2−HYS−6: CH2−HYS−0	Hysteresis of CH2, 1 LSB per step.	R/W				
7:1	CH3−HYS−6: CH3−HYS−0	Hysteresis of CH3, 1 LSB per step.	R/W				
0	Bit_0	Reserved					

Table 61. HYSTERESIS REGISTER 2

Register Information			
Description	This register contains the hysteresis values for REMOTE2, REMOTE1 and LT, with default value 0x2108		
Offset	0x6A	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved	R	0			
14:10	REMOTE2−HYS−7: REMOTE2−HYS−3	Hysteresis of REMOTE2, 1°C per step. Note that bits REMOTE2−HYS−[2:0] are always ‘0’	R/W				
9:5	REMOTE1−HYS−7: REMOTE1−HYS−3	Hysteresis of REMOTE1, 1°C per step. Note that bits REMOTE1−HYS−[2:0] are always ‘0’	R/W				
4:0	Local−HYS−7: Local−HYS−3	Hysteresis of Local, 1°C per step. Note that bits Local−HYS−[2:0] are always ‘0’	R/W				

Table 62. POWER DOWN REGISTER

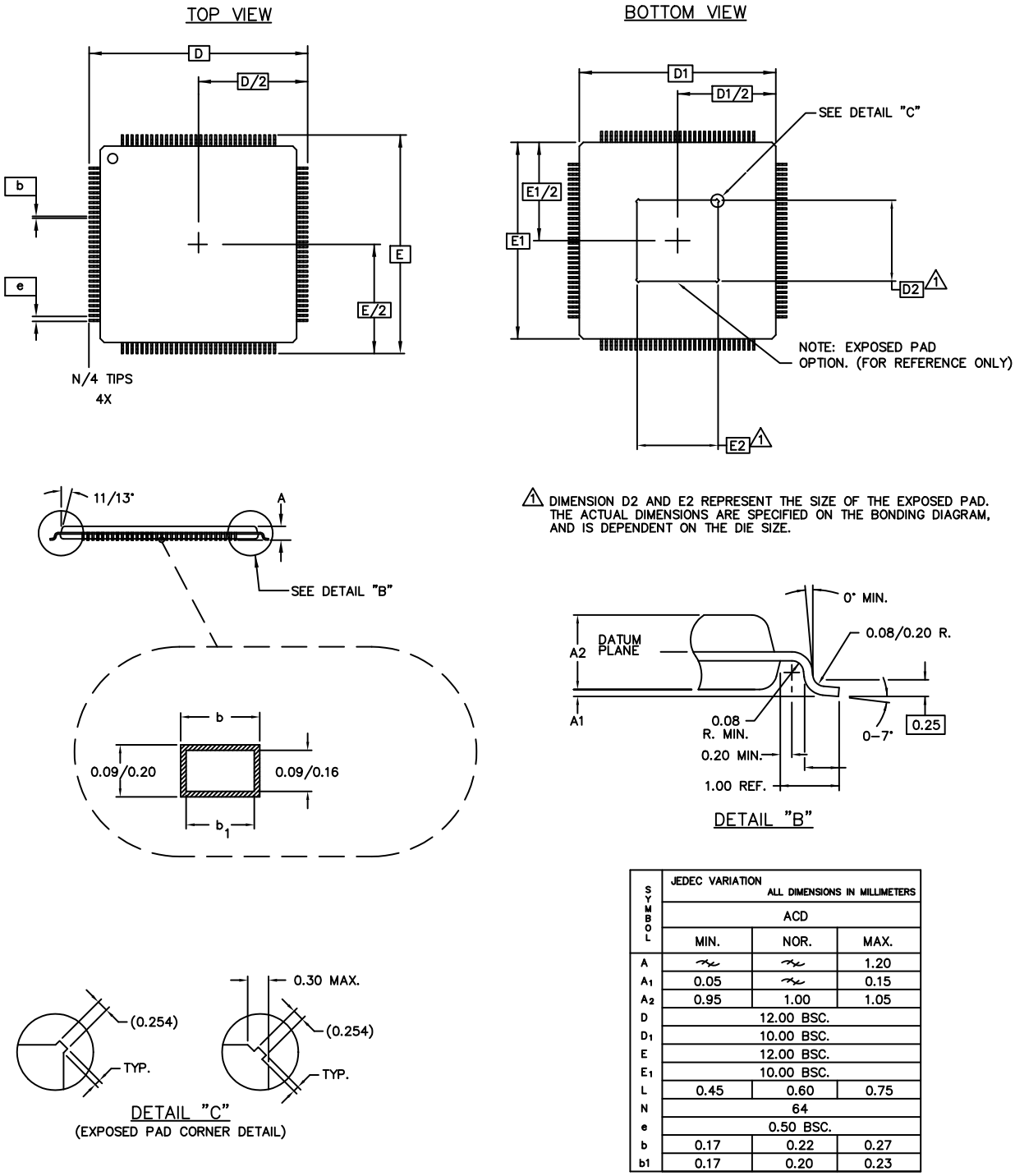
Register Information			
Description	After power−on or reset, all bits in the Power−Down Register are cleared to ‘0’, and all the components controlled by this register are either powered−down or off. The Power−Down Register allows the host to manage the NCD9812 power dissipation. When not required, the ADC, the reference buffer amplifier, and any of the DACs can be put into an inactive low−power mode to reduce current drain from the supply. The bits in the Power−Down Register control this power−down function. Set the respective bit to ‘1’ to activate the corresponding function.		
Offset	0x6B	**Type:**	R/W

Bitfield Details

Field	Name	Description	Access	Default	Sim	Bench	Functionality
15	Bit_15	Reserved	R	0			
14	Bit_14	Power−down mode control bit.	R/W				If PADC = ‘1’, the ADC is in normal operating mode. If PADC = ‘0’, the ADC is inactive in low−power mode.
13	Bit_13	Internal reference in power−down mode control bit	R/W				If PREF = ‘1’, the reference buffer amplifier is powered on. If PREF = ‘0’, the reference buffer amplifier is inactive in low−power mode.
12:1	PDAC0:PDAC11	DAC*n* power−down control bit.	R/W				If PDAC*n* = ‘1’, DAC*n* is in normal operating mode. If PDAC*n* = ‘0’, DAC*n* is inactive in low−power mode and its output buffer amplifier is in a Hi−Z state. The output pin of DAC*n* is internally switched from the buffer output to the analog ground through an internal resistor.
0	Bit_0	Reserved					

PACKAGE OUTLINE

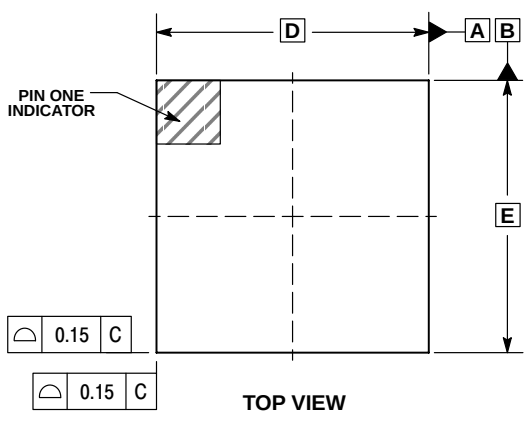
TQFP−64 EP, 10x10
CASE 136AC
ISSUE O

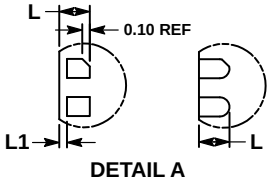


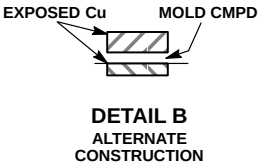
SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
	ACD		
	MIN.	NOR.	MAX.
A			1.20
A_1	0.05		0.15
A_2	0.95	1.00	1.05
D		12.00 BSC.	
D_1		10.00 BSC.	
E		12.00 BSC.	
E_1		10.00 BSC.	
L	0.45	0.60	0.75
N		64	
e		0.50 BSC.	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23

PACKAGE OUTLINE

QFN64 9x9, 0.5P
CASE 485CT
ISSUE O

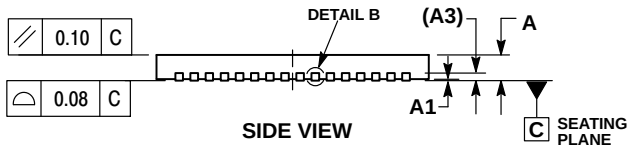


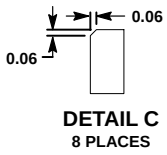


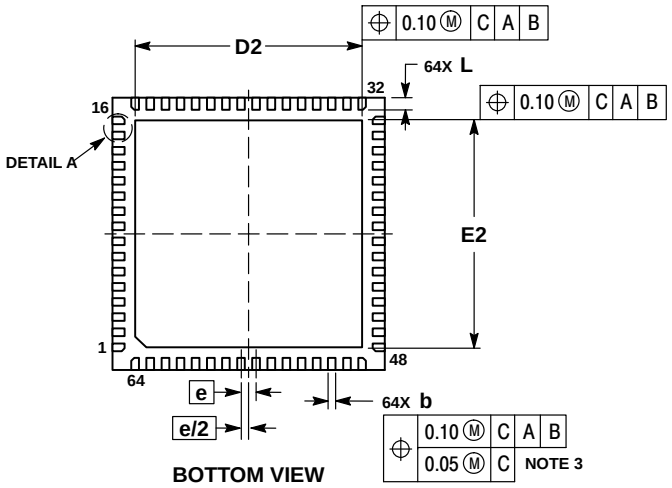


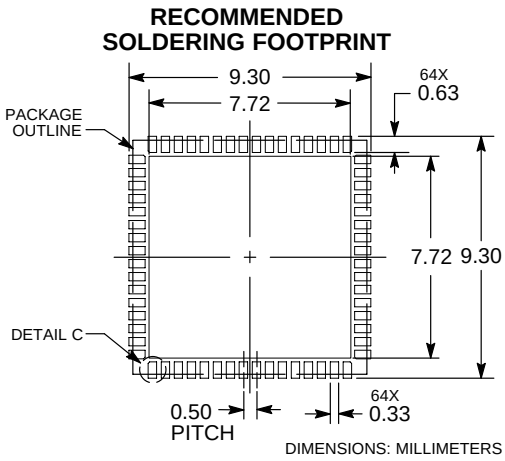
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25mm FROM THE TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.80	0.90
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	9.00 BSC	
D2	7.40	7.60
E	9.00 BSC	
E2	7.40	7.60
e	0.50 BSC	
L	0.30	0.50
L1	0.00	0.15









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