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MOSFET – Power, Single N-Channel, TDFNW8 DUAL COOL[®] 150 V, 4.45 mΩ, 165 A

NVMTSC4D3N15MC

Features

- Small Footprint (8x8 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter			Value	Unit
V _{DSS}	Drain-to-Source Voltage			150	V
V _{GS}	Gate-to-Source Voltage			±20	V
I _D	Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T _C = 25°C	165	Α
P _D	Power Dissipation $R_{\theta JC}$ (Note 2)			292	W
I _D	Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T _C = 100°C	117	Α
P _D	Power Dissipation R _{θJC} (Note 2)			146	W
I _D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T _A = 25°C	23	Α
P _D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			5	W
I _D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady T _A = 100°C		16	Α
P _D	Power Dissipation R _{θJA} (Notes 1, 2)			3	W
I _{DM}	Pulsed Drain Current	T _A = 25°C	C, t _p = 10 μs	900	Α
T _J , T _{stg}	Operating Junction and Storage Temperature Range			-55 to +175	°C
I _S	Source Current (Body Diode)			243	Α
E _{AS}	Single Pulse Drain-to-Source Avalanche Energy (I _L = 14.1 A _{pk} ,)			3390	mJ
TL	Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

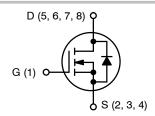
- 1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted



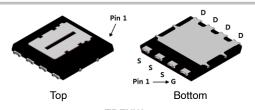
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V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
150 V	4.45 mΩ @ 10 V	165 A

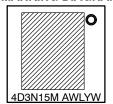


N-CHANNEL MOSFET



TDFNW8 CASE 507AS

MARKING DIAGRAM



4D3N15M = Specific Device Code

A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

ORDERING INFORMATION

Device	Package	Shipping [†]
NVMTSC4D3N15MC	TDFNW8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{ hetaJC}$	Junction-to-Case - Steady State (Note 2)	0.5	°C/W
$R_{ hetaJC}$	Junction-to-Case Top (Note 2)	0.8	
$R_{ hetaJA}$	Junction-to-Ambient - Steady State (Note 2)	28	

V(BR)DSS / TJ	Drain – to – Source Breakdown Voltage Drain – to – Source Breakdown Voltage Temperature Coefficient Zero Gate Voltage Drain Current Gate – to – Source Leakage Current RISTICS (Note 3) Gate Threshold Voltage Negative Threshold Temperature Coefficient Drain – to – Source On Resistance Forward Transconductance Gate–Resistance	$\begin{split} &V_{GS} = 0 \text{ V}, \text{ I}_{D} = \\ &I_{D} = 250 \mu\text{A}, \text{ ref} \\ &V_{GS} = 0 \text{ V}, \\ &V_{DS} = 120 \text{ V} \\ &V_{DS} = 120 \text{ V} \\ &V_{DS} = 0 \text{ V}, \text{ V}_{GS} \\ &V_{GS} = V_{DS}, \text{ I}_{D} = \\ &I_{D} = 250 \mu\text{A}, \text{ ref} \\ &V_{GS} = 10 \text{ V}, \text{ I}_{D} = \\ &V_{DS} = 5 \text{ V}, \text{ I}_{D} = \\ &T_{A} = 25^{\circ}\text{C} \end{split}$	f to 25°C $T_{J} = 25^{\circ}C$ $T_{J} = 125^{\circ}C$ $= \pm 20 \text{ V}$ $= 521 \mu\text{A}$ f to 25°C $= 95 \text{ A}$	150	- 49.84 3.6 - 9.93 3.4	1 10 ±100 4.5 - 4.45	V mV/°C μA μA nA
V(BR)DSS	Drain – to – Source Breakdown Voltage Drain – to – Source Breakdown Voltage Temperature Coefficient Zero Gate Voltage Drain Current Gate – to – Source Leakage Current RISTICS (Note 3) Gate Threshold Voltage Negative Threshold Temperature Coefficient Drain – to – Source On Resistance Forward Transconductance Gate–Resistance PACITANCES	$\begin{split} I_D &= 250 \; \mu\text{A, ref} \\ V_{GS} &= 0 \; \text{V,} \\ V_{DS} &= 120 \; \text{V} \\ \end{split} \\ V_{DS} &= 0 \; \text{V, } V_{GS} \\ \end{split} \\ V_{GS} &= V_{DS}, \; I_D = \\ I_D &= 250 \; \mu\text{A, ref} \\ V_{GS} &= 10 \; \text{V, } I_D = \\ \end{split}$	f to 25°C $T_{J} = 25^{\circ}C$ $T_{J} = 125^{\circ}C$ $= \pm 20 \text{ V}$ $= 521 \mu\text{A}$ f to 25°C $= 95 \text{ A}$	- - - - 2.5 -	49.84 - - - - 3.6 -9.93	1 10 ±100	mV/°C μA μA nA
V(BR)DSS / TJ	Drain – to – Source Breakdown Voltage Temperature Coefficient Zero Gate Voltage Drain Current Gate – to – Source Leakage Current RISTICS (Note 3) Gate Threshold Voltage Negative Threshold Temperature Coefficient Drain – to – Source On Resistance Forward Transconductance Gate–Resistance PACITANCES	$\begin{split} I_D &= 250 \; \mu\text{A, ref} \\ V_{GS} &= 0 \; \text{V,} \\ V_{DS} &= 120 \; \text{V} \\ \end{split} \\ V_{DS} &= 0 \; \text{V, } V_{GS} \\ \end{split} \\ V_{GS} &= V_{DS}, \; I_D = \\ I_D &= 250 \; \mu\text{A, ref} \\ V_{GS} &= 10 \; \text{V, } I_D = \\ \end{split}$	f to 25°C $T_{J} = 25^{\circ}C$ $T_{J} = 125^{\circ}C$ $= \pm 20 \text{ V}$ $= 521 \mu\text{A}$ f to 25°C $= 95 \text{ A}$	- - - - 2.5 -	- - - 3.6 -9.93	1 10 ±100	mV/°C μA μA nA
I _{GSS}	Gate – to – Source Leakage Current RISTICS (Note 3) Gate Threshold Voltage Negative Threshold Temperature Coefficient Drain – to – Source On Resistance Forward Transconductance Gate–Resistance PACITANCES	$V_{DS} = 0 \text{ V, } V_{GS}$ $V_{GS} = V_{DS}, I_{D} = I_{D} = 250 \mu\text{A, ref}$ $V_{GS} = 10 \text{ V, } I_{D} = I_{DS} = 10 \text{ V, } I_{DS} = 10 \text{ V, } I_{DS} = 10 \text{ V, } I_{DS} = 10 \text{ V}$	$T_J = 125^{\circ}C$ = ±20 V = 521 μ A f to 25°C = 95 A	2.5	- - 3.6 -9.93	10 ±100	μA nA V mV/°C
VGS(TH)	Gate Threshold Voltage Negative Threshold Temperature Coefficient Drain – to – Source On Resistance Forward Transconductance Gate–Resistance PACITANCES	$V_{DS} = 0 \text{ V, } V_{GS}$ $V_{GS} = V_{DS}, I_{D} = I_{D} = 250 \mu\text{A, ref}$ $V_{GS} = 10 \text{ V, } I_{D} = I_{DS} = 10 \text{ V, } I_{DS} = 10 \text{ V, } I_{DS} = 10 \text{ V, } I_{DS} = 10 \text{ V}$	= ±20 V = 521 μA f to 25°C = 95 A	2.5	3.6	±100	nA V mV/°C
V _{GS(TH)}	Gate Threshold Voltage Negative Threshold Temperature Coefficient Drain – to – Source On Resistance Forward Transconductance Gate–Resistance PACITANCES	$V_{GS} = V_{DS}, I_{D} = I_{D} = 250 \mu A, ref$ $V_{GS} = 10 \text{ V}, I_{D} = V_{DS} = 5 \text{ V}, I_{D} = V_{DS} = 5 \text{ V}, I_{D} = V_{DS} = 5 \text{ V}$	= 521 μA f to 25°C = 95 A	2.5	3.6 -9.93	4.5	V mV/°C
V _{GS(TH)} C V _{GS(TH)} / T _J N R _{DS(on)} [GFS F R _G C CHARGES & CAP C _{ISS} [C _{OSS} C C _{RSS} F Q _{G(TOT)} T Q _{G(TH)} T	Gate Threshold Voltage Negative Threshold Temperature Coefficient Drain – to – Source On Resistance Forward Transconductance Gate–Resistance PACITANCES	$I_D = 250 \mu A, ref$ $V_{GS} = 10 \text{ V}, I_D = 0$ $V_{DS} = 5 \text{ V}, I_D = 0$	f to 25°C = 95 A	-	-9.93	_	mV/°C
V _{GS(TH)} / T _J N R _{DS(on)} [GFS F R _G C CHARGES & CAP ClSS [COSS C CRSS F Q _{G(TOT)} 7 Q _{G(TH)} 7	Negative Threshold Temperature Coefficient Drain – to – Source On Resistance Forward Transconductance Gate–Resistance PACITANCES	$I_D = 250 \mu A, ref$ $V_{GS} = 10 \text{ V}, I_D = 0$ $V_{DS} = 5 \text{ V}, I_D = 0$	f to 25°C = 95 A	-	-9.93	_	mV/°C
V _{GS(TH)} / T _J N R _{DS(on)} [GFS F R _G C CHARGES & CAP C _{ISS} [C _{OSS} C C _{RSS} F Q _{G(TOT)} T Q _{G(TH)} T	Drain – to – Source On Resistance Forward Transconductance Gate–Resistance PACITANCES	$V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ V}$	= 95 A	-			
R _{DS(on)}	Forward Transconductance Gate-Resistance PACITANCES	V _{DS} = 5 V, I _D =		-	3.4	4.45	
R _G	Gate-Resistance PACITANCES	B0 , B	95 A	_			mΩ
CHARGES & CAP CISS COSS CRSS QG(TOT) QG(TH)	PACITANCES	T _A = 25°C			177	-	S
$egin{array}{cccc} C_{ISS} & I & & & & & & & & & & & & & & \\ C_{OSS} & & C_{RSS} & & C_{RSS} & & F_{C} & & & & & & & & & & \\ Q_{G(TOT)} & & & & & & & & & & & & & & & & & & &$		<u> </u>	T _A = 25°C		1.1	-	Ω
C_{OSS} C_{RSS} F $Q_{G(TOT)}$ T $Q_{G(TH)}$	Input Capacitance			1			
C_{RSS} F $Q_{G(TOT)}$ 1 $Q_{G(TH)}$ 1		V _{GS} = 0 V, f = 1 MHz, V _{DS} = 75 V		_	6514	_	pF
$Q_{G(TOT)}$ 1 $Q_{G(TH)}$ 1	Output Capacitance			_	1750	_	-
Q _{G(TH)} 1	Reverse Transfer Capacitance			_	12.5	_	
α(111)	Total Gate Charge	V _{GS} = 10 V, V _{DS} = 75 V, I _D = 95 A		-	79	-	nC
	Threshold Gate Charge			_	21	-	
Q_{GS}	Gate-to-Source Charge			_	36	_	
Q _{GD} (Gate-to-Drain Charge			_	11	-	
V _{GP} F	Plateau Voltage			_	5.8	_	1
SWITCHING CHA	ARACTERISTICS, V _{GS} = 10 V (Note 3)	•		1	•		
t _{d(ON)}	Turn – On Delay Time	V_{GS} = 10 V, V_{D}		-	38	_	ns
t _r F	Rise Time	$I_D = 95 \text{ A}, R_G = 6 \Omega$		_	11	-	
t _{d(OFF)}	Turn – Off Delay Time			_	48	-	1
t _f F	Fall Time			_	8	_	
DRAIN-SOURCE	DIODE CHARACTERISTICS			•			
V _{SD} F	Forward Diode Voltage	V _{GS} = 0 V, I _S = 95 A	T _J = 25°C	_	0.86	1.2	V
			T _J = 125°C	-	0.80	-	1
t _{RR} F	Reverse Recovery Time	$V_{GS} = 0 \text{ V, } dI_S/c$	dt = 100 A/μs,	_	85	-	ns
	Charge Time	I _S = 95 A		_	58	_	
t _b [Charge Time			_	38	_	
Q _{RR} F	Discharge Time		1		194	 	4

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

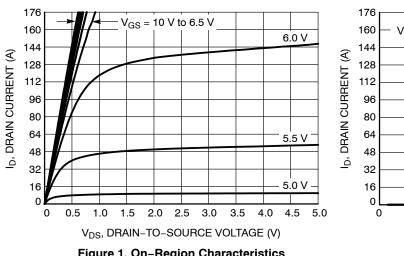


Figure 1. On-Region Characteristics

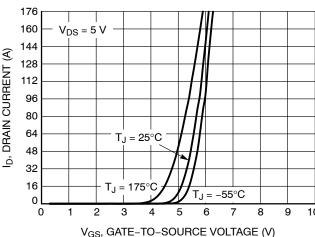


Figure 2. Transfer Characteristics

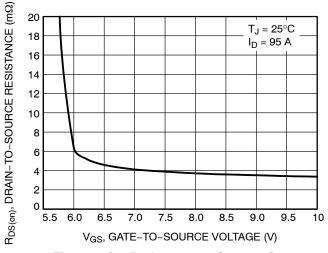


Figure 3. On-Resistance vs. Gate-to-Source Voltage

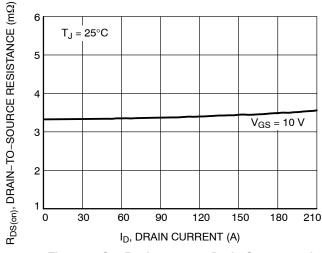


Figure 4. On-Resistance vs. Drain Current and **Gate Voltage**

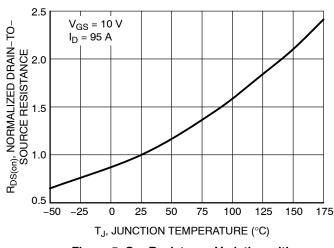


Figure 5. On-Resistance Variation with **Temperature**

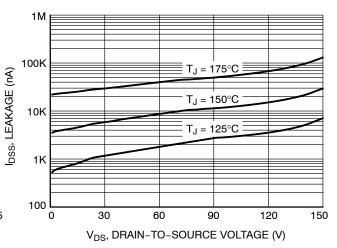
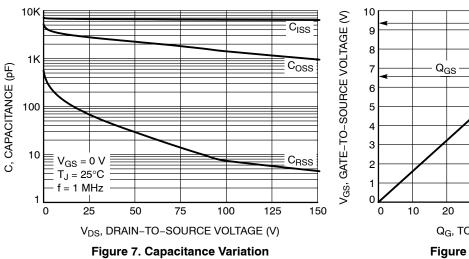


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS



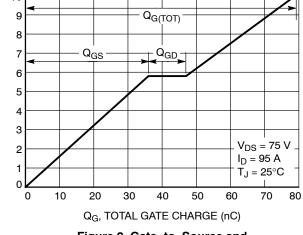


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

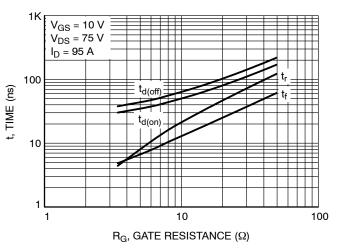


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

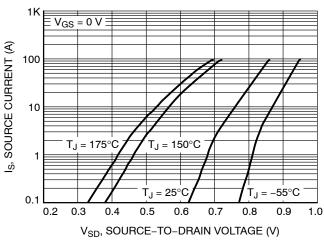


Figure 10. Diode Forward Voltage vs. Current

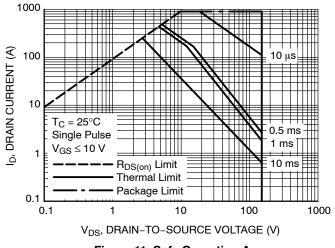


Figure 11. Safe Operating Area

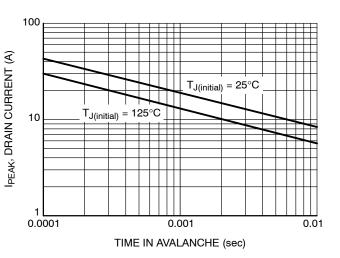


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

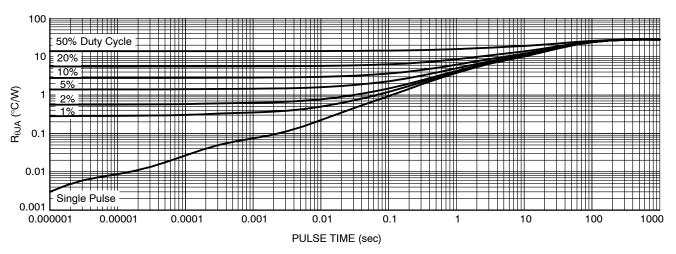
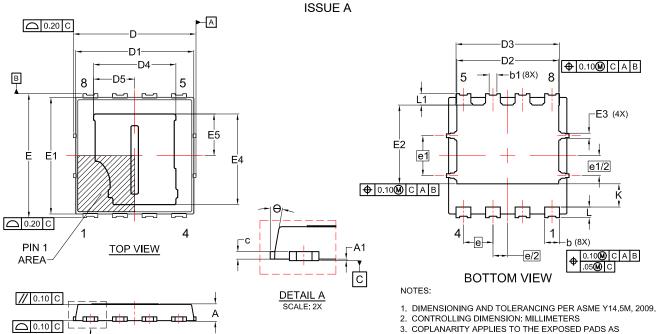
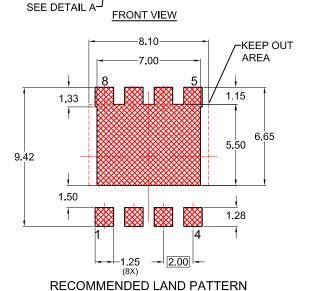


Figure 13. Thermal Characteristics

PACKAGE DIMENSIONS

TDFNW8 8.3x8.4, 2P CASE 507AS





WELL AS THE TERMINALS.

4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

5. SEATING PLANE IS DEFINED BY THE TERMINALS.

"A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS				
5,,,,	MIN.	NOM.	MAX.		
Α	0.82	0.92	1.02		
A1	0.00		0.05		
b	0.90	1.00	1.10		
b1	0.43	0.53	0.63		
С	0.23	0.28	0.33		
D	8.20	8.30	8.40		
D1	7.90	8.00	8.10		
D2	6.80	6.90	7.00		
D3	6.90	7.00	7.10		
D4	5.47	5.57	5.67		
D5	2.69	2.79	2.89		
Ε	8.30	8.40	8.50		
E1	7.80	7.90	8.00		
E2	5.24	5.34	5.44		
E3	0.25	0.35	0.45		
E4	6.03	6.13	6.23		
E5	2.72	2.82	2.92		
е	2.00 BSC				
e/2	1.00 BSC				
e1	2.70 BSC				
e1/2	1.35 BSC				
K	1.50	1.57	1.70		
L	0.64	0.74	0.84		
L1	0.67	0.77	0.87		
θ	0°		12°		

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