# **Power MOSFET**

# 40 V, 3.3 m $\Omega$ , 102 A, Single N-Channel

#### **Features**

- Small Footprint (5x6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- NVMFS5C450NWF Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

# MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	40	V
Gate-to-Source Voltage			$V_{GS}$	±20	V
Continuous Drain	Steady	T <sub>C</sub> = 25°C	I <sub>D</sub>	102	Α
Current R <sub>θJC</sub> (Notes 1, 3)		T <sub>C</sub> = 100°C		72	
Power Dissipation	State	T <sub>C</sub> = 25°C	P <sub>D</sub>	68	W
R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 100°C		34	
Continuous Drain	Steady	T <sub>A</sub> = 25°C	I <sub>D</sub>	24	Α
Current R <sub>0JA</sub> (Notes 1, 2, 3)		T <sub>A</sub> = 100°C		17	
Power Dissipation	State	T <sub>A</sub> = 25°C	P <sub>D</sub>	3.6	W
R <sub>θJA</sub> (Notes 1 & 2)		T <sub>A</sub> = 100°C		1.8	
Pulsed Drain Current	$T_A = 25^{\circ}C$ , $t_p = 10 \mu s$		I <sub>DM</sub>	554	Α
Operating Junction and Storage Temperature		T <sub>J</sub> , T <sub>stg</sub>	-55 to + 175	°C	
Source Current (Body Diode)		I <sub>S</sub>	65	Α	
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 7.0 A)		E <sub>AS</sub>	215	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	2.2	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	41	

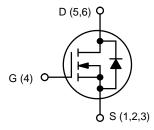
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



## ON Semiconductor®

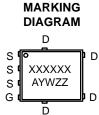
#### www.onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
40 V	$3.3~\mathrm{m}\Omega$ @ $10~\mathrm{V}$	102 A



**N-CHANNEL MOSFET** 





XXXXXX = 5C450N

(NVMFS5C450N) or

450NWF

(NVMFS5C450NWF) = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

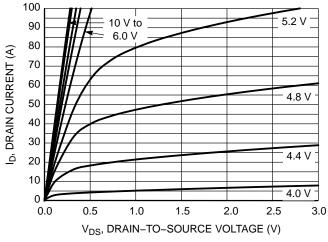
# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS				•		•	
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> / T <sub>J</sub>				20		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V,$	$T_J = 25^{\circ}C$			10	
	$V_{DS} = 40 \text{ V}$		T <sub>J</sub> = 125°C			100	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS}$	; = 20 V			100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D$	= 65 μΑ	2.5		3.5	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-9.1		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V I <sub>D</sub> = 50 A			2.7	3.3	mΩ
Forward Transconductance	9FS	$V_{DS}$ =15 V, $I_{D}$	= 50 A		93		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE						
Input Capacitance	C <sub>ISS</sub>	$V_{GS} = 0 \text{ V, f} = 1 \text{ MHz, } V_{DS} = 25 \text{ V}$ $V_{GS} = 10 \text{ V, } V_{DS} = 20 \text{ V; } I_{D} = 50 \text{ A}$			1600		pF nC
Output Capacitance	C <sub>OSS</sub>				830		
Reverse Transfer Capacitance	C <sub>RSS</sub>				28		
Total Gate Charge	Q <sub>G(TOT)</sub>				23		
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 20 V; I <sub>D</sub> = 50 A			5.1		
Gate-to-Source Charge	Q <sub>GS</sub>				9.0		
Gate-to-Drain Charge	$Q_{GD}$				3.5		
Plateau Voltage	V <sub>GP</sub>				5.3		V
SWITCHING CHARACTERISTICS (Note 5	5)						
Turn-On Delay Time	t <sub>d(ON)</sub>				10		
Rise Time	t <sub>r</sub>	$V_{GS} = 10 \text{ V}, V_{DS} = 20 \text{ V},$ $I_{D} = 50 \text{ A}, R_{G} = 2.5 \Omega$			47		ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>				19		
Fall Time	t <sub>f</sub>				3.0		
DRAIN-SOURCE DIODE CHARACTERIS	TICS						
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 50 A	$T_J = 25^{\circ}C$		0.9	1.2	\/
			T <sub>J</sub> = 125°C		0.78		V
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, dIS/dt} = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 50 \text{ A}$			37		ns
Charge Time	t <sub>a</sub>				18		
Discharge Time	t <sub>b</sub>				19		
Reverse Recovery Charge	$Q_{RR}$				23		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. Pulse Test: pulse width  $\leq 300~\mu s$ , duty cycle  $\leq 2\%$ .

<sup>5.</sup> Switching characteristics are independent of operating junction temperatures.

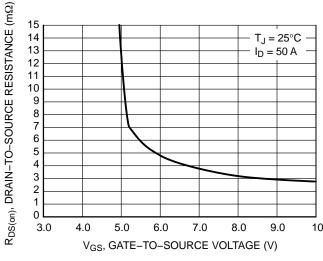
## TYPICAL CHARACTERISTICS



100  $V_{DS} = 10 V$ 90 80 ID, DRAIN CURRENT (A) 70 60 50 40 30  $T_J = 25^{\circ}C$ 20 10  $T_J = -55^{\circ}C$ 0 0 7 V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



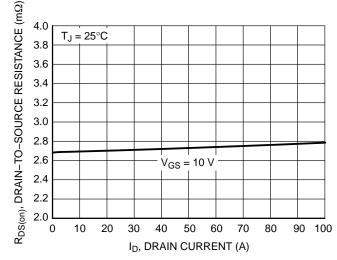
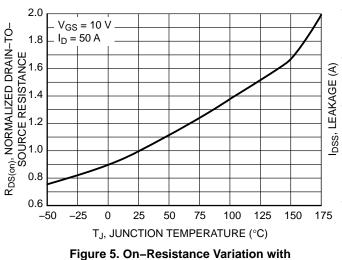


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



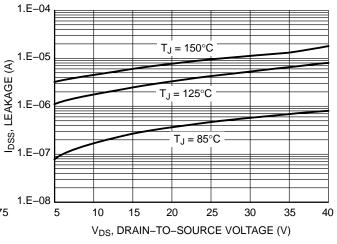


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

## TYPICAL CHARACTERISTICS

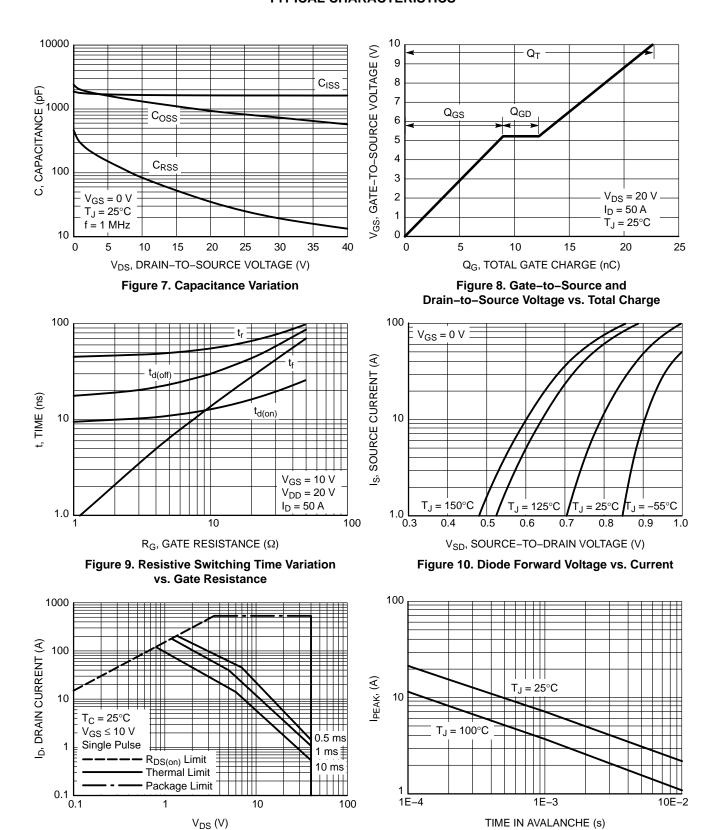


Figure 12. I<sub>PEAK</sub> vs. Time in Avalanche

Figure 11. Safe Operating Area

# **TYPICAL CHARACTERISTICS**

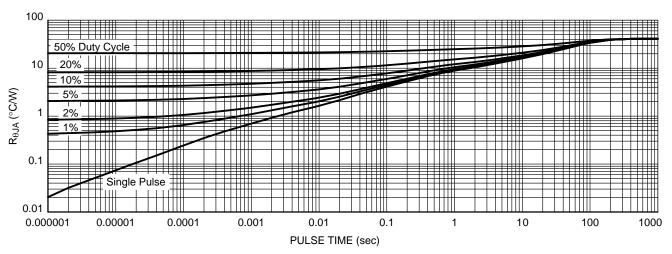


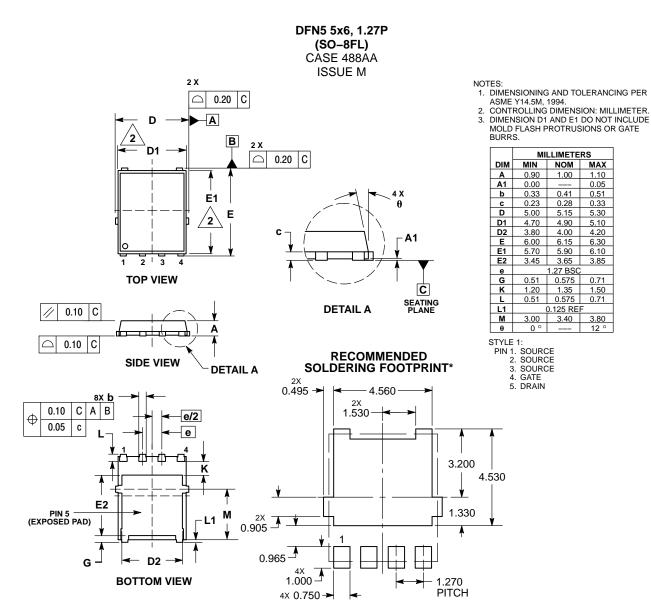
Figure 13. Thermal Characteristics

## **DEVICE ORDERING INFORMATION**

Device	Device Marking Pac		Shipping <sup>†</sup>	
NVMFS5C450NT1G	5C450N	DFN5 (Pb-Free)	1500 / Tape & Reel	
NVMFS5C450NWFT1G	450NWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel	
NVMFS5C450NT3G	5C450N	DFN5 (Pb-Free)	5000 / Tape & Reel	
NVMFS5C450NWFT3G	450NWF	DFN5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel	
NVMFS5C450NAFT1G	5C450N	DFN5 (Pb-Free)	1500 / Tape & Reel	
NVMFS5C450NWFAFT1G	450NWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel	

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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