

NTD4806N, NVD4806N

Power MOSFET

30 V, 76 A, Single N-Channel, DPAK/IPAK

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- AEC-Q101 Qualified and PPAP Capable – NVD4806N
- These Devices are Pb-Free and are RoHS Compliant

Applications

- CPU Power Delivery
- DC-DC Converters
- Low Side Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current ($R_{\theta JA}$) (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	15.6	A
		$T_A = 85^{\circ}\text{C}$		12	
Power Dissipation ($R_{\theta JA}$) (Note 1)		$T_A = 25^{\circ}\text{C}$	P_D	2.65	W
Continuous Drain Current ($R_{\theta JA}$) (Note 2)		$T_A = 25^{\circ}\text{C}$	I_D	11.3	A
		$T_A = 85^{\circ}\text{C}$		8.8	
Power Dissipation ($R_{\theta JA}$) (Note 2)		$T_A = 25^{\circ}\text{C}$	P_D	1.4	W
Continuous Drain Current ($R_{\theta JC}$) (Note 1)		$T_C = 25^{\circ}\text{C}$	I_D	79	A
		$T_C = 85^{\circ}\text{C}$		61	
Power Dissipation ($R_{\theta JC}$) (Note 1)	$T_C = 25^{\circ}\text{C}$	P_D	68	W	
Pulsed Drain Current	$t_p=10\mu\text{s}$	$T_A = 25^{\circ}\text{C}$	I_{DM}	150	A
Current Limited by Package		$T_A = 25^{\circ}\text{C}$	$I_{DmaxPkg}$	45	A
Operating Junction and Storage Temperature			T_J, T_{stg}	-55 to 175	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	50	A
Drain to Source dV/dt			dV/dt	6.0	V/ns
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 24\text{ V}$, $V_{GS} = 10\text{ V}$, $L = 1.0\text{ mH}$, $I_{L(pk)} = 21\text{ A}$, $R_G = 25\text{ }\Omega$)			E_{AS}	220	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

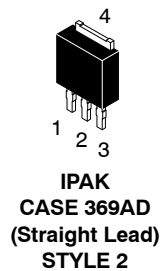
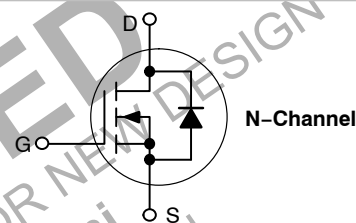
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



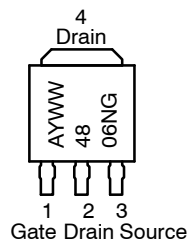
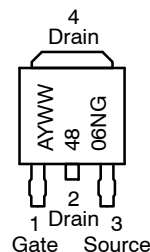
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	6.0 m Ω @ 10 V	76 A
	9.4 m Ω @ 4.5 V	



MARKING DIAGRAMS & PIN ASSIGNMENTS



A = Assembly Location*
Y = Year
WW = Work Week
4806N = Device Code
G = Pb-Free Package

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejector pin), the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.2	$^{\circ}\text{C/W}$
Junction-to-Tab (Drain)	$R_{\theta JC-TAB}$	3.5	
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	56.7	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	106.8	

1. Surface-mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			27		$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^{\circ}\text{C}$		10	μA
			$T_J = 125^{\circ}\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.5		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6.0		$\text{mV}/^{\circ}\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ to }11.5\text{ V}$	$I_D = 30\text{ A}$	4.9	6.0	$\text{m}\Omega$
			$I_D = 15\text{ A}$	4.8		
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$	7.9	9.4	
			$I_D = 15\text{ A}$	7.5		
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		14		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 12\text{ V}$		2142		pF
Output Capacitance	C_{oss}			480		
Reverse Transfer Capacitance	C_{rss}			251		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		15	23	nC
Threshold Gate Charge	$Q_{G(TH)}$			3.0		
Gate-to-Source Charge	Q_{GS}			7.0		
Gate-to-Drain Charge	Q_{GD}			7.0		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		37		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$		13.9		ns
Rise Time	t_r			29.7		
Turn-Off Delay Time	$t_{d(off)}$			18.3		
Fall Time	t_f			7.8		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 11.5 V, V _{DS} = 15 V, I _D = 15 A, R _G = 3.0 Ω		8.5		ns
Rise Time	t _r			23.8		
Turn-Off Delay Time	t _{d(off)}			26		
Fall Time	t _f			4.7		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 30 A	T _J = 25°C T _J = 125°C		0.9 0.8	1.2	V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A			26		ns
Charge Time	t _a				13		
Discharge Time	t _b				13		
Reverse Recovery Time	Q _{RR}				16		nC

PACKAGE PARASITIC VALUES

Source Inductance	L _S	T _A = 25°C		2.49		nH
Drain Inductance, DPAK	L _D			0.0164		
Drain Inductance, IPAK	L _D			1.88		
Gate Inductance	L _G			3.46		
Gate Resistance	R _G			1.0		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

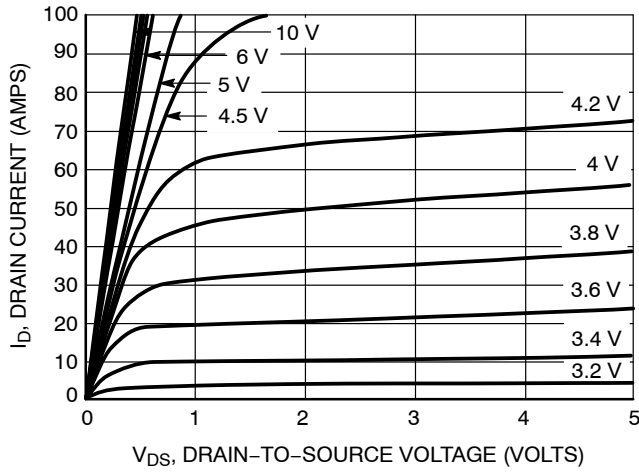


Figure 1. On-Region Characteristics

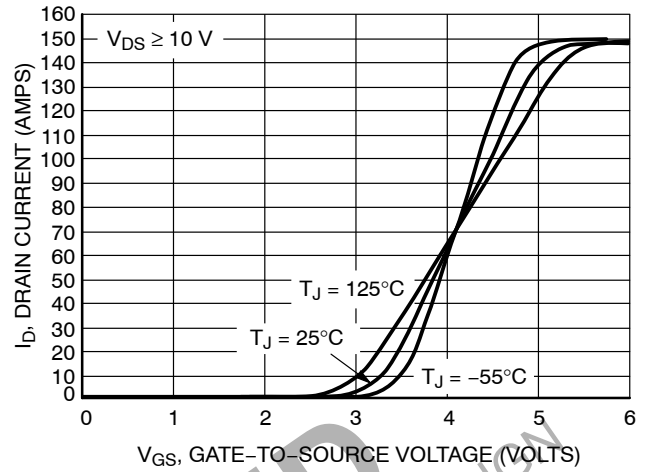


Figure 2. Transfer Characteristics

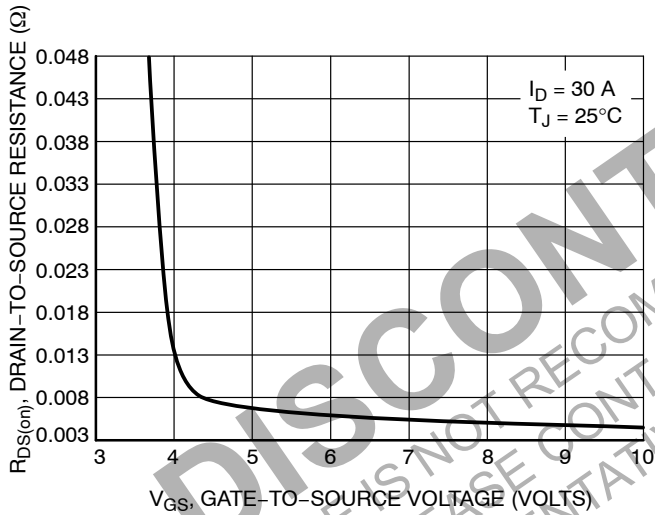


Figure 3. On-Resistance vs. Gate-to-Source Voltage

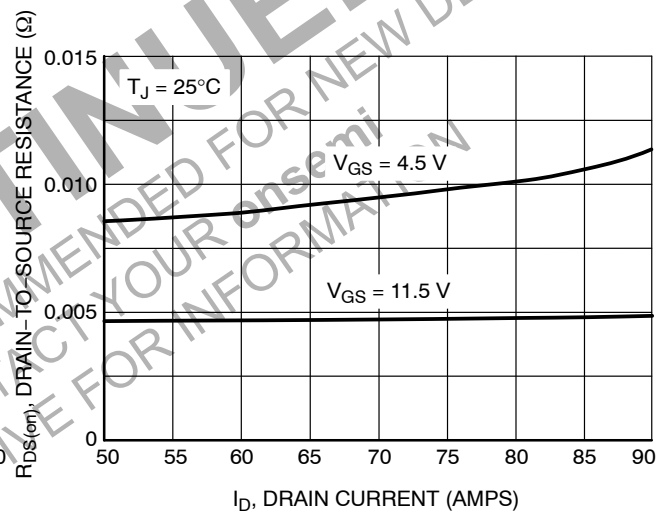


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

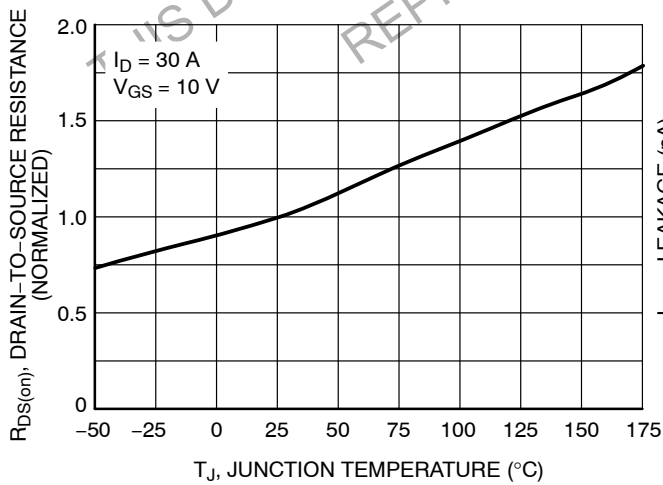


Figure 5. On-Resistance Variation with Temperature

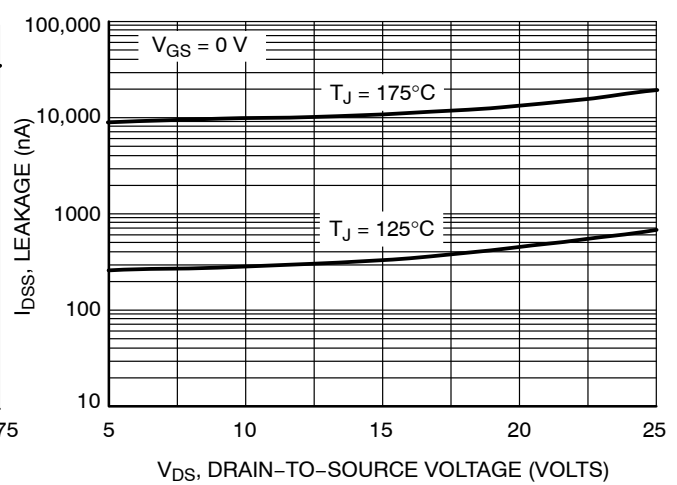


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

TYPICAL PERFORMANCE CURVES

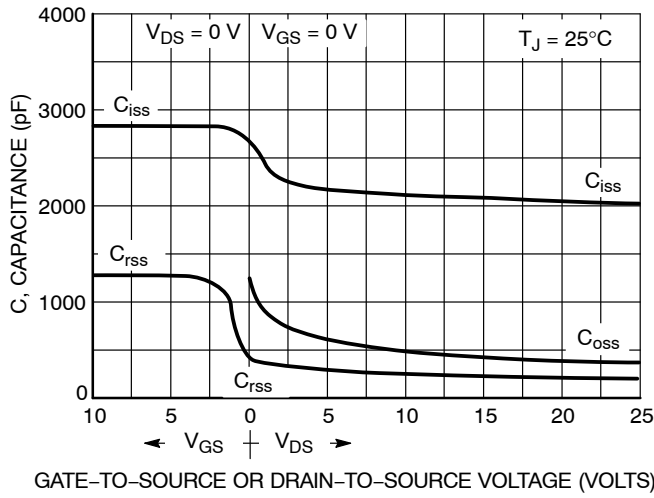


Figure 7. Capacitance Variation

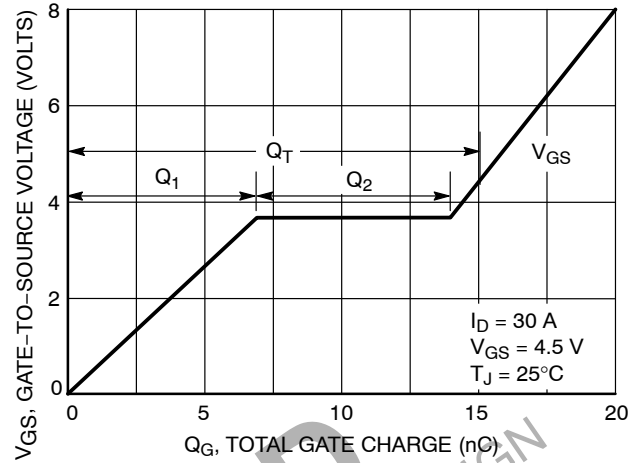


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

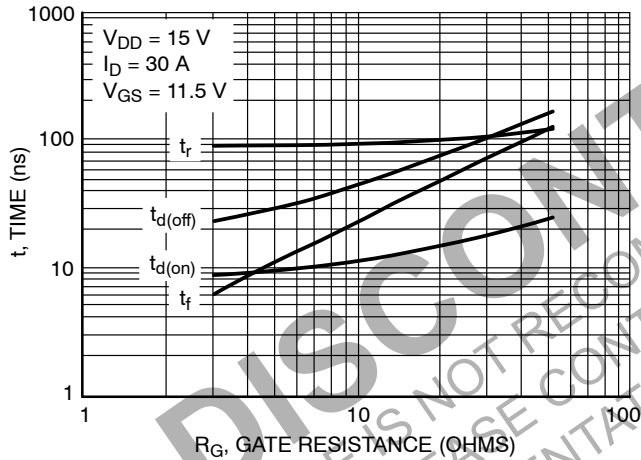


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

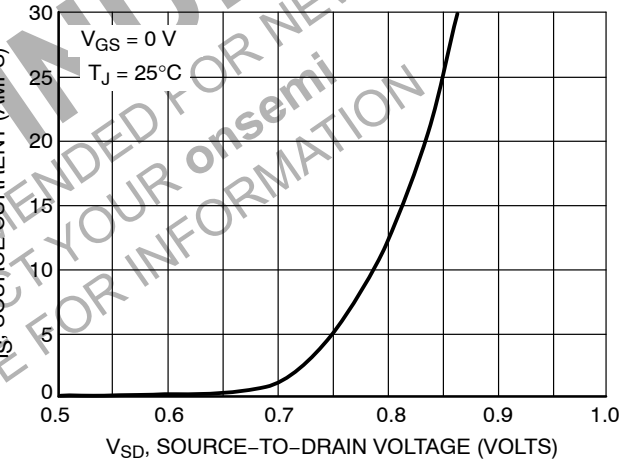


Figure 10. Diode Forward Voltage vs. Current

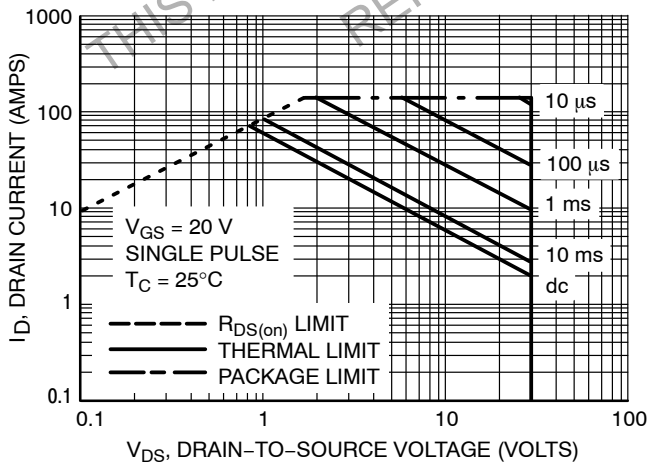


Figure 11. Maximum Rated Forward Biased Safe Operating Area

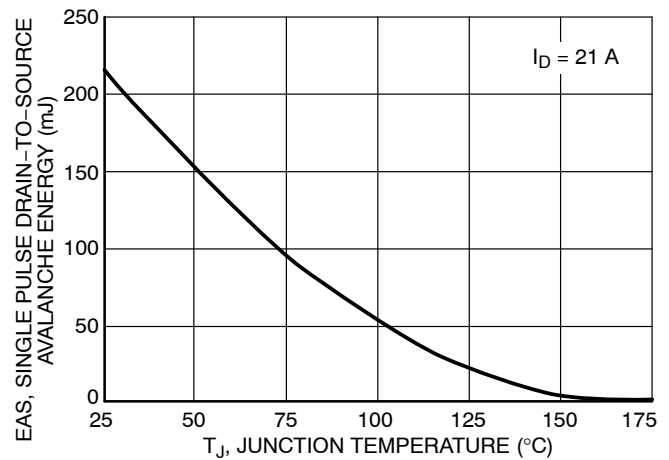


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTD4806N, NVD4806N

TYPICAL PERFORMANCE CURVES

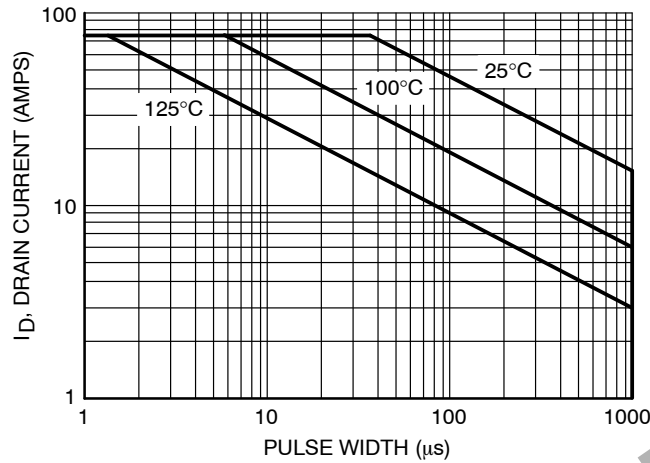


Figure 13. Avalanche Characteristics

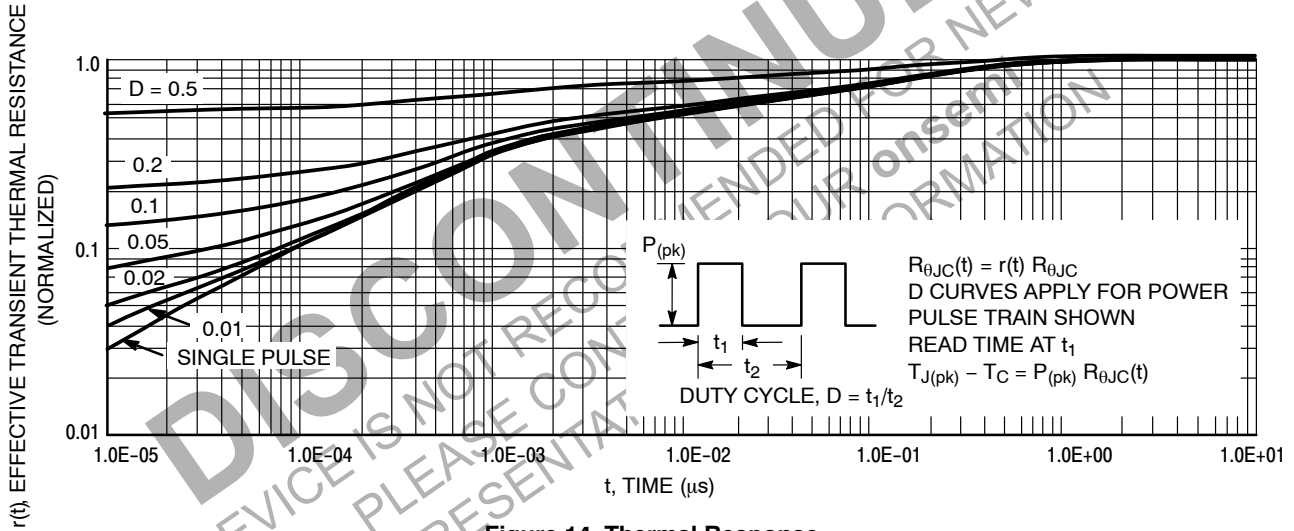
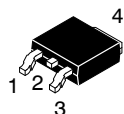


Figure 14. Thermal Response

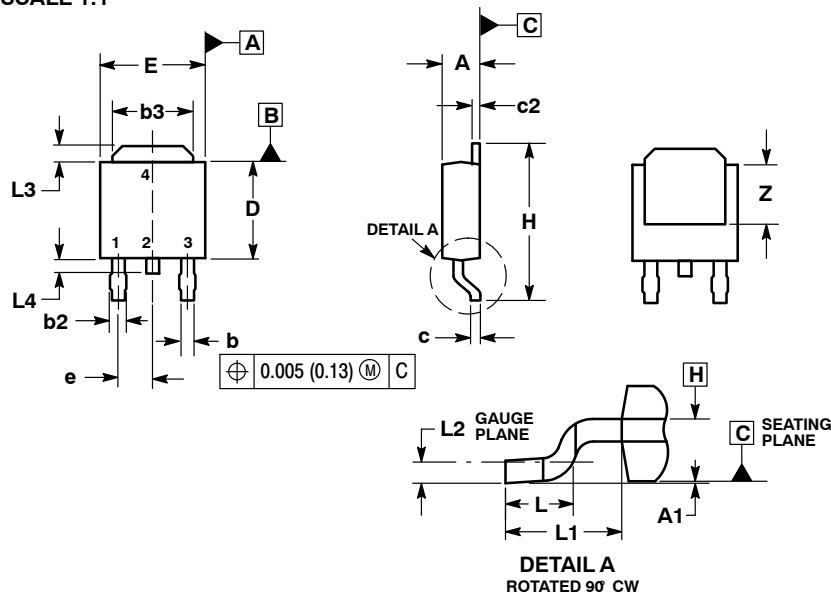
ORDERING INFORMATION

Order Number	Package	Shipping [†]
NTD4806NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD4806N-35G	IPAK Trimmed Lead (3.5 ± 0.15 mm) (Pb-Free)	75 Units / Rail
NVD4806NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD4806NT4G-VF01	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

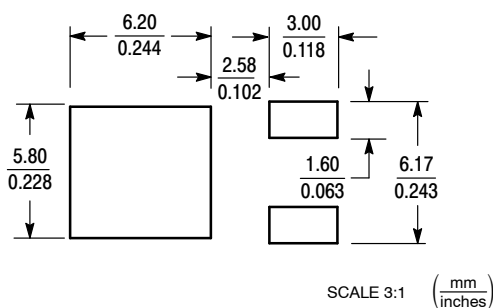
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

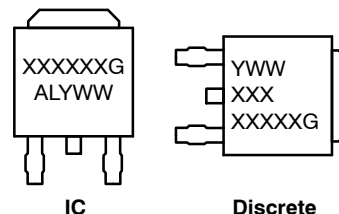
*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

GENERIC MARKING DIAGRAM*

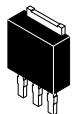


XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

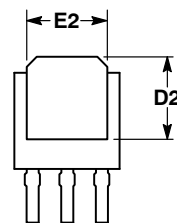
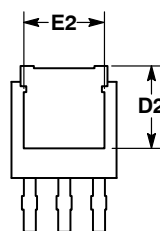
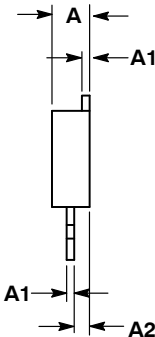
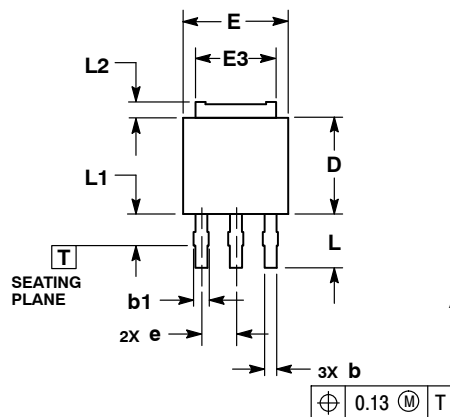
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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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3.5 MM IPAK, STRAIGHT LEAD
CASE 369AD
ISSUE B

DATE 18 APR 2013

SCALE 1:1


**OPTIONAL
CONSTRUCTION**
NOTES:

- 1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	---
E	6.35	6.73
E2	4.57	5.45
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	---	2.10
L2	0.89	1.27

**GENERIC MARKING
DIAGRAMS***
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

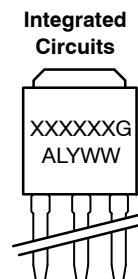
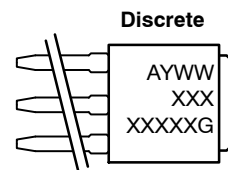
STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
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3. CATHODE
4. ANODE

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4. MT2

STYLE 7:
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3. EMITTER
4. COLLECTOR

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION: 3.5 MM IPAK, STRAIGHT LEAD

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