Low $V_{CE(sat)}$ NPN Transistors, 60 V, 1 A

NSS60101DMR6

ON Semiconductor's e[2]PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC−DC converters and LED lightning, power management…etc. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e[2]PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Base Voltage	V_{CBO}	80	Vdc
Emitter−Base Voltage	V_{EBO}	6	Vdc
Collector Current − Continuous	I_C	1	A
Collector Current − Peak	I_{CM}	2	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Ambient (Notes 1 and 2)	$R_{\theta JA}$	234	°C/W
Total Power Dissipation per Package @ T_A = 25°C (Note 2)	P_D	0.53	W
Thermal Resistance Junction−to−Ambient (Note 3)	$R_{\theta JA}$	300	°C/W
Power Dissipation per Transistor @ T_A = 25°C (Note 3)	P_D	0.40	W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

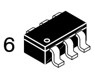
1. Per JESD51−7 with 100 mm^2 pad area and 2 oz. Cu (Dual Operation).
2. P_D per Transistor when both are turned on is one half of Total P_D or 0.53 Watts.
3. Per JESD51−7 with 100 mm^2 pad area and 2 oz. Cu (Single−Operation).

ON Semiconductor®

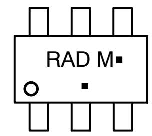
www.onsemi.com

60 Volt, 1 Amp
NPN Low $V_{CE(sat)}$ Transistors

MARKING DIAGRAM

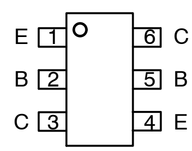


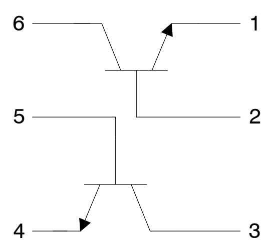
SC−74
CASE 318F



RAD = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS





ORDERING INFORMATION

Device	Package	Shipping†
NSS60101DMR6T1G	SC−74 (Pb−Free)	3000/Tape & Reel
NSS60101DMR6T2G		
NSV60101DMR6T1G		
NSV60101DMR6T2G		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (I_C = 10 mA, I_B = 0)	$V_{(BR)CEO}$	60			V
Collector−Base Breakdown Voltage (Ic = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	80			V
Emitter−Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)	$V_{(BR)EBO}$	6			V
Collector Cutoff Current (V_{CB} = 60 V, I_E = 0)	I_{CBO}			100	nA
Emitter Cutoff Current (V_{BE} = 5.0 V)	I_{EBO}			100	nA
ON CHARACTERISTICS					
DC Current Gain (Note 4)	h_{FE}				
(I_C = 100 mA, V_{CE} = 2 V)		200	320		
(I_C = 500 mA, V_{CE} = 2 V)		150	290		
(I_C = 1 A, V_{CE} = 2 V)		70	110		
(I_C = 1 mA, V_{CE} = 5 V)		250	335		
(I_C = 100 mA, V_{CE} = 5 V)		250	335		
(I_C = 500 mA, V_{CE} = 5 V)		200	310		
(I_C = 1 A, V_{CE} = 5 V)		100	295		
Collector−Emitter Saturation Voltage (Note 4)	$V_{CE(sat)}$				V
(I_C = 100 mA, I_B = 1 mA)			0.080	0.200	
(I_C = 500 mA, I_B = 50 mA)			0.078	0.150	
(I_C = 1 A, I_B = 50 mA)			0.170	0.250	
(I_C = 1 A, I_B = 100 mA)			0.143	0.200	
Base − Emitter Saturation Voltage (Note 4)	$V_{BE(sat)}$				V
(I_C = 500 mA, I_B = 50 mA)			0.87	1.50	
(I_C = 1 A, I_B = 50 mA)			0.91	1.50	
(I_C = 1 A, I_B = 100 mA)			0.94	1.60	
Base−Emitter Turn−on Voltage (Note 4)	$V_{BE(on)}$				V
(I_C = 1 mA, V_{CE} = 1 V)		0.27	0.57		
(I_C = 500 mA, V_{CE} = 2 V)			0.76	0.90	
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{EB} = 1 V, f = 1.0 MHz)	C_{ibo}		100		pF
Output Capacitance (V_{CB} = 10 V, f = 1.0 MHz)	C_{obo}		8.0		pF
Cutoff Frequency (I_C = 50 mA, V_{CE} = 2.0 V, f = 100 MHz)	f_T		200		MHz
SWITCHING TIMES					
Delay Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_d		10		ns
ON Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_{on}		28		ns
Rise Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_r		18		ns
Storage Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_s		622		ns
OFF Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_{off}		709		ns
Fall Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_f		87		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

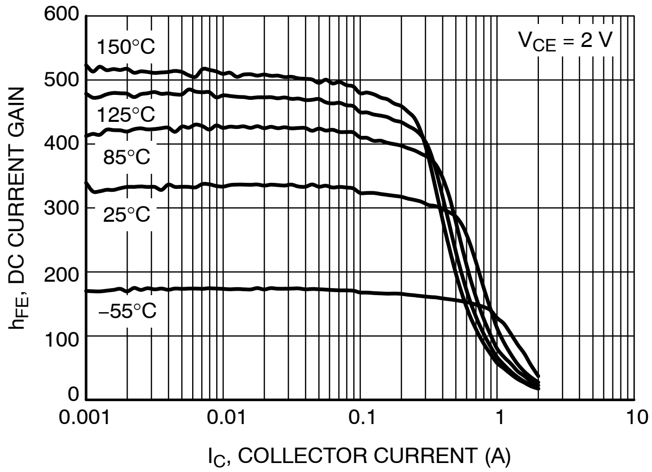


Figure 1. DC Current Gain

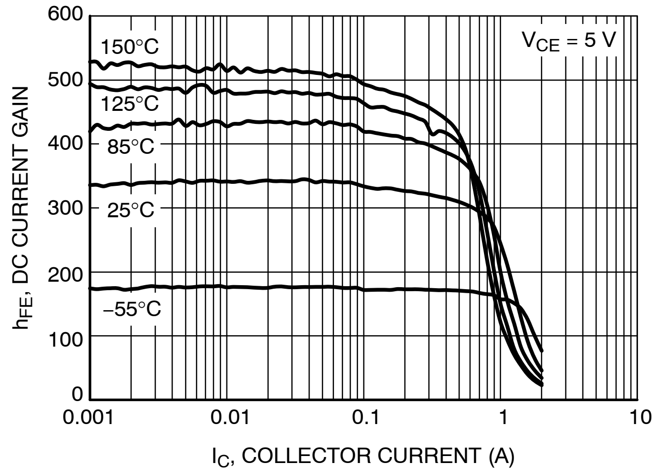


Figure 2. DC Current Gain

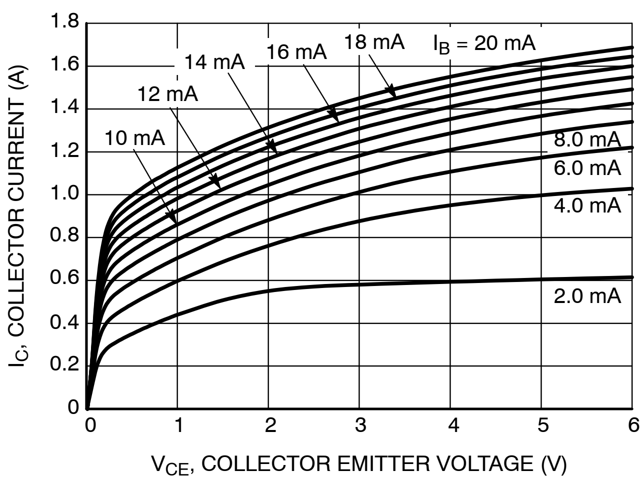


Figure 3. Collector Current as a Function of Collector Emitter Voltage

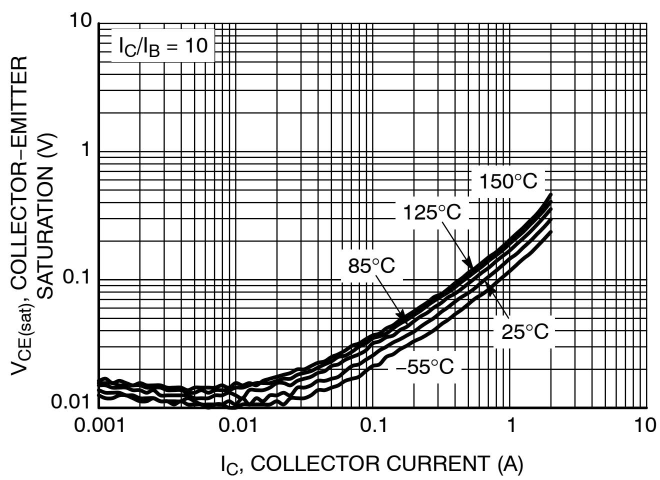


Figure 4. Collector−Emitter Saturation Voltage

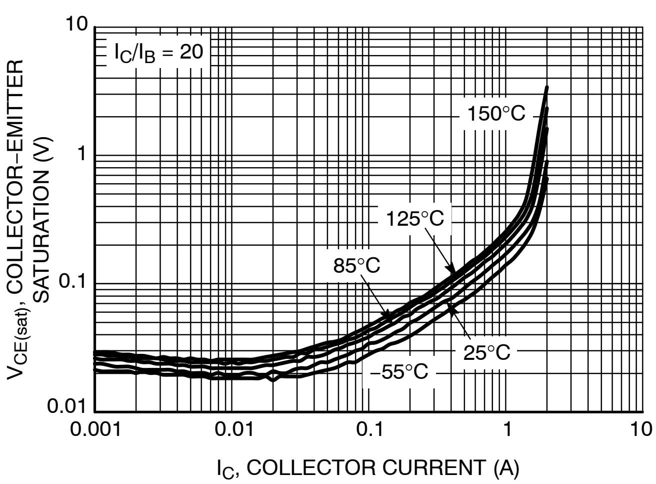


Figure 5. Collector−Emitter Saturation Voltage

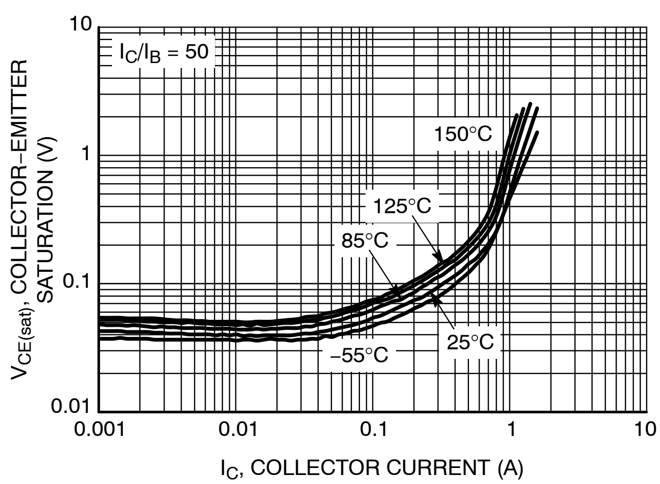


Figure 6. Collector−Emitter Saturation Voltage

TYPICAL CHARACTERISTICS

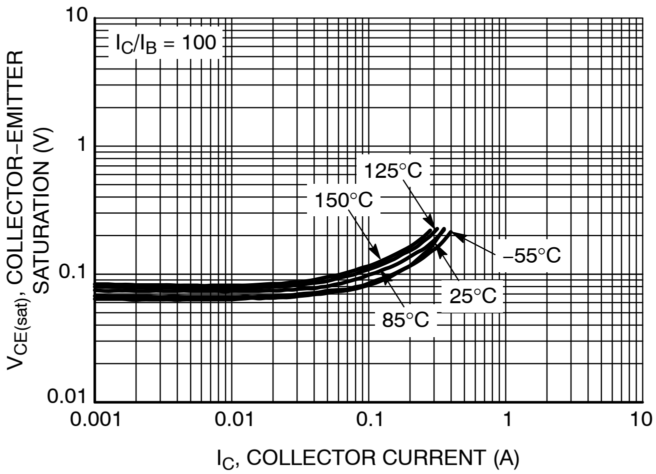


Figure 7. Collector−Emitter Saturation Voltage

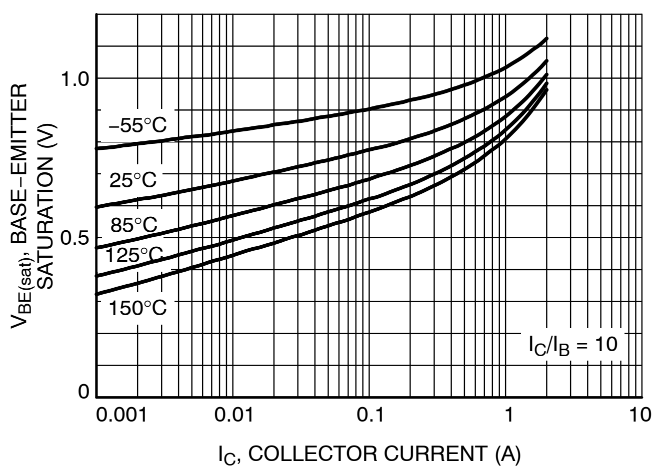


Figure 8. Base−Emitter Saturation Voltage

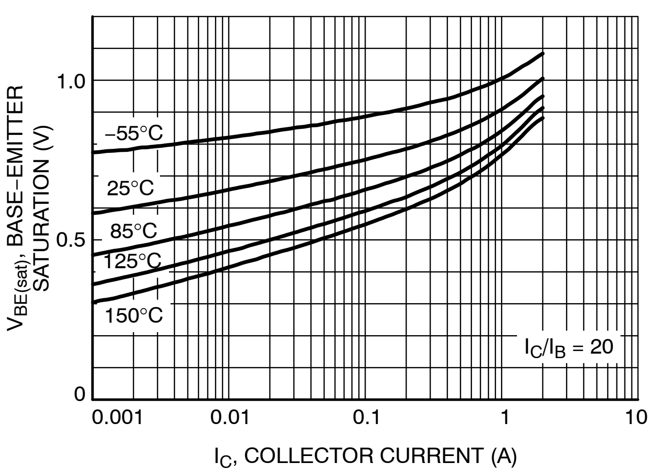


Figure 9. Base−Emitter Saturation Voltage

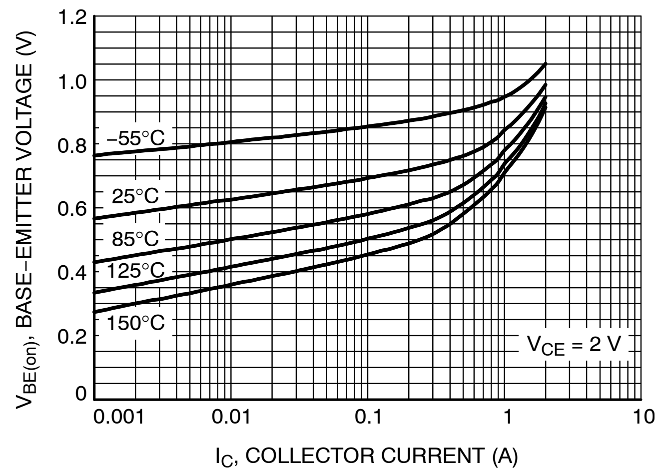


Figure 10. Base−Emitter "ON" Voltage

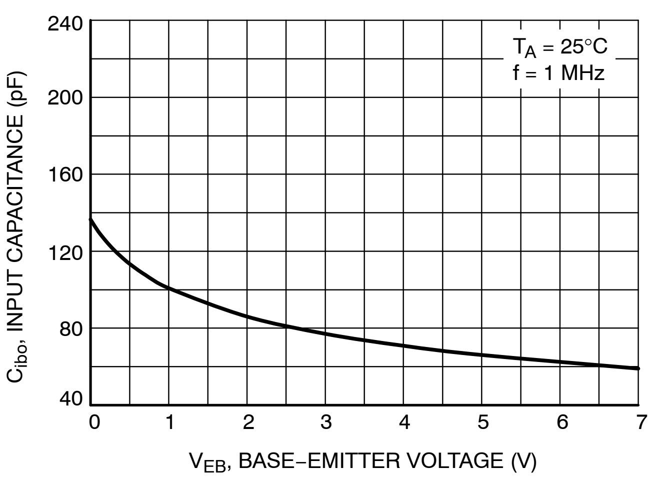


Figure 11. Input Capacitance

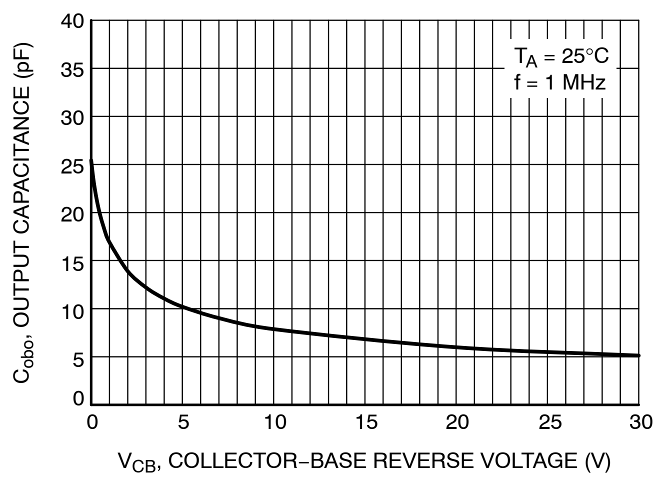


Figure 12. Output Capacitance

TYPICAL CHARACTERISTICS

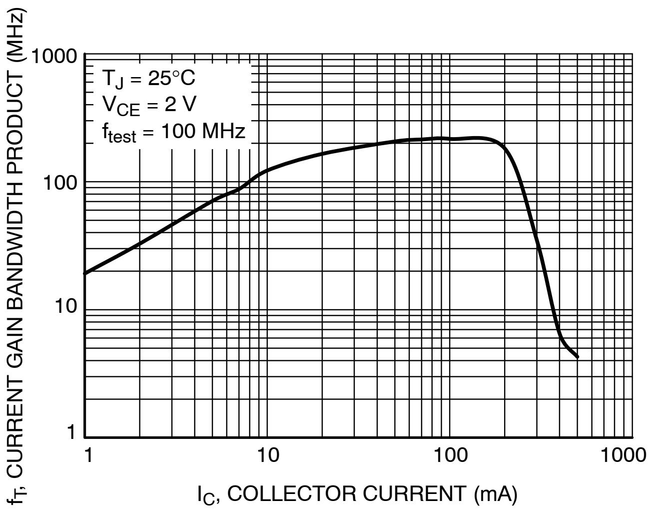


Figure 13. f_T, Current Gain Bandwidth Product

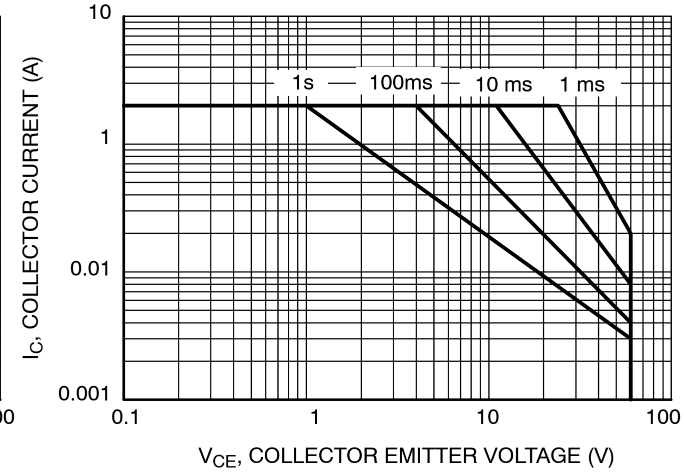


Figure 16. Safe Operating Area (T_A = 25°C)

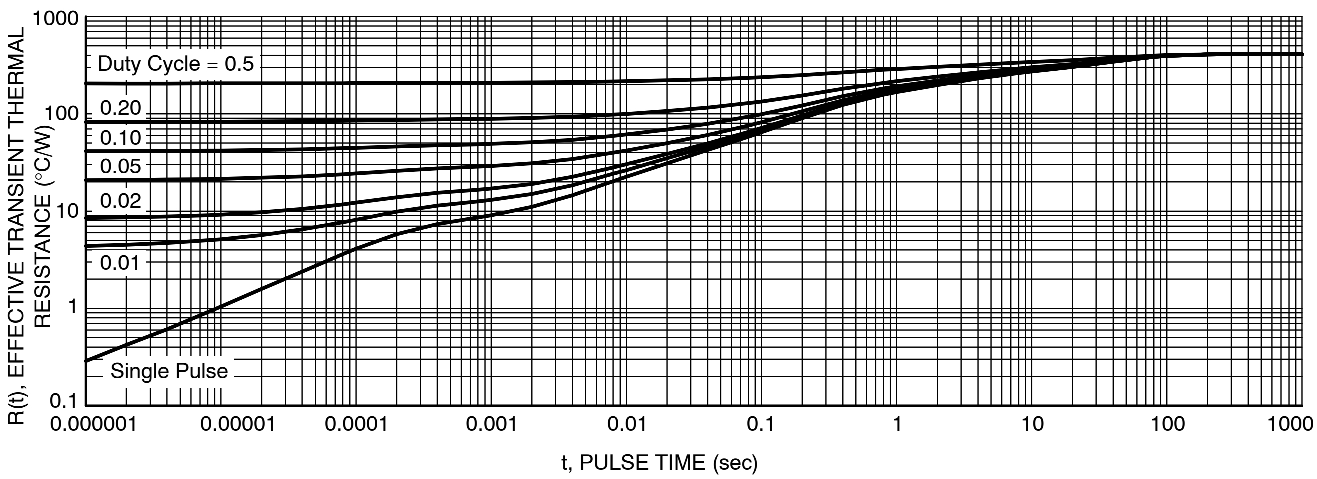


Figure 14. Thermal Resistance by Transistor

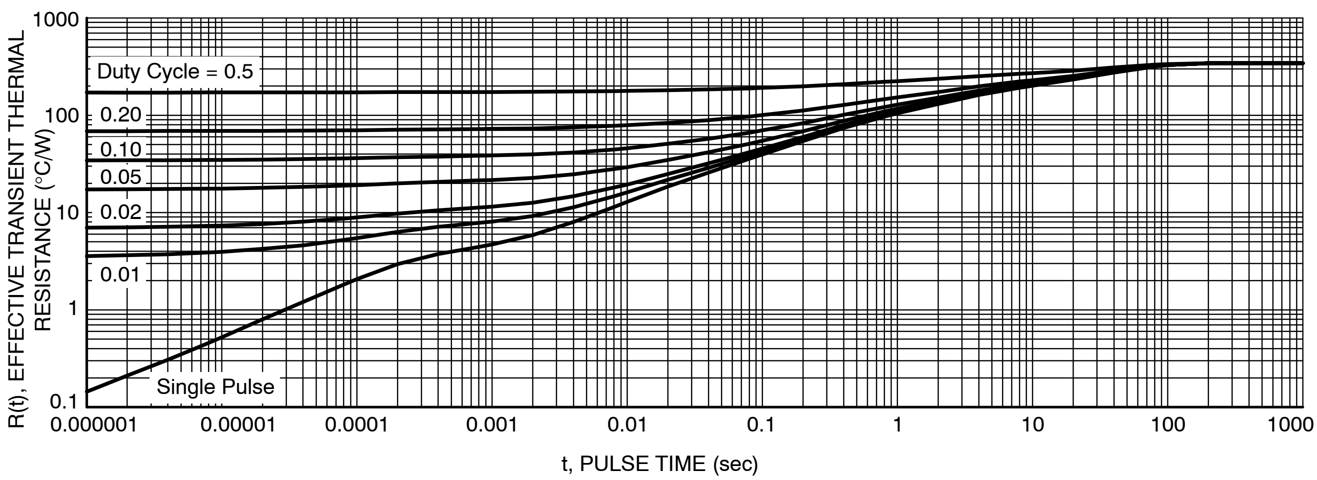
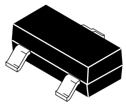


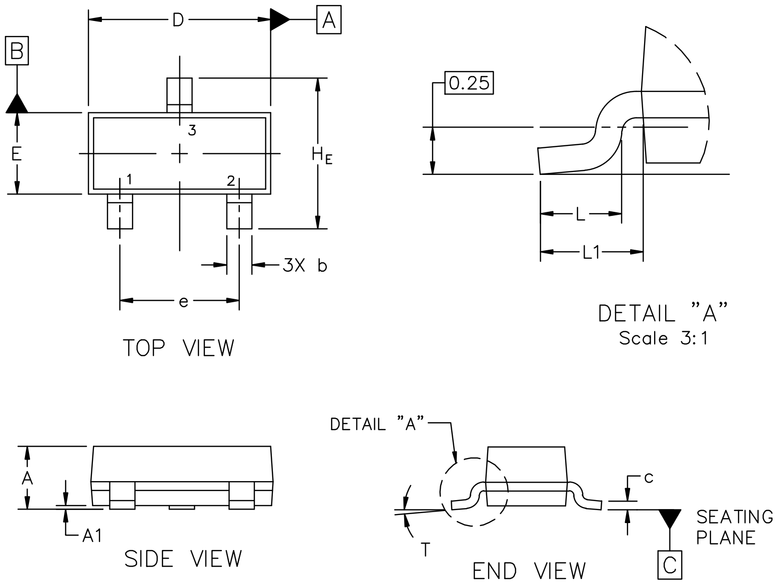
Figure 15. Thermal Resistance for Both Transistors



SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

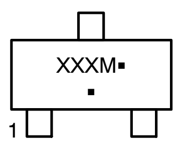
DATE 14 AUG 2024



DIM	MILLIMETERS MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

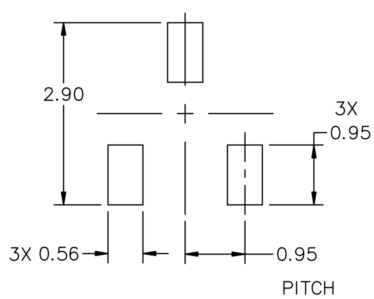
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
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SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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