

NIC9N05TS1, NIC9N05ATS1

Protected Power MOSFET

2.6 A, 52 V, N-Channel, Logic Level,
Clamped MOSFET w/ ESD Protection

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

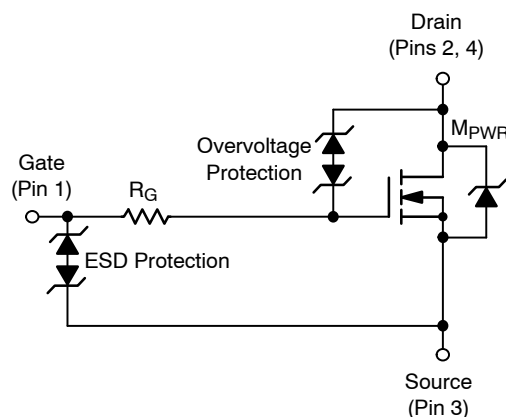
Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V_{DSS}	52–59	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 15	V
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	$^\circ\text{C}$
Electro-Static Discharge Capability (HBM) (MM)	ESD	5000 500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



ON Semiconductor®

<http://onsemi.com>



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NIC9N05TS1, NIC9N05ATS1

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified) (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (V _{GS} = 0 V, I _D = 1.0 mA, T _J = 25°C)	V _{(BR)DSS}	52	55	59	V
Zero Gate Voltage Drain Current (V _{DS} = 40 V, V _{GS} = 0 V)	I _{DSS}			10	μA
Gate-Body Leakage Current (V _{GS} = ±8 V, V _{DS} = 0 V) (V _{GS} = ±14 V, V _{DS} = 0 V)	I _{GSS}		±22	±10	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 100 μA)	V _{GS(th)}	1.3	1.75	2.5	V
Static Drain-to-Source On-Resistance (V _{GS} = 3.5 V, I _D = 0.6 A) (V _{GS} = 4.0 V, I _D = 1.5 A) (V _{GS} = 10 V, I _D = 2.6 A)	R _{DS(on)}		190 165 107	380 200 125	mΩ
SOURCE-DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	I _S = 2.6 A, V _{GS} = 0 V I _S = 2.6 A, V _{GS} = 0 V, T _J = 125°C	V _{SD}		0.81 0.66	1.5 V

1. Wafers tested prior to sawing.

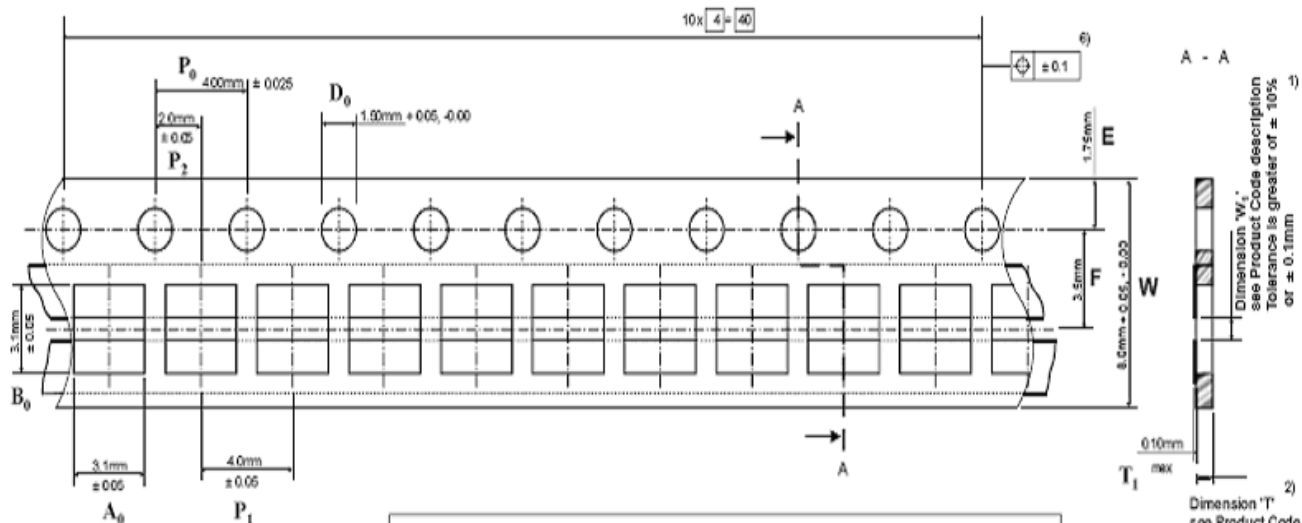
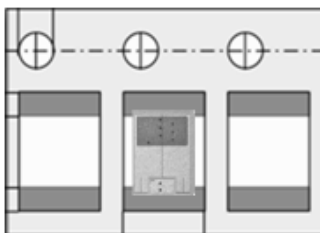
ORDERING INFORMATION

Device	Shipping
NIC9N05TS1	5000 / Reel
NIC9N05ATS1	5000 / Reel

NIC9N05TS1, NIC9N05ATS1

Layout view of the die in reel

Orientation A



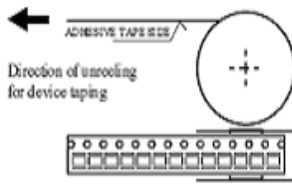
- NOTES**
1. W₁ is specified in the product description and is typically 50% of the component length as laid across the tape width. Tolerance of W₁ is ± 0.1mm or ± 10%, whichever is the greater.
 2. T₁ is specified in the product description and is always greater than the thickness of the component. Tolerance of T₁ is ± 10%.
 3. Total thickness of the tape is T = T₁.
 4. Main tape body volume conductivity 10⁴ to 10⁶ ohms per square. Material modified HIPS or ABS.
 5. Adhesive tape surface resistivity 10¹² ohms per square. Material Nibo SWT10 unless otherwise specified.
 6. Cumulative tolerance for 40 consecutive pitches is ± 0.1mm.

Product code description

S184T-W₁

T = .33, .45, .6, .7, or .85 (mm), as ordered
W₁ = 0.7 to 1.2 (mm) in increments of 0.1, as ordered

For example
S184 7-0.8
Type S184, T=0.7mm, W₁=0.7mm.



Change T0000 Drawing errors corrected - no change to dimensions or tolerances			
Property data Company confidential All rights reserved	Drawing according to ISO 9015 General tolerances ± 0.05mm	Scale 10:1	
		Date: 06/02/05	
		Name: Ken Ball	
		TEMPO ELECTRONICS www.surftape.com	
		ADHESIVE BACKED PUNCHED PLASTIC CARRIER TAPE	
		SURFTAPE®	

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[NIC9N05ATS1](#)