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TinyLogic UHS Dual Inverter

NC7WZ04

Description

The NC7WZ04 is a dual inverter from onsemi's Ultra-High Speed (UHS) series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range. The inputs tolerate voltages up to 5.5 V independent of V_{CC} operating voltage.

Features

- Ultra-High Speed: $t_{PD} = 2.3$ ns (Typical) into 50 pF at 5 V V_{CC}
- High Output Drive: ± 24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches Performance of LCX when Operated at 3.3 V V_{CC}
- Power Down High-Impedance Inputs / Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Space-Saving SC-88 6-Lead Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

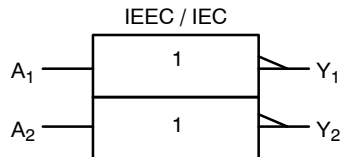
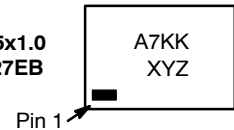


Figure 1. Logic Symbol

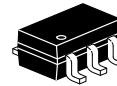
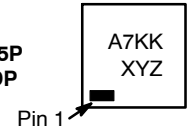
MARKING DIAGRAMS



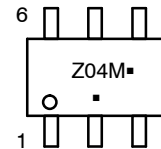
SIP6 1.45x1.0
CASE 127EB



UDFN6
1.0X1.0, 0.35P
CASE 517DP



SC-88
CASE 419B-02



A7, Z04 = Specific Device Code
KK = 2-Digit Lot Run Traceability Code
XY = 2-Digit Date Code Format
Z = Assembly Plant Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

Pin Configurations

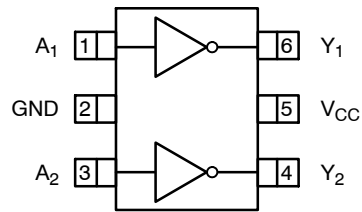


Figure 2. SC-88 (Top View)

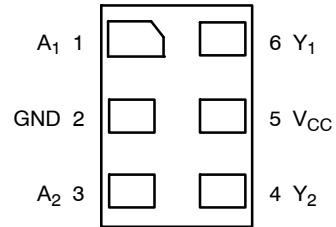
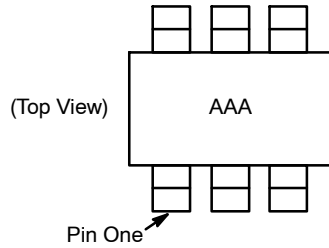


Figure 3. MicroPak (Top Through View)



NOTES:

1. AAA represents product code top mark (see *Ordering Information*).
2. Orientation of top mark determines pin one location.
3. Reading the top mark left to right, pin one is the lower left pin.

Figure 4. SC-88 Pin 1 Orientation

PIN DEFINITIONS

Pin # SC-88	Pin # MicroPak	Name	Description
1	1	A	Input
2	2	GND	Ground
3	3	A	Input
4	4	Y	Output
5	5	V _{CC}	Supply Voltage
6	6	Y	Output

FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply Voltage		-0.5	6.5	V
V _{IN}	DC Input Voltage		-0.5	6.5	V
V _{OUT}	DC Output Voltage		-0.5	6.5	V
I _{IK}	DC Input Diode Current	V _{IN} < 0 V	-	-50	mA
I _{OK}	DC Output Diode Current	V _{OUT} < 0 V	-	-50	mA
I _{OUT}	DC Output Source / Sink Current		-	±50	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current		-	±100	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
T _J	Junction Temperature Under Bias		-	+150	°C
T _L	Junction Lead Temperature (Soldering, 10 Seconds)		-	+260	°C
P _D	Power Dissipation in Still Air	SC-88	-	332	mW
		MicroPak-6	-	812	
		MicroPak2™-6	-	812	
ESD	Human Body Model, JEDEC: JESD22-A114		-	4000	V
	Charge Device Model, JEDEC: JESD22-C101		-	2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
V _{IN}	Input Voltage		0	5.5	V
V _{OUT}	Output Voltage		0	V _{CC}	V
t _r , t _f	Input Rise and Fall Times	V _{CC} at 1.8 V, 2.5 V ±0.2 V	0	20	ns/V
		V _{CC} at 3.3 V ±0.3 V	0	10	
		V _{CC} at 5.0 V ±0.5 V	0	5	
T _A	Operating Temperature		-40	+85	°C
θ _{JA}	Thermal Resistance	SC-88	-	377	°C/W
		MicroPak-6	-	154	
		MicroPak2-6	-	154	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must be held HIGH or LOW. They may not float.

NC7WZ04

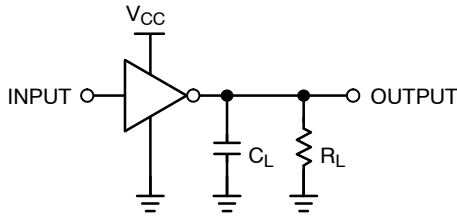
DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C			T _A = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage	1.65 to 1.95		0.65 V _{CC}	–	–	0.65 V _{CC}	–	V
		2.30 to 5.50		0.70 V _{CC}	–	–	0.70 V _{CC}	–	
V _{IL}	LOW Level Input Voltage	1.65 to 1.95		–	–	0.35 V _{CC}	–	0.35 V _{CC}	V
		2.30 to 5.50		–	–	0.30 V _{CC}	–	0.30 V _{CC}	
V _{OH}	HIGH Level Output Voltage	1.65	V _{IN} = V _{IH} or V _{IL} , I _{OH} = –100 µA	1.55	1.65	–	1.55	–	V
		1.80		1.70	1.80	–	1.70	–	
		2.30		2.20	2.30	–	2.20	–	
		3.00		2.90	3.00	–	2.90	–	
		4.50		4.40	4.50	–	4.40	–	
		1.65	I _{OH} = –4 mA	1.29	1.52	–	1.29	–	
		2.30	I _{OH} = –8 mA	1.90	2.14	–	1.90	–	
		3.00	I _{OH} = –16 mA	2.40	2.75	–	2.40	–	
		3.00	I _{OH} = –24 mA	2.30	2.62	–	2.30	–	
		4.50	I _{OH} = –32 mA	3.80	4.13	–	3.80	–	
V _{OL}	LOW Level Output Voltage	1.65	V _{IN} = V _{IH} or V _{IL} , I _{OL} = 100 µA	–	0.10	0.10	–	0.10	V
		1.80		–	0.00	0.10	–	0.10	
		2.30		–	0.00	0.10	–	0.10	
		3.00		–	0.00	0.10	–	0.10	
		4.50		–	0.00	0.10	–	0.10	
		1.65	I _{OL} = 4 mA	–	0.80	0.24	–	0.24	
		2.30	I _{OL} = 8 mA	–	0.10	0.30	–	0.30	
		3.00	I _{OL} = 16 mA	–	0.16	0.40	–	0.40	
		3.00	I _{OL} = 24 mA	–	0.24	0.55	–	0.55	
		4.50	I _{OL} = 32 mA	–	0.25	0.55	–	0.55	
I _{IN}	Input Leakage Current	1.65 to 5.5	0 ≤ V _{IN} ≤ 5.5 V	–	–	±1	–	±1.0	µA
I _{OFF}	Power Off Leakage Current	0	V _{IN} or V _{OUT} = 5.5 V	–	–	1	–	10	µA
I _{CC}	Quiescent Supply Current	1.65 to 5.50	V _{IN} = 5.5 V, GND	–	–	1	–	10	µA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C			T _A = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay (Figure 5, 6)	1.65	C _L = 15 pF, R _L = 1 MΩ	–	5.3	9.2	–	11.0	ns
		1.80		–	4.4	7.6	–	8.4	
		2.50 ±0.20		–	3.0	5.1	–	5.6	
		3.30 ±0.30		–	2.2	3.4	–	3.8	
		5.00 ±0.50		–	1.8	2.8	–	3.1	
		3.30 ±0.30	C _L = 50 pF, R _L = 500 Ω	–	2.9	4.5	–	5.0	
		5.00 ±0.50		–	2.3	3.6	–	4.0	
C _{IN}	Input Capacitance	0.00		–	2.5	–	–	–	pF
C _{PD}	Power Dissipation Capacitance (Note 5) (Figure 7)	3.30		–	9	–	–	–	pF
		5.00		–	11	–	–	–	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CCstatic})$.



NOTE:

6. C_L includes load and stray capacitance.
7. Input PRR = 1.0 MHz, t_W = 500 ns.

Figure 5. AC Test Circuit

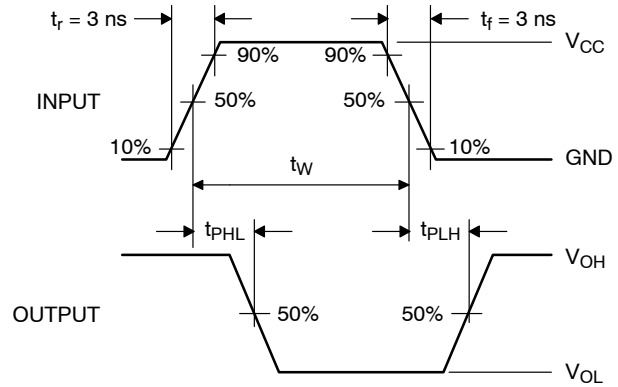
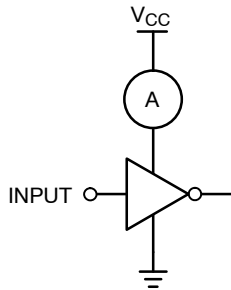


Figure 6. AC Waveforms



NOTE:

8. Input = AC Waveform; t_r = t_f = 1.8 ns.
9. PRR = Variable; Duty Cycle = 50%.

Figure 7. I_{CCD} Test Circuit

NC7WZ04

DEVICE ORDERING INFORMATION

Device	Top Mark	Packages	Shipping [†]
NC7WZ04P6X	Z04	6-Lead SC70, EIAJ SC-88, 1.25 mm Wide	3000 / Tape & Reel
NC7WZ04L6X	A7	6-Lead MicroPak, 1.00 mm Wide	5000 / Tape & Reel
NC7WZ04FHX	A7	6-Lead, MicroPak2, 1x1 mm Body, .35 mm Pitch	5000 / Tape & Reel

DISCONTINUED (Note 10)

NC7WZ04P6X-L22347	Z04	6-Lead SC70, EIAJ SC-88, 1.25 mm Wide	3000 / Tape & Reel
NC7WZ04L6X-L22175	A7	6-Lead MicroPak, 1.00 mm Wide	5000 / Tape & Reel
NC7WZ04FHX-L22175	A7	6-Lead, MicroPak2, 1x1 mm Body, .35 mm Pitch	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

10. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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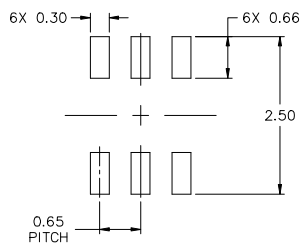


SC-88 2.00x1.25x0.90, 0.65P
CASE 419B-02
ISSUE Z

DATE 18 APR 2024

NOTES:

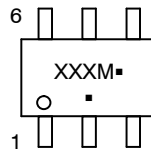
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		

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SC-88 2.00x1.25x0.90, 0.65P
CASE 419B-02
ISSUE Z

DATE 18 APR 2024

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. I OUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

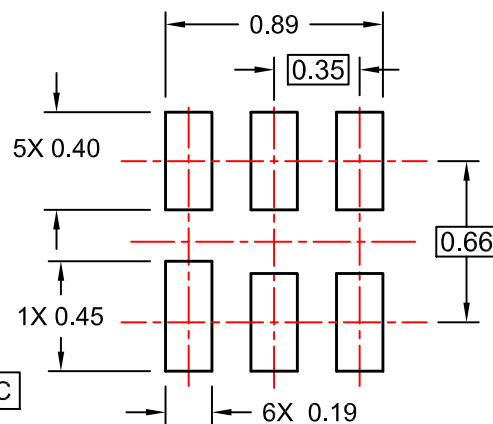
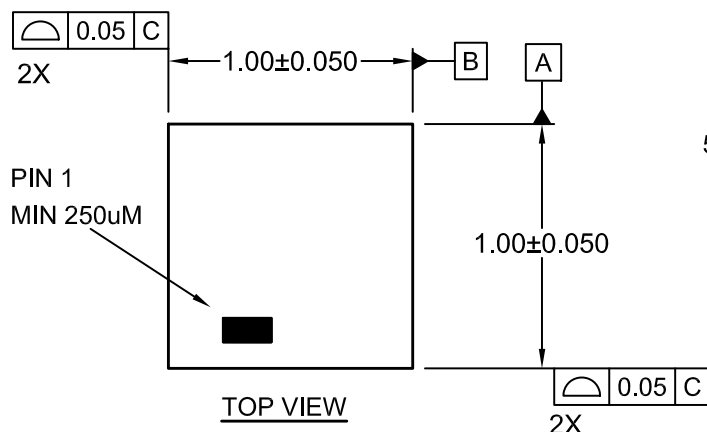
Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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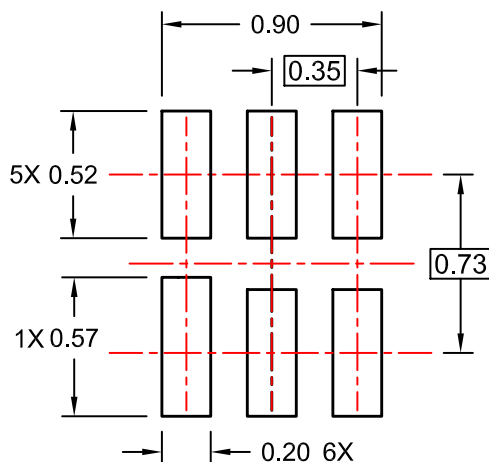
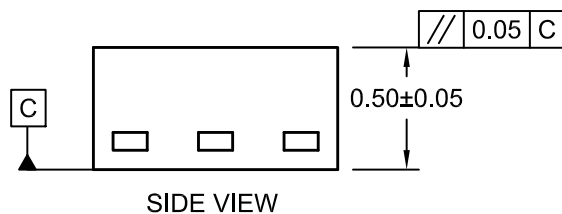
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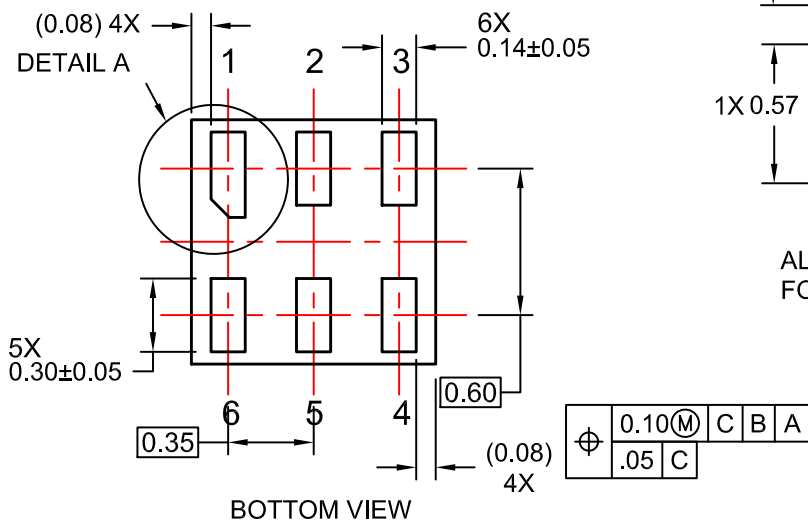
DATE 31 AUG 2016



RECOMMENDED LAND PATTERN FOR SPACE CONSTRAINED PCB

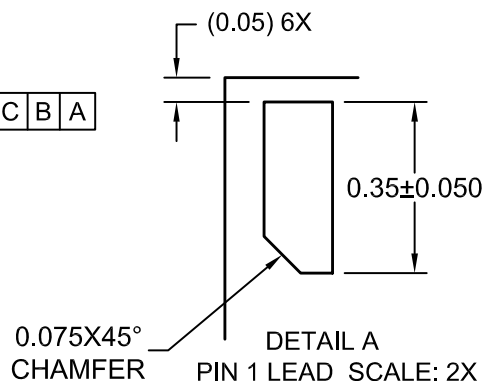


ALTERNATIVE LAND PATTERN FOR UNIVERSAL APPLICATION



NOTES:

- A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009



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