

# TinyLogic HST 2-Input NAND Gate

## NC7ST00

### Description

The NC7ST00 is a single 2-Input high performance CMOS NAND Gate, with TTL-compatible inputs. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation. ESD protection diodes inherently guard both inputs and output with respect to the V<sub>CC</sub> and GND rails. High gain circuitry offers high noise immunity and reduced sensitivity to input edge rate. The TTL-compatible inputs facilitate TTL to NMOS / CMOS interfacing. Device performance is similar to MM74HCT but with 1/2 the output current drive of HC / HCT.

### Features

- Space Saving SC-74A and SC-88A 5-Lead Package
- Ultra Small MicroPak™ Leadless Package
- High Speed:  $t_{PD} < 7$  ns Typ,  $V_{CC} = 5$  V,  $C_L = 15$  pF
- Low Quiescent Power:  $I_{CC} < 1$   $\mu$ A Typ,  $V_{CC} = 5.5$  V
- Balanced Output Drive: 2 mA I<sub>OL</sub>, -2 mA I<sub>OH</sub>
- TTL-compatible Inputs
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

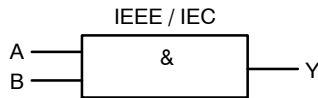


Figure 1. Logic Symbol



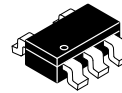
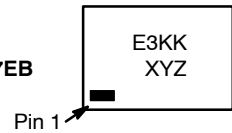
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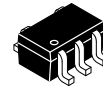
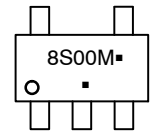
### MARKING DIAGRAMS



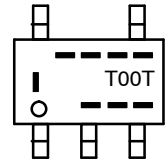
SIP6  
CASE 127EB



SC-74A  
CASE 318BQ



SC-88A  
CASE 419A-02



E3, 8S00, T00 = Specific Device Code  
 KK = 2-Digit Lot Run Traceability Code  
 XY = 2-Digit Date Code Format  
 Z = Assembly Plant Code  
 M = Date Code  
 ■ = Pb-Free Package  
 T = Die Run Code  
 - - - - = Year Coding Scheme  
 | - - = Plant Code Identifier  
 - - - = Eight-Week Datacoding Scheme

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

# NC7ST00

## Pin Configurations

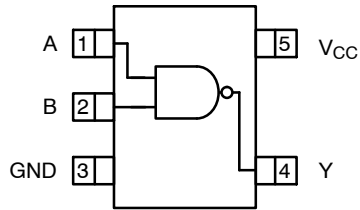


Figure 2. SC-88A and SC-74A (Top View)

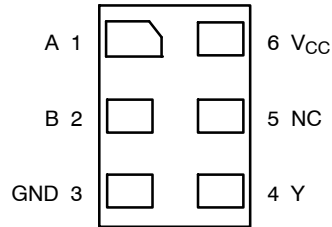


Figure 3. MicroPak (Top Through View)

## PIN DESCRIPTIONS

Pin Names	Description
A, B	Inputs
Y	Output
NC	No Connect

## FUNCTION TABLE ( $Y = \overline{AB}$ )

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level  
L = LOW Logic Level

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	Supply Voltage	-0.5	6.5	V	
$I_{IK}$	DC Input Diode Current	$V_{IN} < -0.5\text{ V}$	-	-20	mA
		$V_{IN} \geq V_{CC} + 0.5\text{ V}$	-	+20	
$V_{IN}$	DC Input Voltage	-0.5	$V_{CC} + 0.5$	V	
$I_{OK}$	DC Output Diode Current	$V_{OUT} < -0.5\text{ V}$	-	-20	mA
		$V_{OUT} > V_{CC} + 0.5\text{ V}$	-	+20	
$V_{OUT}$	Output Voltage	-0.5	$V_{CC} + 0.5$	V	
$I_{OUT}$	DC Output Source or Sink Current	-	$\pm 12.5$	mA	
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Supply Pin	-	$\pm 25$	mA	
$T_{STG}$	Storage Temperature	-65	+150	$^{\circ}\text{C}$	
$T_J$	Junction Temperature	-	+150	$^{\circ}\text{C}$	
$T_L$	Lead Temperature (Soldering, 10 Seconds)	-	+260	$^{\circ}\text{C}$	
$P_D$	Power Dissipation in Still Air	SC-74A	-	225	mW
		SC-88A	-	190	
		MicroPak	-	327	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# NC7ST00

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage		4.5	5.5	V
V <sub>IN</sub>	Input Voltage		0	V <sub>CC</sub>	V
V <sub>OUT</sub>	Output Voltage		0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 5.0 V	0	500	ns
θ <sub>JA</sub>	Thermal Resistance	SC-74A	-	555	°C/W
		SC-88A	-	659	
		MicroPak	-	382	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- Unused inputs must be held HIGH or LOW. They may not float.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage	4.5 – 5.5		2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW Level Input Voltage	4.5 – 5.5		-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	4.5 4.5	I <sub>OH</sub> = -20 μA I <sub>OH</sub> = -2 mA V <sub>IN</sub> = V <sub>IL</sub>	4.4 4.18	4.5 4.35	-	4.4 4.13	-	V
V <sub>OL</sub>	LOW Level Output Voltage	4.5 4.5	I <sub>OL</sub> = 20 μA I <sub>OL</sub> = 2 mA V <sub>IN</sub> = V <sub>IH</sub>	-	0 0.10	0.1 0.26	-	0.1 0.33	V
I <sub>IN</sub>	Input Leakage Current	5.5	0 ≤ V <sub>IN</sub> ≤ 5.5 V	-	-	±0.1	-	±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND	-	-	1.0	-	10.0	μA
I <sub>CCT</sub>	I <sub>CC</sub> per Input	5.5	One Input V <sub>IN</sub> = 0.5 V or 2.4 V, Other Input V <sub>CC</sub> or GND	-	-	2.0	-	2.9	mA

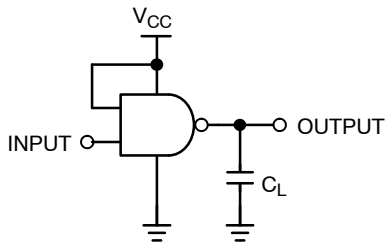
## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay (Figure 4, 6)	5.0	C <sub>L</sub> = 15 pF	-	3.4	12	-	-	ns
				-	6.3	17	-	-	
		4.5	C <sub>L</sub> = 50 pF	-	6.0	16	-	20	
				-	11.5	27	-	31	
		5.5	C <sub>L</sub> = 50 pF	-	4.1	14	-	18	
				-	11.2	26	-	30	
t <sub>TLH</sub> , t <sub>THL</sub>	Output Transition Time (Figure 4, 6)	5.0	C <sub>L</sub> = 15 pF	-	4	10	-	-	ns
		4.5	C <sub>L</sub> = 50 pF	-	11	25	-	31	
		5.5	C <sub>L</sub> = 50 pF	-	10	21	-	26	
C <sub>IN</sub>	Input Capacitance	Open		-	2	10	-	-	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Figure 5)	5.0	(Note 2)	-	6	-	-	-	pF

- C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current. Current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 5). C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression: I<sub>CCD</sub> = (C<sub>PD</sub>) (V<sub>CC</sub>) (f<sub>IN</sub>) + (I<sub>CCstatic</sub>).

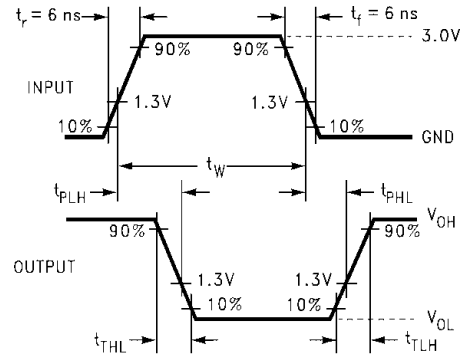
# NC7ST00

## AC Loading and Waveforms

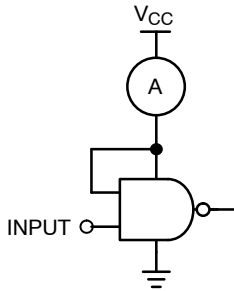


$C_L$  includes load and stray capacitance  
Input PRR = 1.0 MHz,  $t_W = 500$  ns

**Figure 4. AC Test Circuit**



**Figure 6. AC Waveforms**



Input = AC Waveform;  
PRR = Variable; Duty Cycle = 50%.

**Figure 5.  $I_{CCD}$  Test Circuit**

## ORDERING INFORMATION

Device	Top Mark	Packages	Shipping†
NC7ST00M5X	8S00	SC-74A	3000 / Tape & Reel
NC7ST00P5X	T00	SC-88A	3000 / Tape & Reel
NC7ST00L6X	E3	SIP6, MicroPak	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

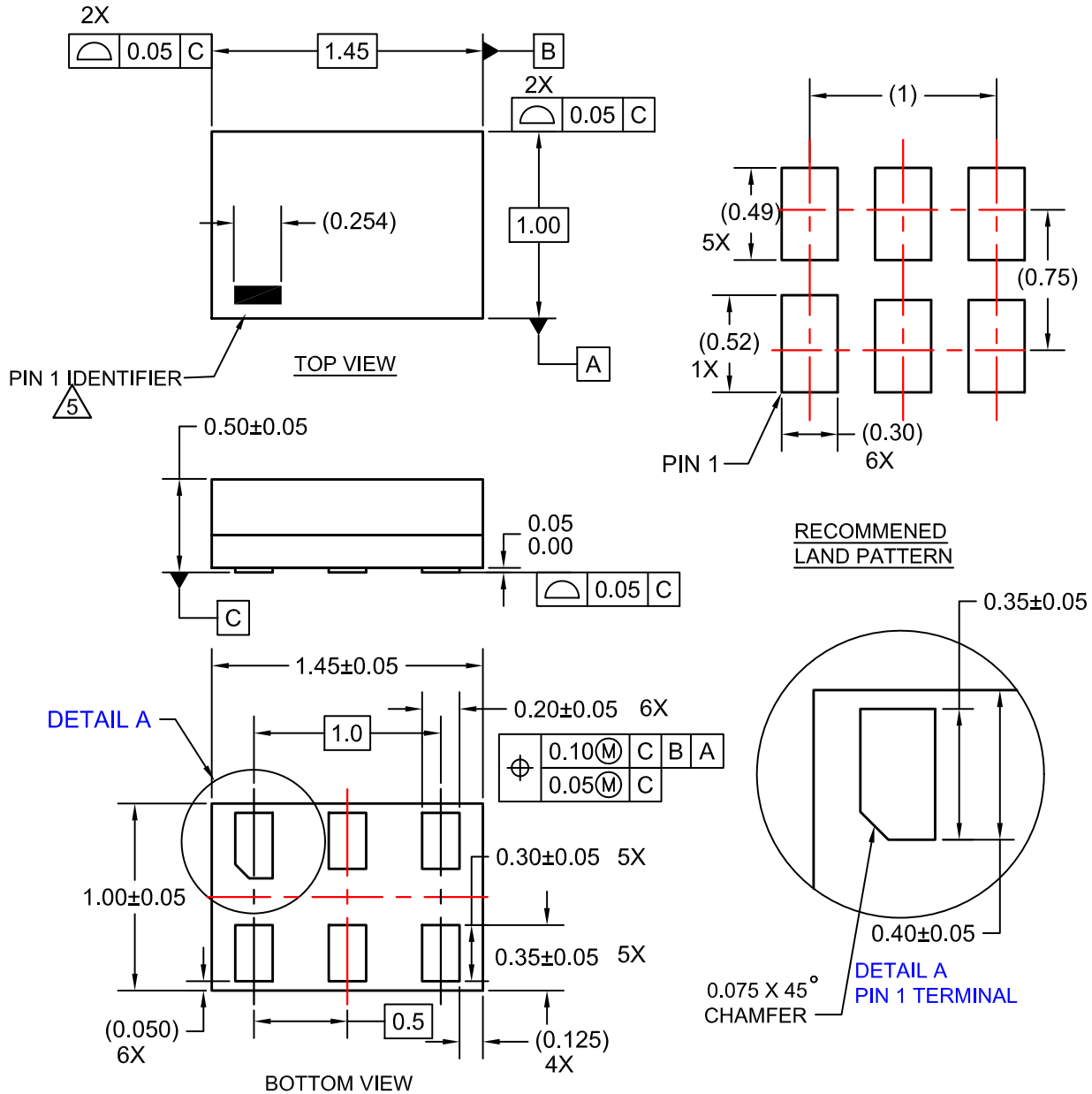
## PACKAGE DIMENSIONS

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SIP6 1.45X1.0  
CASE 127EB  
ISSUE O

DATE 31 AUG 2016



**NOTES:**

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

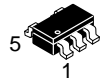
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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

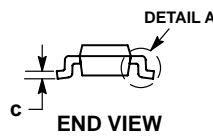
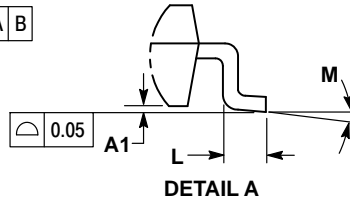
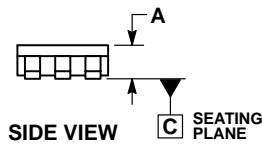
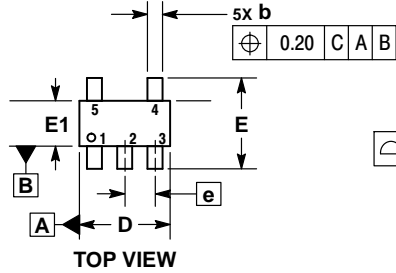
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SCALE 2:1

### SC-74A CASE 318BQ ISSUE B

DATE 18 JAN 2018

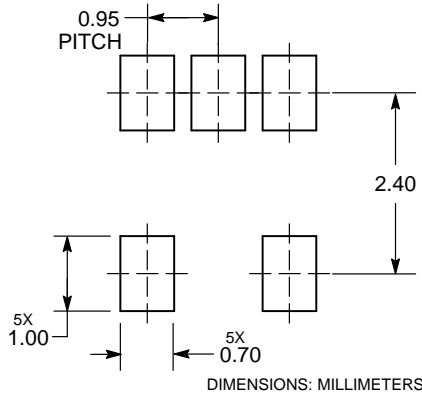


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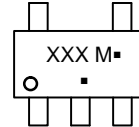
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0°	10°

#### RECOMMENDED SOLDERING FOOTPRINT\*



#### GENERIC MARKING DIAGRAM\*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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STATUS:	ON SEMICONDUCTOR STANDARD	
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DESCRIPTION:	SC-74A	PAGE 1 OF 2



# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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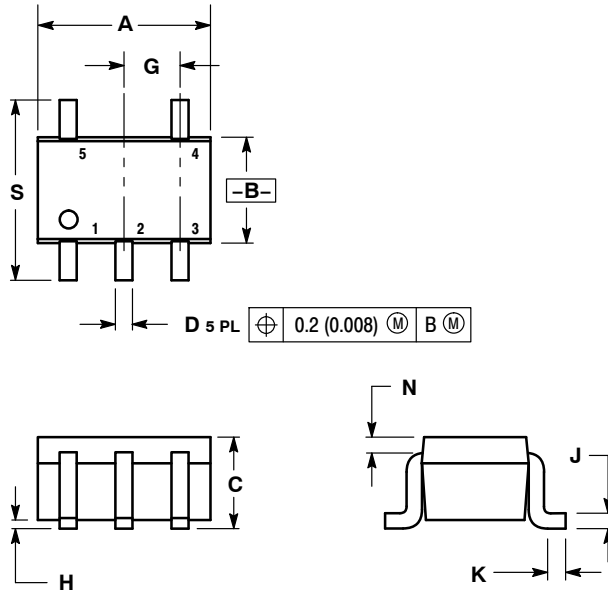
### SC-88A (SC-70-5/SOT-353)

#### CASE 419A-02

#### ISSUE L

SCALE 2:1

DATE 17 JAN 2013

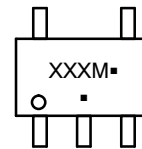


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

### GENERIC MARKING DIAGRAM\*

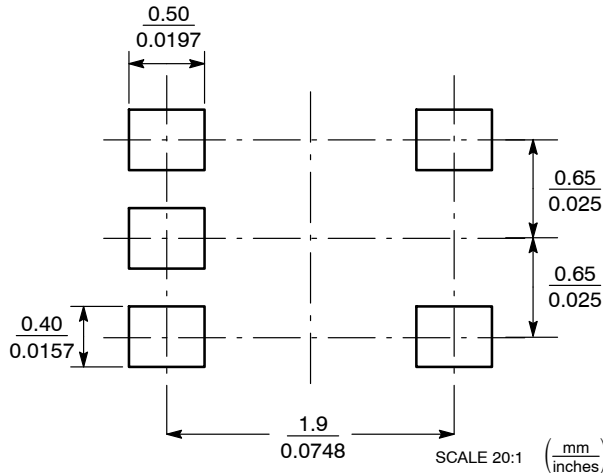


- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDER FOOTPRINT



STYLE 1:  
PIN 1. BASE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. COLLECTOR

STYLE 2:  
PIN 1. ANODE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. CATHODE

STYLE 3:  
PIN 1. ANODE 1  
2. N/C  
3. ANODE 2  
4. CATHODE 2  
5. CATHODE 1

STYLE 4:  
PIN 1. SOURCE 1  
2. DRAIN 1/2  
3. SOURCE 1  
4. GATE 1  
5. GATE 2

STYLE 5:  
PIN 1. CATHODE  
2. COMMON ANODE  
3. CATHODE 2  
4. CATHODE 3  
5. CATHODE 4

STYLE 6:  
PIN 1. EMITTER 2  
2. BASE 2  
3. EMITTER 1  
4. COLLECTOR  
5. COLLECTOR 2/BASE 1

STYLE 7:  
PIN 1. BASE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. COLLECTOR

STYLE 8:  
PIN 1. CATHODE  
2. COLLECTOR  
3. N/C  
4. BASE  
5. EMITTER

STYLE 9:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. ANODE

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