MSB92ASWT1G, MSB92AS1WT1G

PNP Silicon General Purpose High Voltage Transistor

This PNP Silicon Planar Transistor is designed for general purpose amplifier applications. This device is housed in the SC-70/SOT-323 package which is designed for low power surface mount applications.

Features

- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{(BR)CBO}$	−300	Vdc
Collector-Emitter Voltage	$V_{(BR)CEO}$	−300	Vdc
Emitter-Base Voltage	$V_{(BR)EBO}$	−5.0	Vdc
Collector Current − Continuous	I_C	500	mAdc
ESD Rating: Human Body Model Machine Model	ESD	Class 1C Class C	−

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Power Dissipation (Note 1)	P_D	150	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.

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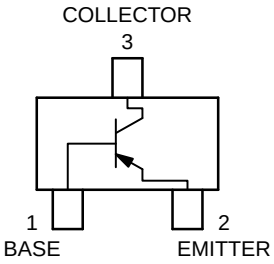
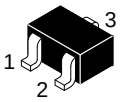
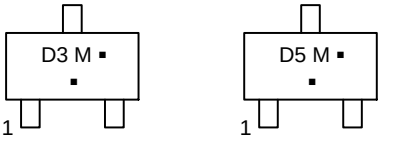




SC−70 (SOT−323)
CASE 419
STYLE 3

MARKING DIAGRAM



MSB92ASWT1G MSB92AS1WT1G

Dx = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MSB92ASWT1G	SC−70 (Pb−Free)	3000/Tape & Reel
MSB92AS1WT1G	SC−70 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Collector-Emitter Breakdown Voltage (I_C = −1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−300	−	Vdc
Collector-Base Breakdown Voltage (I_C = −100 μAdc, I_E = 0)	$V_{(BR)CBO}$	−300	−	Vdc
Emitter-Base Breakdown Voltage (I_E = −100 μAdc, I_E = 0)	$V_{(BR)EBO}$	−5.0	−	Vdc
Collector-Base Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	−	−0.25	μA
Emitter−Base Cutoff Current (V_{EB} = −3.0 Vdc, I_B = 0)	I_{EBO}	−	−0.1	μA
DC Current Gain (Note 2) (V_{CE} = −10 Vdc, I_C = −1.0 mAdc) (V_{CE} = −10 Vdc, I_C = −10 mAdc) (V_{CE} = −10 Vdc, I_C = −30 mAdc)	 h_{FE1} h_{FE2} h_{FE3}	 120 40 25	 200 − −	−
Collector-Emitter Saturation Voltage (Note 2) (I_C = −20 mAdc, I_B = −2.0 mAdc)	$V_{CE(sat)}$	−	−0.5	Vdc
Base−Emitter Saturation Voltage (I_C = −20 mAdc, I_B = −2.0 mAdc)	$V_{BE(sat)}$	−	−0.9	Vdc

SMALL SIGNAL CHARACTERISTICS

Current−Gain − Bandwidth Product (I_C = −10 mAdc, V_{CE} = −20 Vdc, f = 20 MHz)	f_T	50	−	MHz
Collector−Base Capacitance (V_{CB} = −20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	−	6.0	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, D.C. ≤ 2%.

TYPICAL CHARACTERISTICS

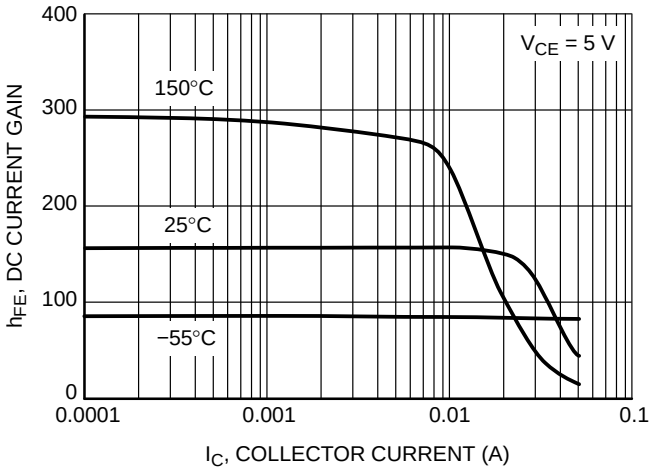


Figure 1. DC Current Gain

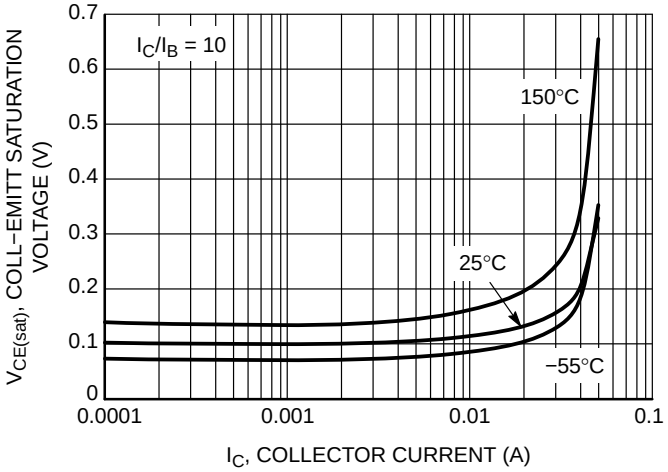


Figure 2. $V_{CE(sat)}$ Curve

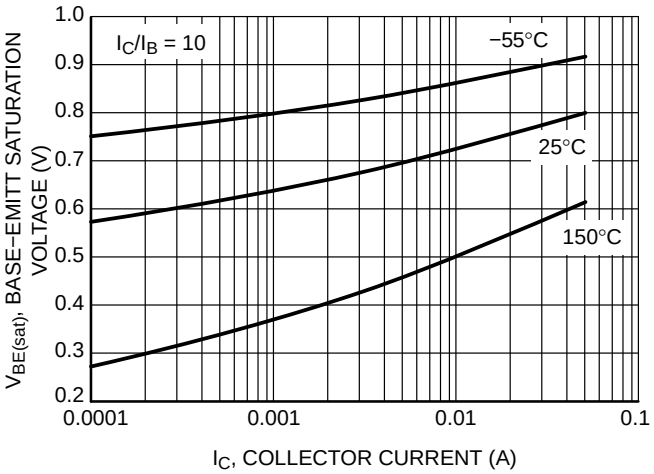


Figure 3. $V_{BE(sat)}$ Curve

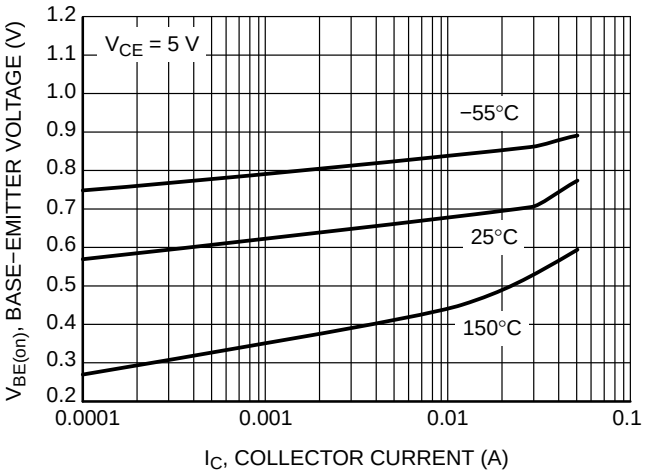


Figure 4. $V_{BE(on)}$ Curve

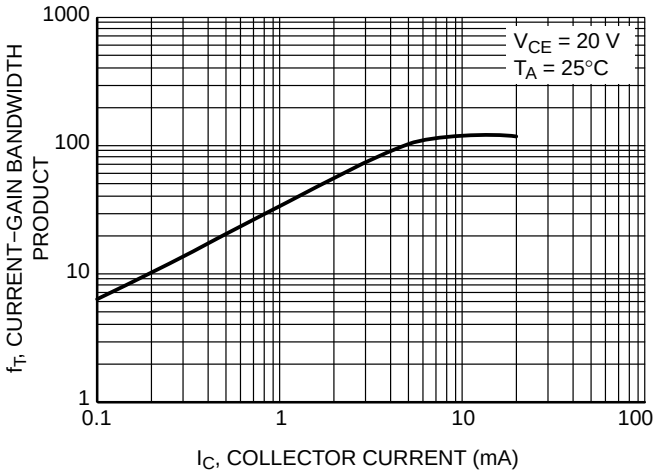


Figure 5. Current−Gain Bandwidth Product

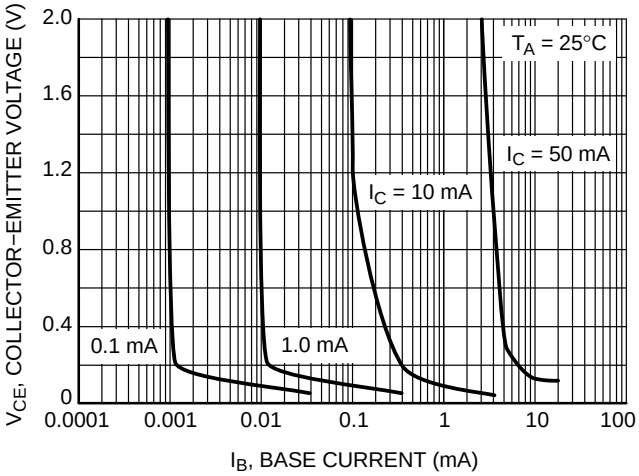


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

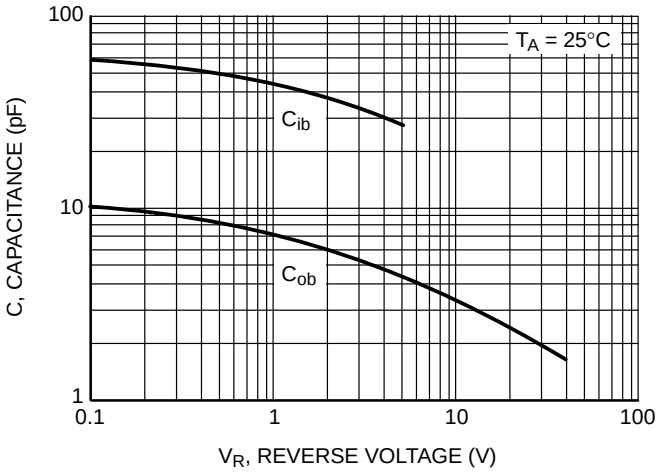


Figure 7. Capacitance

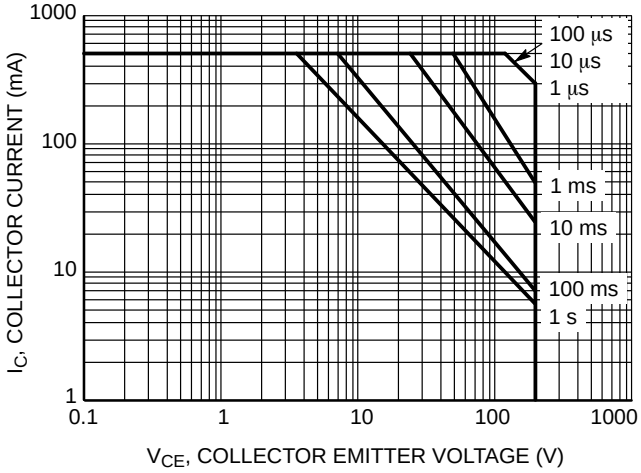
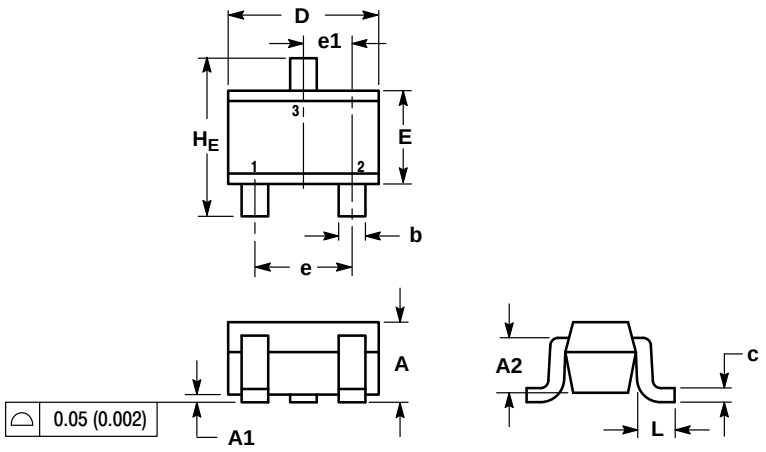


Figure 8. Safe Operating Area

PACKAGE DIMENSIONS

SC−70 (SOT−323)
CASE 419−04
ISSUE N

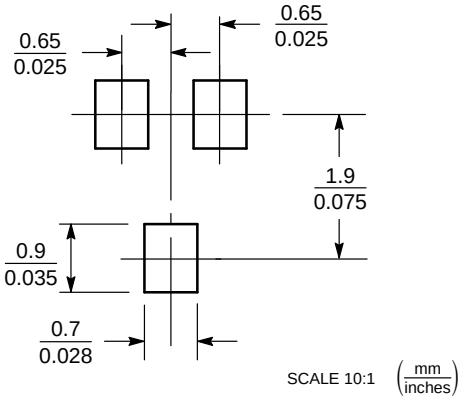


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.70 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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