

# MC100LVEL38

## 3.3 V ECL ÷2, ÷4/6 Clock Generation Chip

### Description

The MC100LVEL38 is a low skew ÷2, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended input signal.

The common enable ( $\overline{EN}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Phase\_Out output will go HIGH for one clock cycle whenever the ÷2 and the ÷4/6 outputs are both transitioning from a LOW to a HIGH. This output allows for clock synchronization within the system.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL38s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL38, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2 and the ÷4/6 outputs of a single device.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

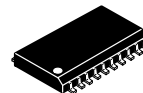
### Features

- 50 ps Maximum Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: > 2 kV Human Body Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  
 $V_{CC} = 3.0 \text{ V to } 3.8 \text{ V with } V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:  
 $V_{CC} = 0 \text{ V with } V_{EE} = -3.0 \text{ V to } -3.8 \text{ V}$
- Internal Input 75 k $\Omega$  Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test



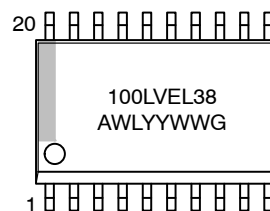
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SOIC-20 WB  
DW SUFFIX  
CASE 751D

### MARKING DIAGRAM\*



- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

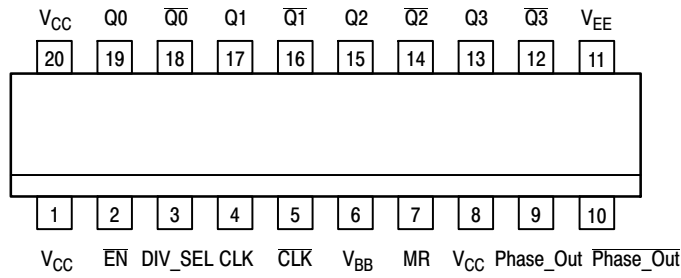
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

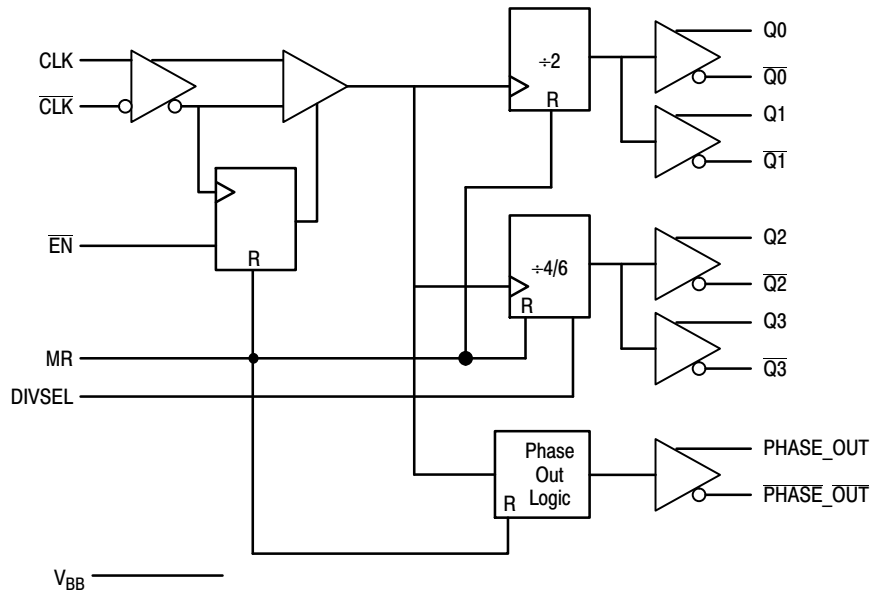
- Moisture Sensitivity: Level 3 (Pb-Free)  
For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 388 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

# MC100LEVEL38



**Figure 1. Pinout: 20-Lead SOIC (Top View)**

Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.



**Figure 2. Logic Diagram**

**Table 1. PIN DESCRIPTION**

Pin	Function
CLK, $\overline{\text{CLK}}$	ECL Diff Clock Inputs
$Q_0, Q_1, \overline{Q_0}, \overline{Q_1}$	ECL Diff $\div 2$ Outputs
$Q_2, Q_3, \overline{Q_2}, \overline{Q_3}$	ECL Diff $\div 4/6$ Outputs
EN	ECL Sync Enable Input
MR	ECL Master Reset Input
DIVSEL	ECL Frequency Select Input
Phase_Out, $\overline{\text{Phase\_Out}}$	ECL Phase Sync Diff. Signal Output
$V_{BB}$	Reference Voltage Output
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply

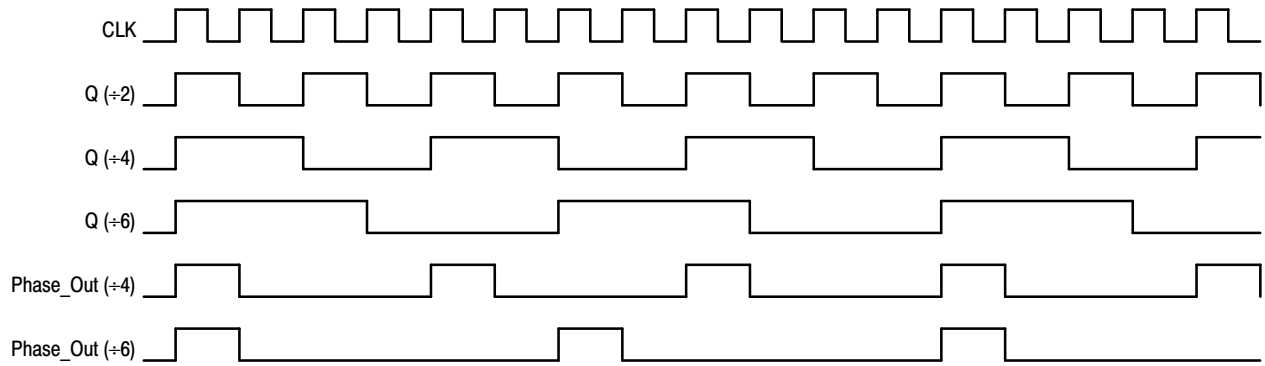
**Table 2. FUNCTION TABLE**

CLK	EN	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold $Q_{0-3}$
X	X	H	Reset $Q_{0-3}$

Z = Low-to-High Transition  
 ZZ = High-to-Low Transition  
 X = Don't Care

DVSEL	$Q_2, Q_3$ OUTPUTS
L	Divide by 4
H	Divide by 6

# MC100LEVEL38



**Figure 3. Timing Diagrams**

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8 to 0	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-8 to 0	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 -6 to 0	V
$I_{out}$	Output Current	Continuous Surge		50 100	mA
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
$T_A$	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-20 WB	90 60	$^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-20 WB	30 to 35	$^{\circ}\text{C}/\text{W}$
$T_{sol}$	Wave Solder (Pb-Free)	< 2 to 3 sec @ 260 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# MC100LEVEL38

**Table 4. LVPECL DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		50	60		50	60		54	65	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
$V_{OL}$	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
$V_{BB}$	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	1.65		2.75	1.65		2.75	1.65		2.75	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PP\text{ Min}}$  and  $1.0\text{ V}$ .

**Table 5. LVNECL DC CHARACTERISTICS** ( $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		50	60		50	60		54	65	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	-1.65		-0.55	-1.65		-0.55	-1.65		-0.55	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PP\text{ Min}}$  and  $1.0\text{ V}$ .

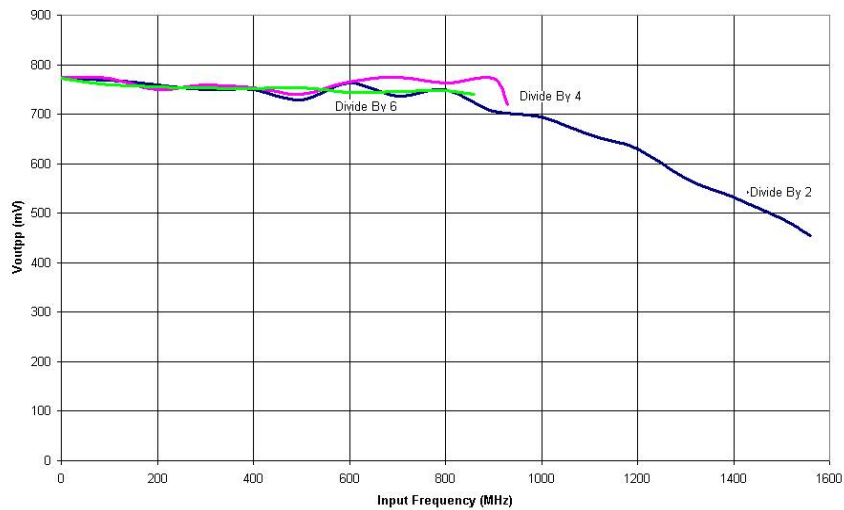
# MC100LVEL38

**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f <sub>max</sub>	Maximum Toggle Frequency (Figure 4) Divide by 2 Divide by 4, Divide by 6	1.0 0.8	1.2 0.82		1.0 0.8	1.2 0.82		1.0 0.8	1.2 0.82		GHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output CLK to Q (Differential) CLK to Q (Single-Ended) CLK to Phase_Out (Differential) CLK to Phase_Out (Single-Ended) MR to Q	810 710 800 750 510		1010 1010 1000 1050 810	850 750 840 790 540		1050 1050 1040 1090 840	900 800 890 840 570		1100 1100 1090 1140 870	ps
t <sub>SKEW</sub>	Within-Device Skew (Note 2) Q <sub>0</sub> - Q <sub>3</sub> All			50 75			50 75			50 75	ps
	Part-to-Part Q <sub>0</sub> - Q <sub>3</sub> (Differential) All			200 240			200 240			200 240	ps
t <sub>S</sub>	Setup Time EN to CLK DIVSEL to CLK	150			150			150			ps
t <sub>H</sub>	Hold Time CLK to EN CLK to Div_Sel	150 200			150 200			150 200			ps
V <sub>PP</sub>	Input Swing (Note 3) CLK	250		1000	250		1000	250		1000	mV
t <sub>RR</sub>	Reset Recovery Time			100			100			100	ps
t <sub>PW</sub>	Minimum Pulse Width CLK MR	800 700			800 700			800 700			ps
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Times Q (20% - 80%)	280		550	280		550	280		550	ps

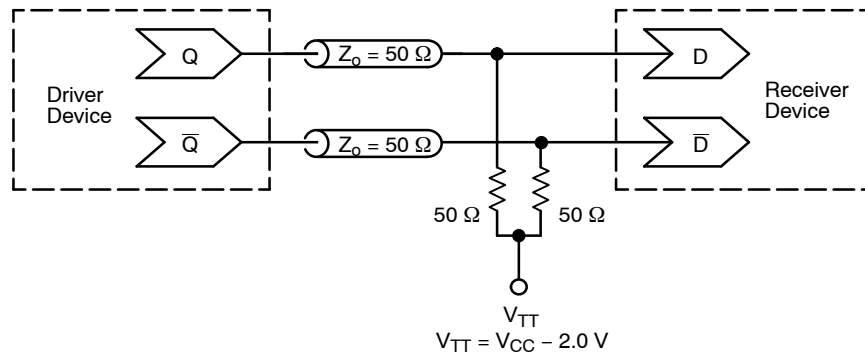
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Skew is measured between outputs under identical transitions.
3.  $V_{PP}$  (min) is minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100 mV.



**Figure 4. Fmax: Voutpp vs Input Frequency per DIV2/4/6**

## MC100LVEL38



**Figure 5. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC100LVEL38DWG	SOIC-20 WB (Pb-Free)	38 Units / Tube
MC100LVEL38DWR2G	SOIC-20 WB (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

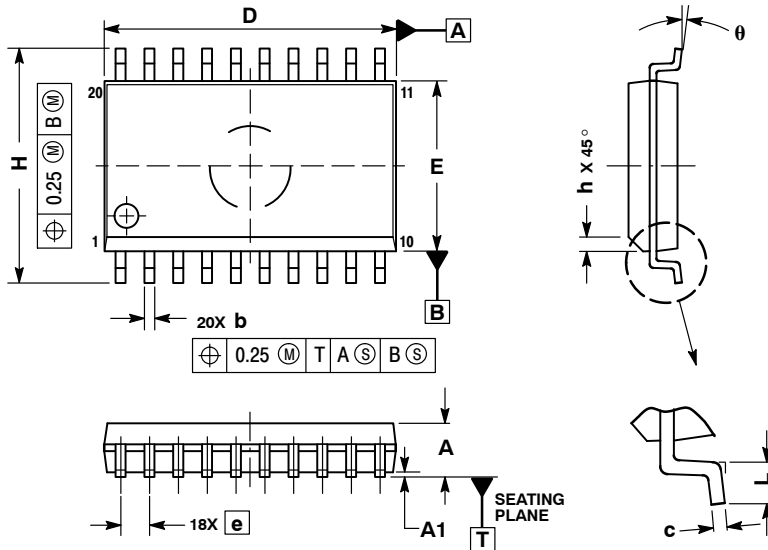
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC100LVEL38

## PACKAGE DIMENSIONS

### SOIC-20 WB CASE 751D-05 ISSUE H

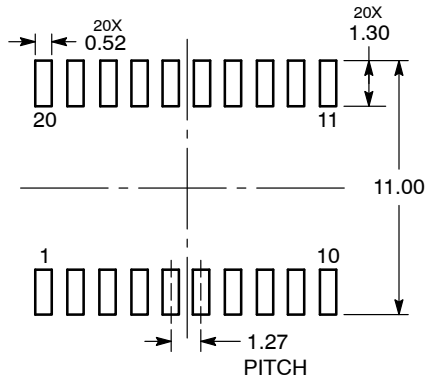


**NOTES:**

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](#).

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