

# J111, J112

## JFET Chopper Transistors

### N-Channel — Depletion

#### Features

- Pb-Free Packages are Available\*

#### MAXIMUM RATINGS

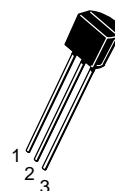
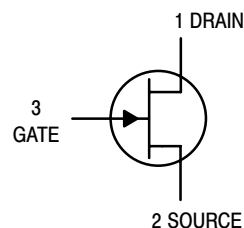
Rating	Symbol	Value	Unit
Drain–Gate Voltage	$V_{DG}$	–35	Vdc
Gate–Source Voltage	$V_{GS}$	–35	Vdc
Gate Current	$I_G$	50	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above = $25^\circ\text{C}$	$P_D$	350 2.8	mW mW/ $^\circ\text{C}$
Lead Temperature	$T_L$	300	$^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



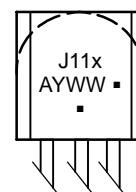
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TO-92  
CASE 29-11  
STYLE 5

#### MARKING DIAGRAM



J11x = Device Code  
x = 1 or 2

A = Assembly Location

Y = Year

WW = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# J111, J112

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Gate–Source Breakdown Voltage (I <sub>G</sub> = –1.0 $\mu$ Adc)	V <sub>(BR)GSS</sub>	35	–	Vdc
Gate Reverse Current (V <sub>GS</sub> = –15 Vdc)	I <sub>GSS</sub>	–	–1.0	nAdc
Gate Source Cutoff Voltage (V <sub>DS</sub> = 5.0 Vdc, I <sub>D</sub> = 1.0 $\mu$ Adc) J111 J112	V <sub>GS(off)</sub>	–3.0 –1.0	–10 –5.0	Vdc
Drain–Cutoff Current (V <sub>DS</sub> = 5.0 Vdc, V <sub>GS</sub> = –10 Vdc)	I <sub>D(off)</sub>	–	1.0	nAdc
<b>ON CHARACTERISTICS</b>				
Zero–Gate–Voltage Drain Current <sup>(1)</sup> (V <sub>DS</sub> = 15 Vdc) J111 J112	I <sub>DSS</sub>	20 5.0 2.0	– – –	mAdc
Static Drain–Source On Resistance (V <sub>DS</sub> = 0.1 Vdc) J111 J112	r <sub>DS(on)</sub>	– –	30 50	$\Omega$
Drain Gate and Source Gate On–Capacitance (V <sub>DS</sub> = V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>dg(on)</sub> + C <sub>sg(on)</sub>	–	28	pF
Drain Gate Off–Capacitance (V <sub>GS</sub> = –10 Vdc, f = 1.0 MHz)	C <sub>dg(off)</sub>	–	5.0	pF
Source Gate Off–Capacitance (V <sub>GS</sub> = –10 Vdc, f = 1.0 MHz)	C <sub>sg(off)</sub>	–	5.0	pF

1. Pulse Width = 300  $\mu$ s, Duty Cycle = 3.0%.

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
J111RL1	TO–92	2000 Units / Tape & Reel
J111RL1G	TO–92 (Pb–Free)	
J111RLRA	TO–92	2000 Units / Tape & Reel
J111RLRAG	TO–92 (Pb–Free)	
J111RLRP	TO–92	2000 Units / Tape & Reel
J111RLRPG	TO–92 (Pb–Free)	
J112	TO–92	1000 Units / Bulk
J112G	TO–92 (Pb–Free)	
J112RL1	TO–92	2000 Units / Tape & Reel
J112RL1G	TO–92 (Pb–Free)	
J112RLRA	TO–92	2000 Units / Tape & Reel
J112RLRAG	TO–92 (Pb–Free)	

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## TYPICAL SWITCHING CHARACTERISTICS

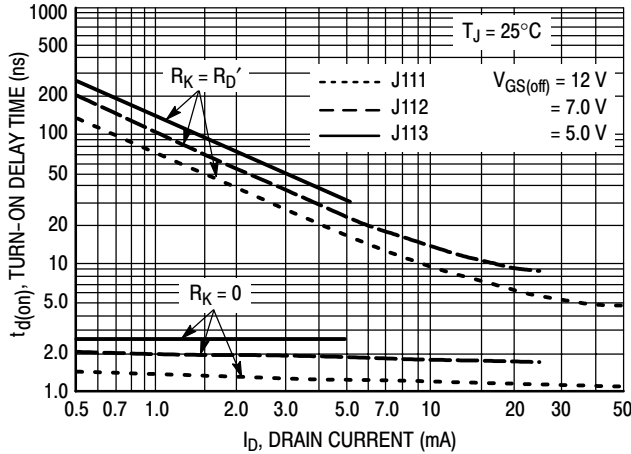


Figure 1. Turn-On Delay Time

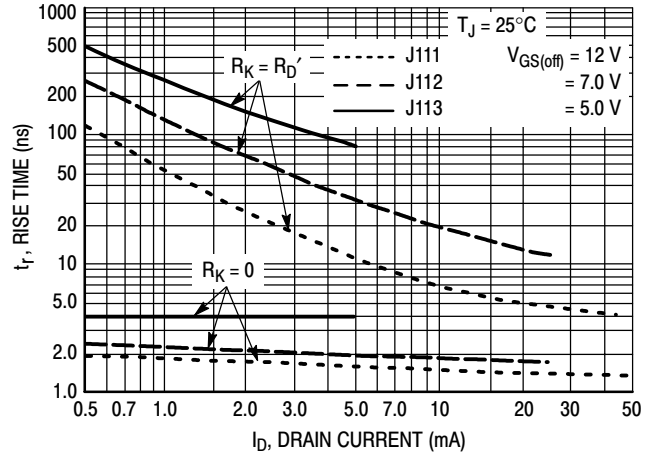


Figure 2. Rise Time

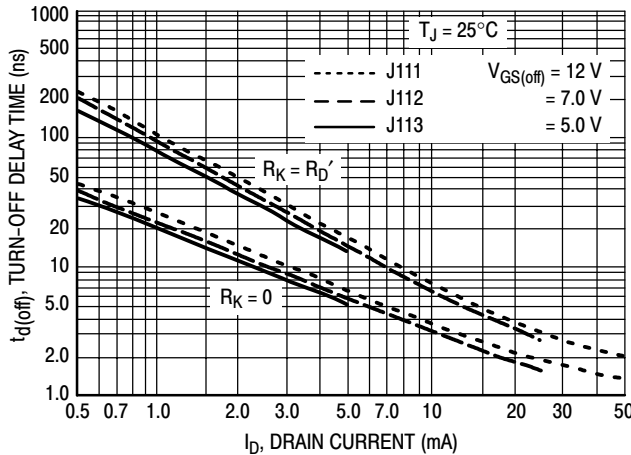


Figure 3. Turn-Off Delay Time

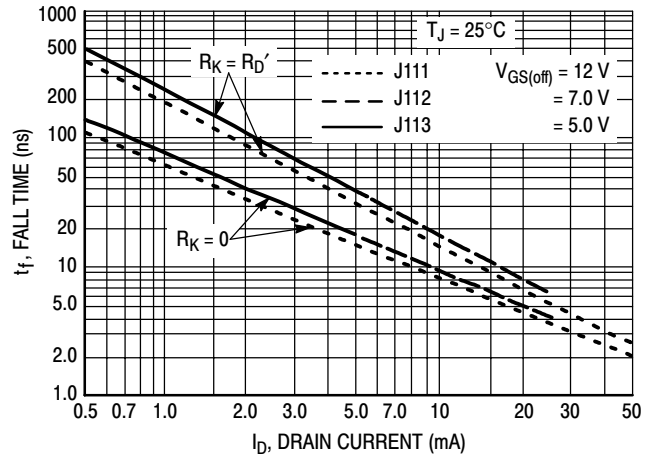


Figure 4. Fall Time

## NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ( $-V_{GG}$ ). The Drain-Source Voltage ( $V_{DS}$ ) is slightly lower than Drain Supply Voltage ( $V_{DD}$ ) due to the voltage divider. Thus Reverse Transfer Capacitance ( $C_{rss}$ ) or Gate-Drain Capacitance ( $C_{gd}$ ) is charged to  $V_{GG} + V_{DS}$ .

During the turn-on interval, Gate-Source Capacitance ( $C_{gs}$ ) discharges through the series combination of  $R_{GEN}$  and  $R_K$ .  $C_{gd}$  must discharge to  $V_{DS(on)}$  through  $R_G$  and  $R_K$  in series with the parallel combination of effective load impedance ( $R'_D$ ) and Drain-Source Resistance ( $r_{ds}$ ). During the turn-off, this charge flow is reversed.

Predicting turn-on time is somewhat difficult as the channel resistance  $r_{ds}$  is a function of the gate-source voltage. While  $C_{gs}$  discharges,  $V_{GS}$  approaches zero and  $r_{ds}$  decreases. Since  $C_{gd}$  discharges through  $r_{ds}$ , turn-on time is non-linear. During turn-off, the situation is reversed with  $r_{ds}$  increasing as  $C_{gd}$  charges.

The above switching curves show two impedance conditions; 1)  $R_K$  is equal to  $R_D$ , which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2)  $R_K = 0$  (low impedance) the driving source impedance is that of the generator.

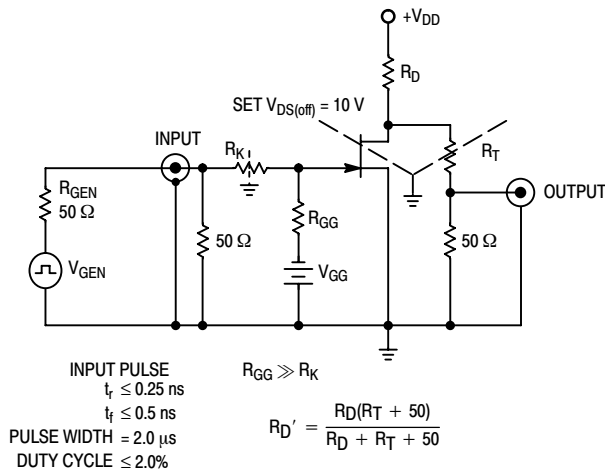


Figure 5. Switching Time Test Circuit

# J111, J112

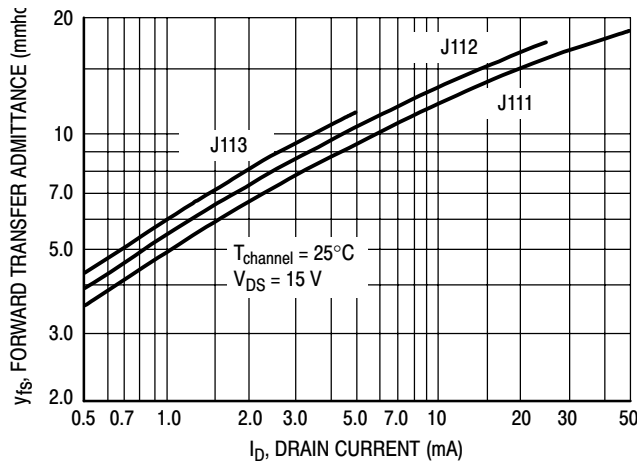


Figure 6. Typical Forward Transfer Admittance

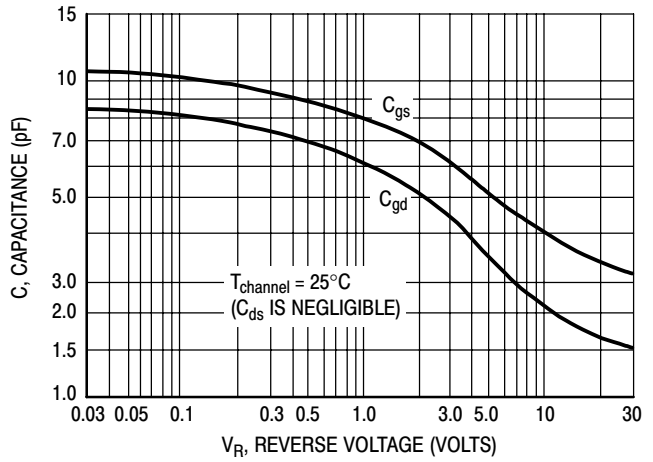


Figure 7. Typical Capacitance

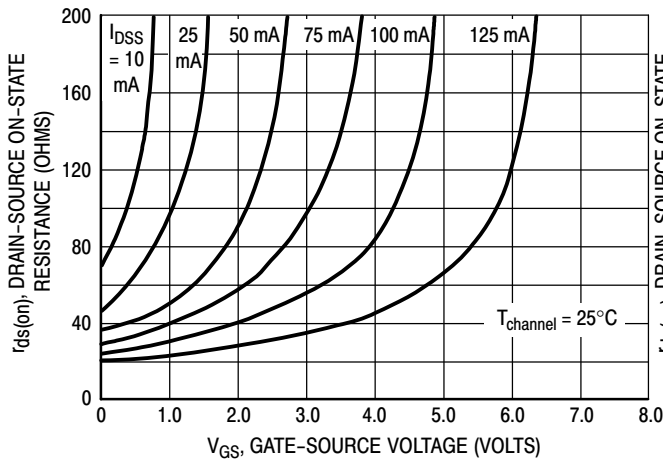


Figure 8. Effect of Gate-Source Voltage On Drain-Source Resistance

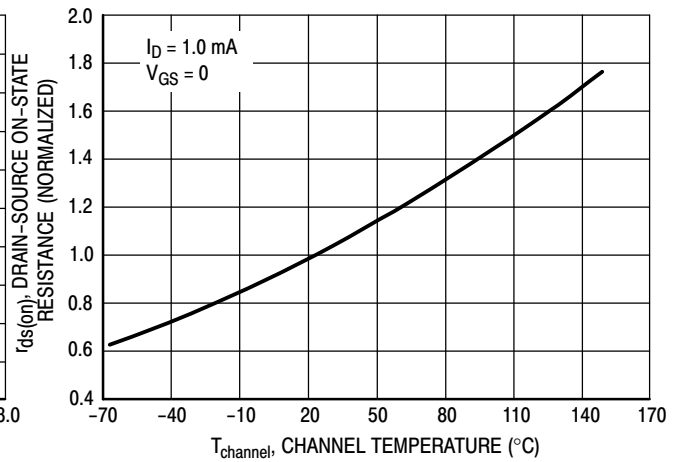


Figure 9. Effect of Temperature On Drain-Source On-State Resistance

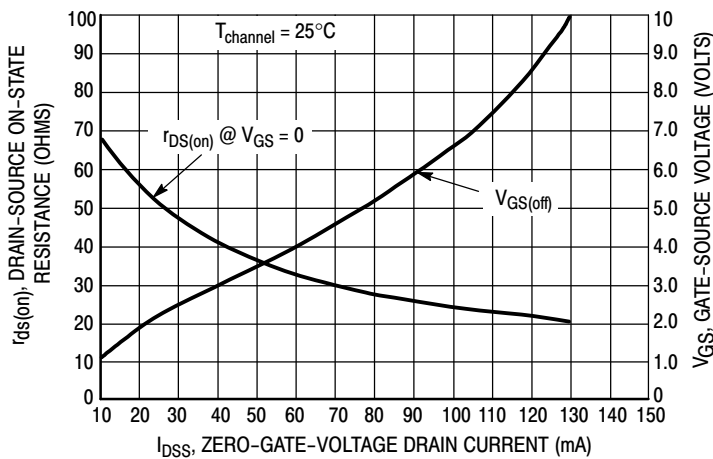


Figure 10. Effect of  $I_{DSS}$  On Drain-Source Resistance and Gate-Source Voltage

## NOTE 2

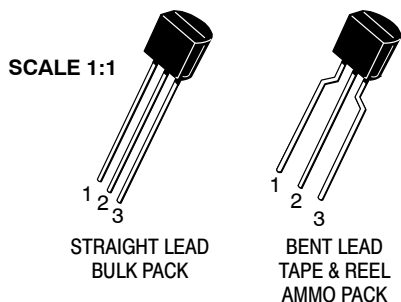
The Zero-Gate-Voltage Drain Current ( $I_{DSS}$ ), is the principle determinant of other J-FET characteristics. Figure 10 shows the relationship of Gate-Source Off Voltage ( $V_{GS(off)}$ ) and Drain-Source On Resistance ( $r_{ds(on)}$ ) to  $I_{DSS}$ . Most of the devices will be within  $\pm 10\%$  of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

For example:

Unknown

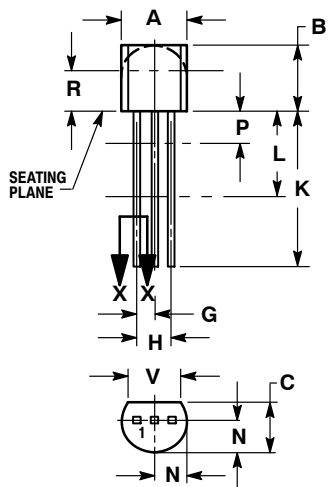
$r_{ds(on)}$  and  $V_{GS}$  range for an J112

The electrical characteristics table indicates that an J112 has an  $I_{DSS}$  range of 25 to 75 mA. Figure 10, shows  $r_{ds(on)} = 52 \Omega$  for  $I_{DSS} = 25$  mA and  $30 \Omega$  for  $I_{DSS} = 75$  mA. The corresponding  $V_{GS}$  values are 2.2 V and 4.8 V.

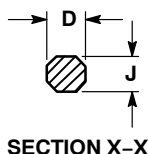


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DATE 09 MAR 2007



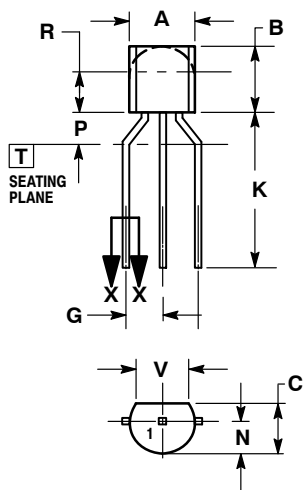
STRAIGHT LEAD  
BULK PACK



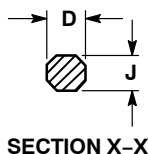
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD  
TAPE & REEL  
AMMO PACK



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
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3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

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**CASE 29-11**  
**ISSUE AM**

DATE 09 MAR 2007

STYLE 1: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 2: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 3: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 5: PIN 1. DRAIN 2. SOURCE 3. GATE
STYLE 6: PIN 1. GATE 2. SOURCE & SUBSTRATE 3. DRAIN	STYLE 7: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 8: PIN 1. DRAIN 2. GATE 3. SOURCE & SUBSTRATE	STYLE 9: PIN 1. BASE 1 2. EMITTER 3. BASE 2	STYLE 10: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 11: PIN 1. ANODE 2. CATHODE & ANODE 3. CATHODE	STYLE 12: PIN 1. MAIN TERMINAL 1 2. GATE 3. MAIN TERMINAL 2	STYLE 13: PIN 1. ANODE 1 2. GATE 3. CATHODE 2	STYLE 14: PIN 1. EMITTER 2. COLLECTOR 3. BASE	STYLE 15: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2
STYLE 16: PIN 1. ANODE 2. GATE 3. CATHODE	STYLE 17: PIN 1. COLLECTOR 2. BASE 3. EMITTER	STYLE 18: PIN 1. ANODE 2. CATHODE 3. NOT CONNECTED	STYLE 19: PIN 1. GATE 2. ANODE 3. CATHODE	STYLE 20: PIN 1. NOT CONNECTED 2. CATHODE 3. ANODE
STYLE 21: PIN 1. COLLECTOR 2. EMITTER 3. BASE	STYLE 22: PIN 1. SOURCE 2. GATE 3. DRAIN	STYLE 23: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 24: PIN 1. EMITTER 2. COLLECTOR/ANODE 3. CATHODE	STYLE 25: PIN 1. MT 1 2. GATE 3. MT 2
STYLE 26: PIN 1. V <sub>CC</sub> 2. GROUND 2 3. OUTPUT	STYLE 27: PIN 1. MT 2. SUBSTRATE 3. MT	STYLE 28: PIN 1. CATHODE 2. ANODE 3. GATE	STYLE 29: PIN 1. NOT CONNECTED 2. ANODE 3. CATHODE	STYLE 30: PIN 1. DRAIN 2. GATE 3. SOURCE
STYLE 31: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 32: PIN 1. BASE 2. COLLECTOR 3. EMITTER	STYLE 33: PIN 1. RETURN 2. INPUT 3. OUTPUT	STYLE 34: PIN 1. INPUT 2. GROUND 3. LOGIC	STYLE 35: PIN 1. GATE 2. COLLECTOR 3. EMITTER

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