

## FDH5500\_F085

### N-Channel UltraFET Power MOSFET

55V, 75A, 7mΩ

#### Features

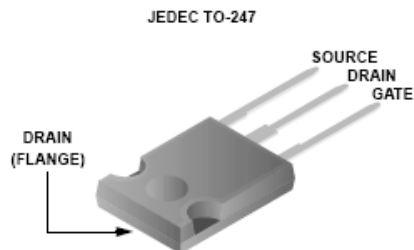
- Typ  $r_{DS(on)}$  = 5.2mΩ at  $V_{GS}$  = 10V,  $I_D$  = 75A
- Typ  $Q_{g(10)}$  = 118nC at  $V_{GS}$  = 10V
- Simulation Models
  - Temperature Compensated PSPICE and SABER™ Models
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"
- Qualified to AEC Q101
- RoHS Compliant

#### Applications

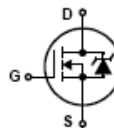
- DC Linear Mode Control
- Solenoid and Motor Control
- Switching Regulators
- Automotive Systems



#### Package



#### Symbol



**MOSFET Maximum Ratings**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage (Note 1)	55	V
$V_{DGR}$	Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1)	55	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current Continuous ( $T_C < 135^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )	75	A
	Pulsed	See Figure 4	
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	864	mJ
$P_D$	Power Dissipation	375	W
	Dereate above $25^\circ\text{C}$	2.5	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to + 175	$^\circ\text{C}$
$T_L$	Max. Lead Temp. for Soldering (at 1.6mm from case for 10sec)	300	
$T_{pkg}$	Max. Package Temp. for Soldering (Package Body for 10sec)	260	

**Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance Junction to Case	0.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-247, 1in <sup>2</sup> copper pad area	30	$^\circ\text{C/W}$

**Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDH5500	FDH5500_F085	TO-247	Tube	N/A	30 units

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	55	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 50\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 45\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	250	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2	2.9	4	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 75\text{A}$ , $V_{GS} = 10\text{V}$	-	5.2	7	m $\Omega$

**Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz		-	3565	-	pF
C <sub>oss</sub>	Output Capacitance			-	1310	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			-	395	-	pF
Q <sub>g(TOT)</sub>	Total Gate Charge at 20V	V <sub>GS</sub> = 0 to 20V	V <sub>DD</sub> = 30V I <sub>D</sub> = 75A R <sub>L</sub> = 0.4Ω I <sub>g</sub> = 1.0mA	-	206	268	nC
Q <sub>g(10)</sub>	Total Gate Charge at 10V	V <sub>GS</sub> = 0 to 10V		-	118	153	nC
Q <sub>g(TH)</sub>	Threshold Gate Charge	V <sub>GS</sub> = 0 to 2V		-	6.2	8.1	nC
Q <sub>gs</sub>	Gate to Source Gate Charge			-	17.8	-	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge			-	51	-	nC

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Switching Characteristics**

$t_{on}$	Turn-On Time	$V_{DD} = 30\text{V}, I_D = 75\text{A},$ $R_L = 0.4\Omega, V_{GS} = 10\text{V},$ $R_{GS} = 2.5\Omega$	-	-	185	ns
$t_{d(on)}$	Turn-On Delay Time		-	13.7	-	ns
$t_r$	Rise Time		-	102	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	34	-	ns
$t_f$	Fall Time		-	22	-	ns
$t_{off}$	Turn-Off Time		-	-	91	ns

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 75\text{A}$	-	1	1.25	V
$t_{rr}$	Reverse Recovery Time	$I_F = 75\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	60	78	ns
$Q_{rr}$	Reverse Recovery Charge		-	77	100	nC

**Notes:**1: Starting  $T_J = 25^\circ\text{C}$  to  $175^\circ\text{C}$ .2: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.48\text{mH}$ ,  $I_{AS} = 60\text{A}$ 

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

## Typical Characteristics

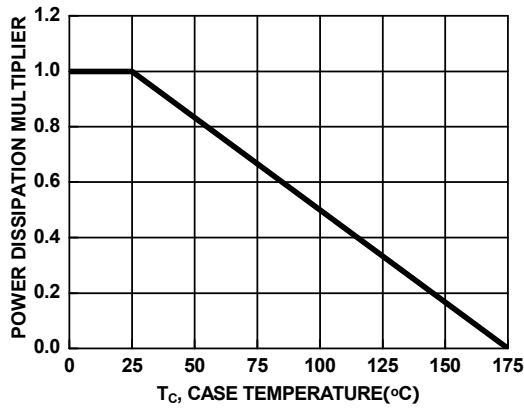


Figure 1. Normalized Power Dissipation vs Case Temperature

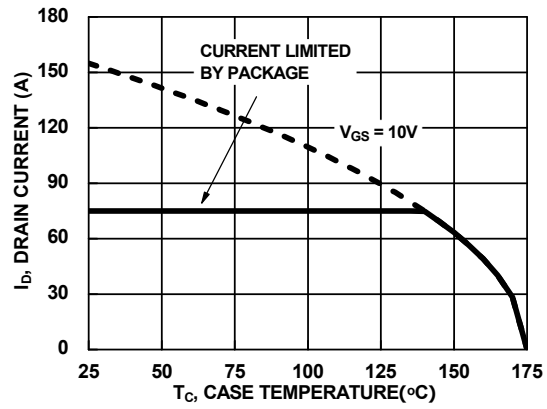


Figure 2. Maximum Continuous Drain Current vs Case Temperature

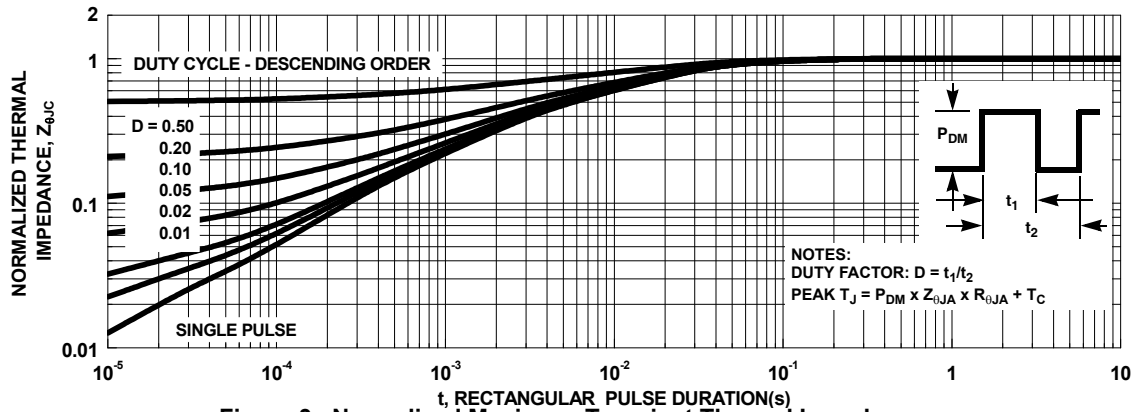


Figure 3. Normalized Maximum Transient Thermal Impedance

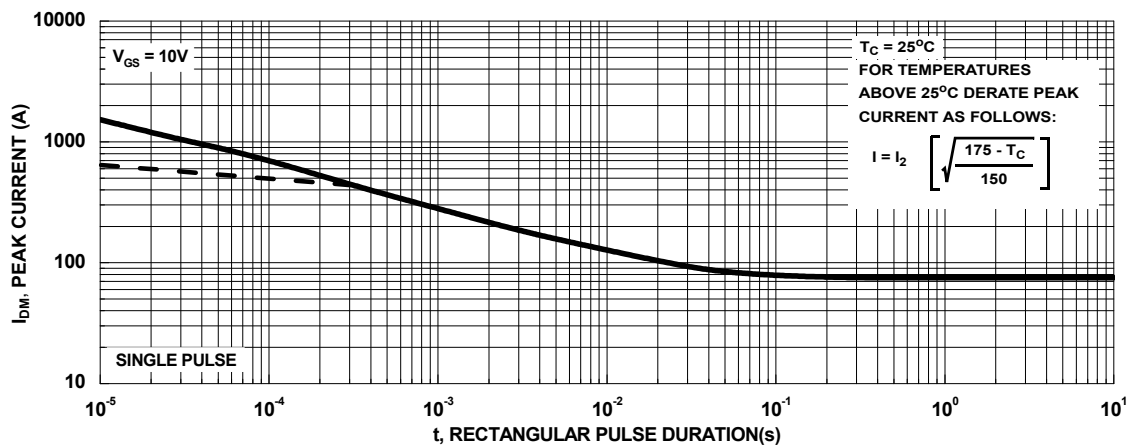


Figure 4. Peak Current Capability

## Typical Characteristics

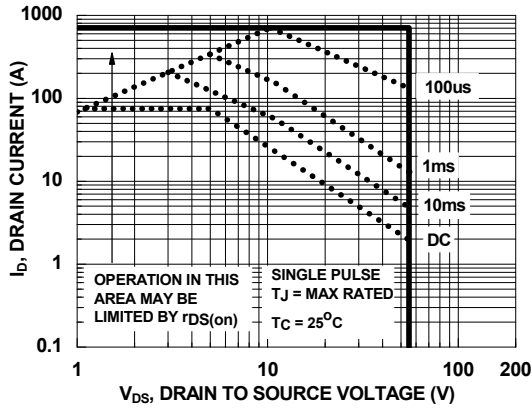
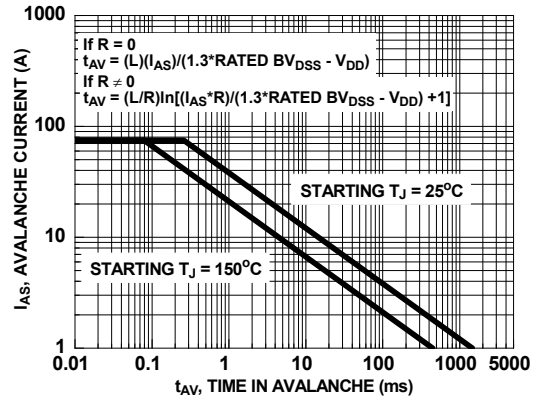


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

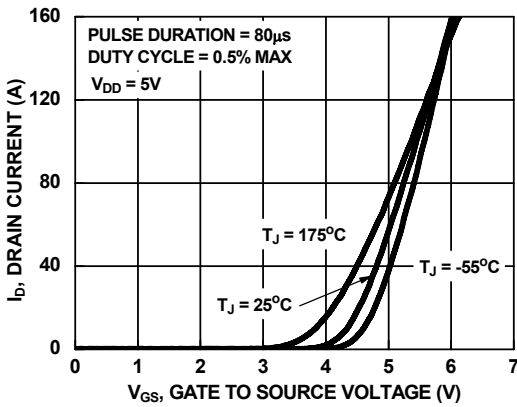


Figure 7. Transfer Characteristics

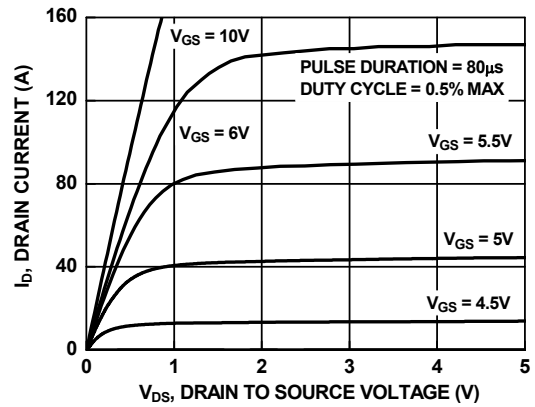


Figure 8. Saturation Characteristics

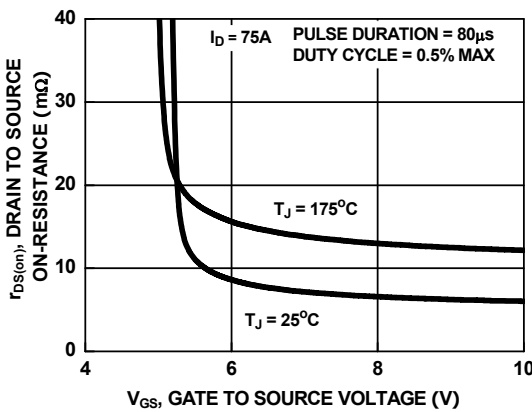


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

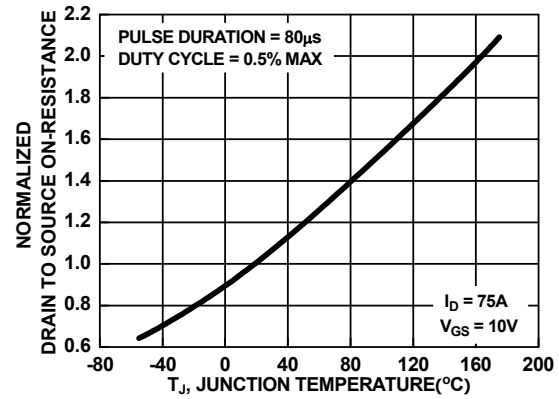


Figure 10. Normalized Drain to Source On-Resistance vs Junction Temperature

## Typical Characteristics

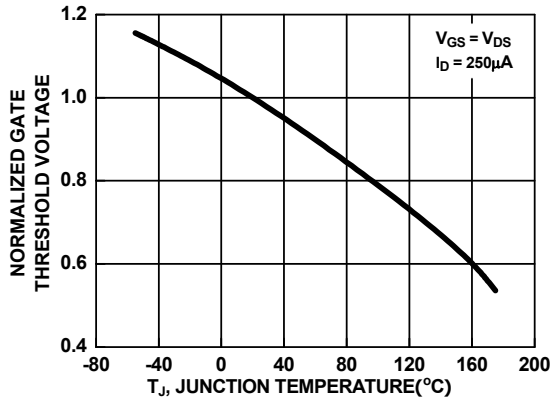


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

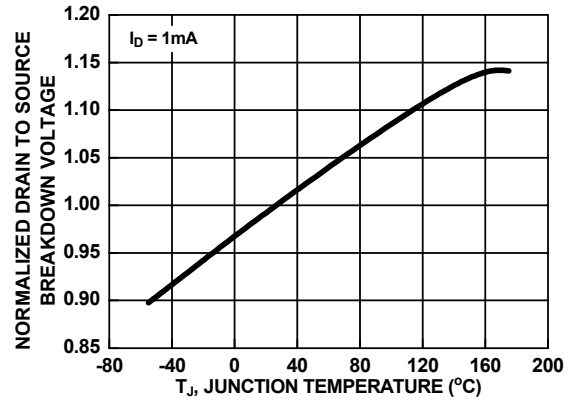


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

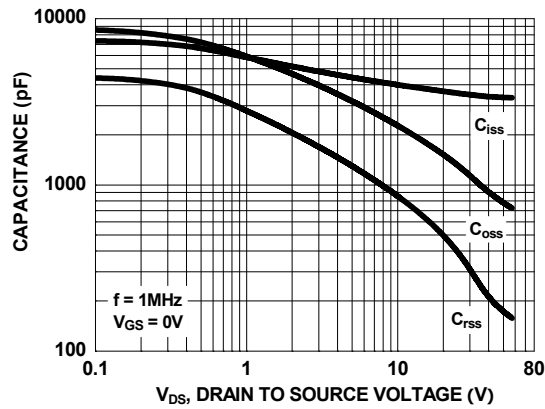


Figure 13. Capacitance vs Drain to Source Voltage

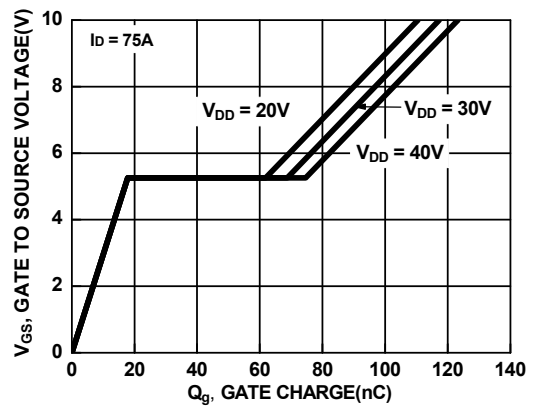





Figure 14. Gate Charge vs Gate to Source Voltage

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