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September 2010



FSL127H — Green Mode Fairchild Power Switch (FPS™)

## FSL127H

### Green Mode Fairchild Power Switch (FPS™)

#### Features

- Built-in 5ms Soft-Start Function
- Internal Avalanche-Rugged 700V SenseFET
- Low Audio Noise
- High-Voltage Startup
- Fixed PWM Frequency at 100KHz
- Linearly Decreasing PWM Frequency to 18KHz
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- Internal Open-Loop Protection (OLP)
- $V_{DD}$  Under-Voltage Lockout (UVLO)
- $V_{DD}$  Over-Voltage Protection (OVP)
- Constant Power Limit (Full AC Input Range)
- Internal OTP Sensor with Hysteresis

#### Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- SMPS for VCR, SVR, STB, DVD & VCD Player, Printer, Facsimile, & Scanner
- Adapter for Camcorder

#### Description

The highly integrated FSL127H consists of a current mode Pulse Width Modulator (PWM) and an avalanche-rugged 700V SenseFET. It is specifically designed for high-performance offline Switch Mode Power Supplies (SMPS) with minimal external components.

The integrated PWM controller features include a proprietary green-mode function that provides off-time modulation to linearly decrease the switching frequency at light-load conditions to minimize standby power consumption. To avoid acoustic noise problems, the minimum PWM frequency is set above 18KHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, the PWM controller is manufactured using the BiCMOS process, which allows an operating current of only 3.5mA.

The FSL127H built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary external line compensation ensures constant output power limit over a wide AC input voltage range, from 90V<sub>AC</sub> to 264V<sub>AC</sub>.

The FSL127H provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety when an open-loop or output short-circuit failure occurs. PWM output is disabled until  $V_{DD}$  drops below the UVLO lower limit, when the controller starts up again. As long as  $V_{DD}$  exceeds ~28V, the internal OVP circuit is triggered.

Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSL127H reduces total component count, design size, and weight while increasing efficiency, productivity, and system reliability. These devices provide a basic platform well suited for design of cost-effective flyback converters.

#### Ordering Information

Part Number	SenseFET	Operating Temperature Range	Package	Packing Method
FSL127HNY	2.0A 700V	-40°C to +105°C	8-Pin Dual In-Line Package (MDIP), JEDEC MS-001, .300" Wide	Tube

## Application Diagram

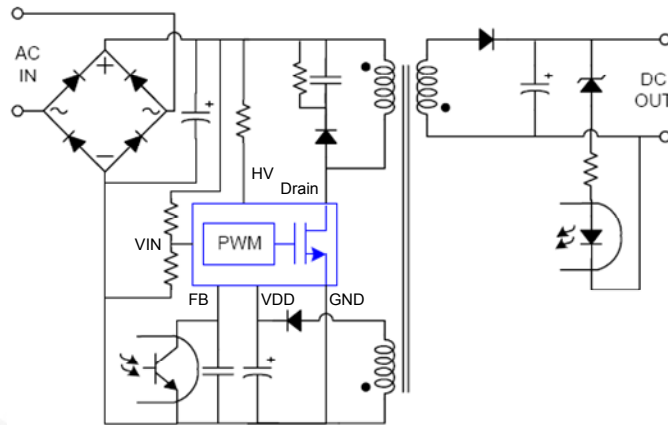


Figure 1. Typical Flyback Application

## Output Power Table<sup>(1)</sup>

Product	230V <sub>AC</sub> ± 15% <sup>(2)</sup>		85-265V <sub>AC</sub>	
	Adapter <sup>(3)</sup>	Open Frame <sup>(4)</sup>	Adapter <sup>(3)</sup>	Open Frame <sup>(4)</sup>
FSL127H	14W	20W	11W	16W

### Notes:

1. The maximum output power can be limited by junction temperature.
2. 230 V<sub>AC</sub> or 100/115 V<sub>AC</sub> with doublers.
3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink, at T<sub>A</sub>=50°C ambient.
4. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sink, at T<sub>A</sub>=50°C ambient.

## Internal Block Diagram

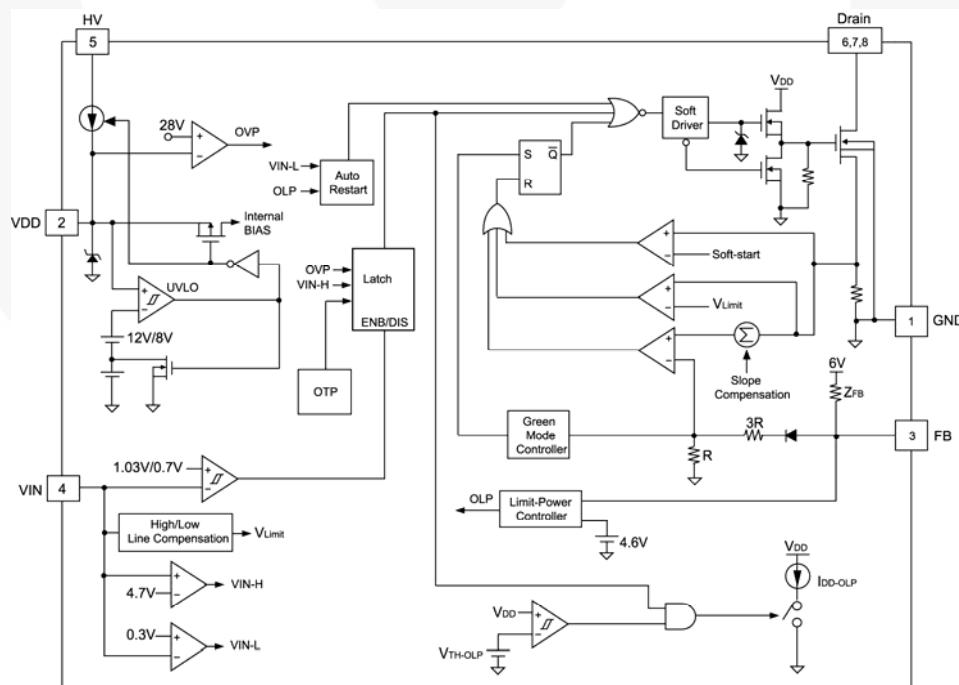
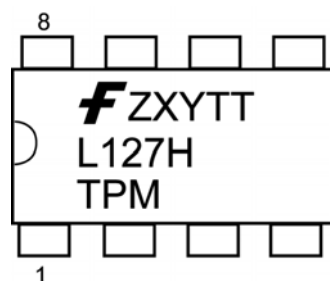


Figure 2. Internal Block Diagram

## Pin Configuration



F – Fairchild Logo  
 Z – Plant Code  
 X – 1-Digit Year Code  
 Y – 1-Digit Week Code  
 TT – 2-Digit Die Run Code  
 T – Package Type (N: DIP)  
 P – Y: Green Package  
 M – Manufacture Flow Code

Figure 3. Pin Configuration

## Pin Definitions

Pin #	Name	Description
1	GND	<b>Ground.</b> SenseFET source terminal on primary side and internal control ground.
2	V <sub>DD</sub>	<b>Power Supply.</b> The internal protection circuit disables PWM output as long as V <sub>DD</sub> exceeds the OVP trigger point.
3	FB	<b>Feedback.</b> The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the current-sense signal on the SENSE pin.
4	V <sub>IN</sub>	<b>Line-Voltage Detection.</b> The line-voltage detection is used for constant output power limit. It is suggested to add a low pass filter to filter out line ripple on bulk capacitor.
5	HV	<b>Startup.</b> For startup, this pin is pulled high to the line input or bulk capacitor via resistors.
6	Drain	<b>SenseFET Drain.</b> High-voltage power SenseFET drain connection.
7	Drain	<b>SenseFET Drain.</b> High-voltage power SenseFET drain connection.
8	Drain	<b>SenseFET Dain.</b> High-voltage power SenseFET drain connection.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V <sub>DRAIN</sub>	Drain Pin Voltage <sup>(5,6)</sup>		700	V
I <sub>DM</sub>	Drain Current Pulsed <sup>(7)</sup>		8	A
E <sub>AS</sub>	Single Pulsed Avalanche Energy <sup>(8)</sup>		140	mJ
V <sub>VDD</sub>	DC Supply Voltage		30	V
V <sub>FB</sub>	FB Pin Input Voltage	-0.3	7.0	V
V <sub>VIN</sub>	VIN Pin Input Voltage	-0.3	7.0	V
V <sub>HV</sub>	HV Pin Input Voltage		700	V
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> < 50°C)		1.5	W
θ <sub>JA</sub>	Junction-to-Air Thermal Resistance		80	°C/W
Ψ <sub>JT</sub>	Junction-to-Top Thermal Resistance <sup>(9)</sup>		35	°C/W
T <sub>J</sub>	Operating Junction Temperature		+150	°C
T <sub>STG</sub>	Storage Temperature Range	-55	+150	°C
T <sub>L</sub>	Lead Temperature (Wave Soldering or IR, 10 Seconds)		+260	°C
ESD	Electrostatic Discharge Capability, All Pins Except HV Pin <sup>(10)</sup>	Human Body Model: JESD22-A114	4.5	kV
		Charged Device Model: JESD22-C101	1.5	

### Notes:

5. All voltage values, except differential voltages, are given with respect to the network ground terminal.
6. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
7. Non-repetitive rating: pulse width is limited by maximum junction temperature.
8. L = 51mH, starting T<sub>J</sub> = 25°C.
9. Measured on the package top surface.
10. All pins including HV pin: HBM=500V, CDM=1250V.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T <sub>A</sub>	Operating Ambient Temperature	-40		+105	°C

## Electrical Characteristics

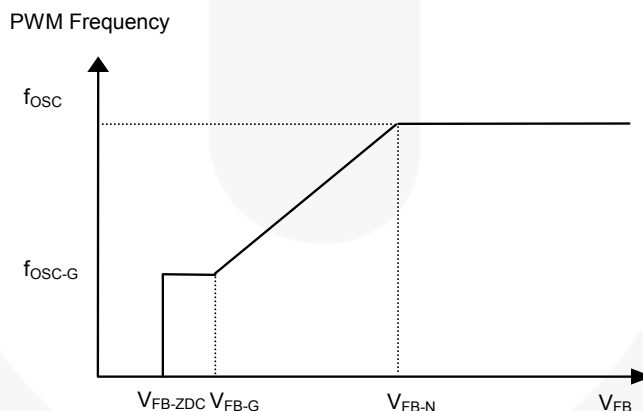
$V_{DD}=15V$  and  $T_A=25^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>SenseFET Section<sup>(11)</sup></b>						
$BV_{DSS}$	Drain- Source Breakdown Voltage	$V_{GS} = 0V$	700			V
$I_{DSS}$	Zero-Gate-Voltage Drain Current	$V_{DS} = 700V, V_{GS} = 0V$		0.5	50.0	$\mu A$
		$V_{DS} = 560V, V_{GS} = 0V, T_A = 125^{\circ}C$		1	200	
$R_{DS(ON)}$	Drain-Source On-State Resistance <sup>(12)</sup>	$V_{GS} = 10V, I_D = 0.5A$		6.0	7.2	$\Omega$
$C_{ISS}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		550	715	pF
$C_{OSS}$	Output Capacitance	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		38	50	pF
$C_{RSS}$	Reverse Transfer Capacitance	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		17	26	pF
$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 350V, I_D = 1.0A$		20	50	ns
$t_r$	Rise Time	$V_{DS} = 350V, I_D = 1.0A$		15	40	ns
$t_{d(off)}$	Turn-Off Delay Time	$V_{DS} = 350V, I_D = 1.0A$		55	120	ns
$t_f$	Fall Time	$V_{DS} = 350V, I_D = 1.0A$		25	60	ns
<b>V<sub>DD</sub> Section</b>						
$V_{OP}$	Continuously Operating Voltage				22	V
$V_{DD-ON}$	Start Threshold Voltage		11	12	13	V
$V_{DD-OFF}$	Minimum Operating Voltage		7	8	9	V
$I_{DD-ST}$	Startup Current	$V_{DD-ON} - 0.16V$			30	$\mu A$
$I_{DD-OP}$	Operating Supply Current	$V_{DD} = 15V, V_{FB} = 3V$	3.0	3.5	4.0	mA
$I_{DD-BM}$	Green-Mode Operating Supply Current	$V_{FB} = V_{ZDC}$		2		mA
$I_{DD-OLP}$	Internal Sink Current	$V_{TH-OLP}+0.1V$	30	60	90	$\mu A$
$V_{TH-OLP}$	$I_{DD-OLP}$ Off Voltage		5	6	7	V
$V_{DD-OVP}$	$V_{DD}$ Over-Voltage Protection		27	28	29	V
$t_{D-VDDOVP}$	$V_{DD}$ Over-Voltage Protection Debounce Time		75	130	200	$\mu s$
<b>HV Section</b>						
$I_{HV}$	Maximum Current Drawn from HV Pin	HV 120V <sub>DC</sub> , $V_{DD} = 0V$ with 10 $\mu F$	1.5	3.5	5.0	mA
$I_{HV-LC}$	Leakage Current After Startup	HV = 700V, $V_{DD} = V_{DD-OFF}+1V$		1	20	$\mu A$
<b>Oscillator Section</b>						
$f_{OSC}$	Frequency in Nominal Mode	Center Frequency	94	100	106	kHz
$f_{OSC-G}$	Green-Mode Frequency		14	18	22	kHz
$D_{MAX}$	Maximum Duty Cycle			85		%
$f_{DV}$	Frequency Variation vs. $V_{DD}$ Deviation	$V_{DD} = 9V$ to 22V			5	%
$f_{DT}$	Frequency Variation vs. Temperature Deviation <sup>(11)</sup>	$T_A = -40$ to $+105^{\circ}C$			5	%

Continued on the following page...

**Electrical Characteristics** (Continued) $V_{DD}=15V$  and  $T_A=25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>V<sub>IN</sub> Section</b>						
$V_{IN-ON}$	PWM Turn-on Threshold Voltage		0.98	1.03	1.08	V
$V_{IN-RL}$	Release Latch Voltage		0.60	0.70	0.80	V
$V_{IN-H}$	Pull HIGH Latch Trigger Level		4.4	4.7	5.0	V
$t_{IN-H}$	Pull HIGH Latch Debounce Time			120		$\mu s$
$V_{IN-L}$	Pull LOW Auto Recovery Trigger Level		0.2	0.3	0.4	V
<b>Feedback Input Section</b>						
$A_V$	FB Voltage to Current-Sense Attenuation			1/4.0		V/V
$Z_{FB}$	Input Impedance			9.5		k $\Omega$
$V_{FB-OPEN}$	Output High Voltage		5			V
$V_{FB-OLP}$	FB Open-Loop Trigger Level		4.4	4.6	4.8	V
$t_{D-OLP}$	Delay Time of FB Pin Open-loop Protection		50	56	59	ms
$V_{FB-N}$	Green-Mode Entry FB Voltage		2.3	2.5	2.7	V
$V_{FB-G}$	Green-Mode Ending FB Voltage			$V_{FB-N} - 0.1$		V
$V_{FB-ZDC}$	Zero Duty Cycle FB Voltage		1.9	2.1	2.3	V

**Figure 4.  $V_{FB}$  vs. PWM Frequency**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Current-Sense Section</b>						
$I_{LIM}$ at $V_{IN} = 1.2V$	Peak Current Limit	$V_{IN} = 1.2V$	0.51	0.61	0.71	A
$I_{LIM}$ at $V_{IN} = 3.6V$	Peak Current Limit	$V_{IN} = 3.6V$	0.44	0.54	0.64	A
$t_{SS}$	Period During Soft-Start Time <sup>(11)</sup>		4.5	5.0	5.5	ms
<b>Over-Temperature Protection Section (OTP)</b>						
$T_{OTP}$	Protection Junction Temperature <sup>(11,13)</sup>			142		$^\circ C$

**Notes:**

11. These parameters, although guaranteed, are not 100% tested in production.
12. Pulse test: pulse width  $\leq 300\mu s$ , duty  $\leq 2\%$ .
13. When activated, the output is disabled and the latch is turned off.

## Typical Characteristics

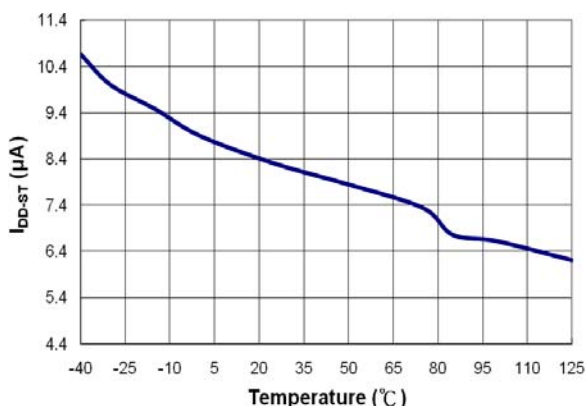


Figure 5.  $I_{DD-ST}$  vs. Temperature

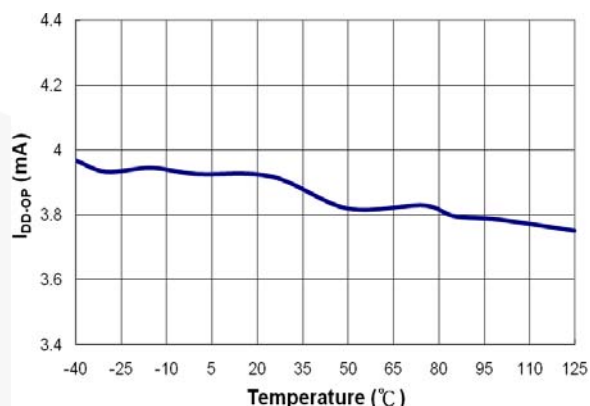


Figure 6.  $I_{DD-OP}$  vs. Temperature

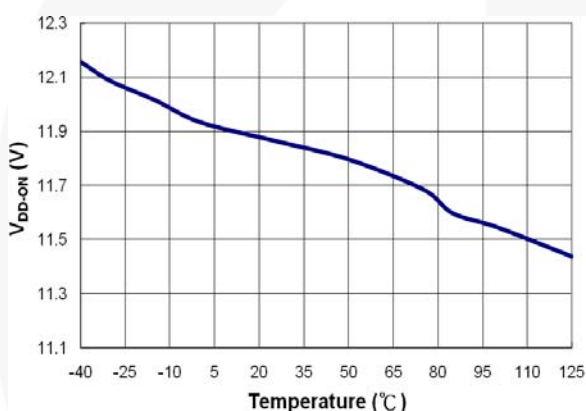


Figure 7.  $V_{DD-ON}$  vs. Temperature

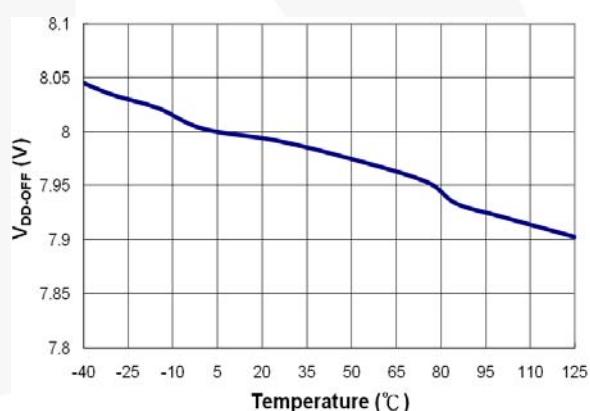


Figure 8.  $V_{DD-OFF}$  vs. Temperature

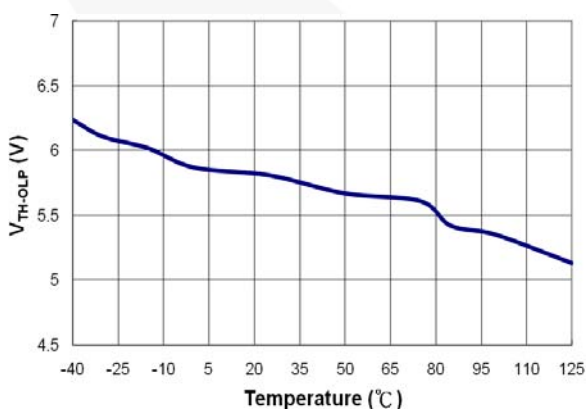


Figure 9.  $V_{TH-OLP}$  vs. Temperature

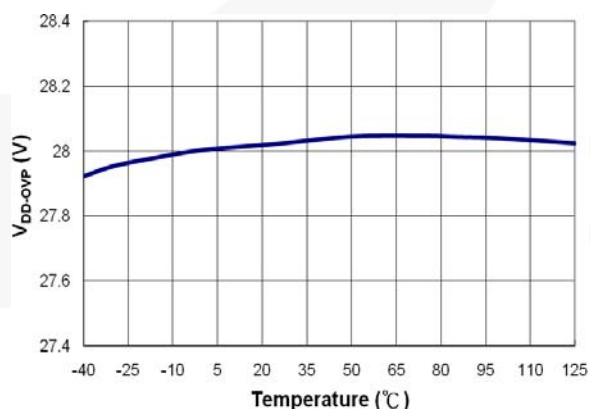


Figure 10.  $V_{DD-OVP}$  vs. Temperature



## Typical Characteristics

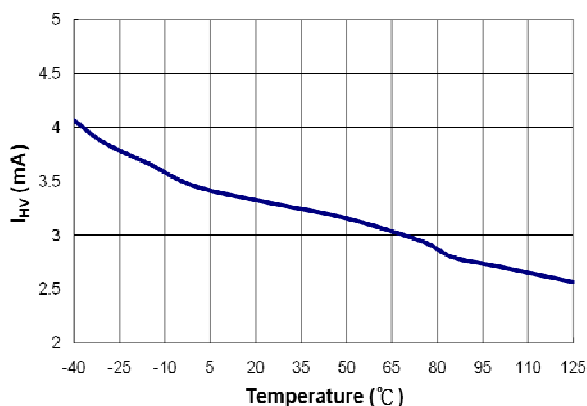


Figure 11.  $I_{HV}$  vs. Temperature

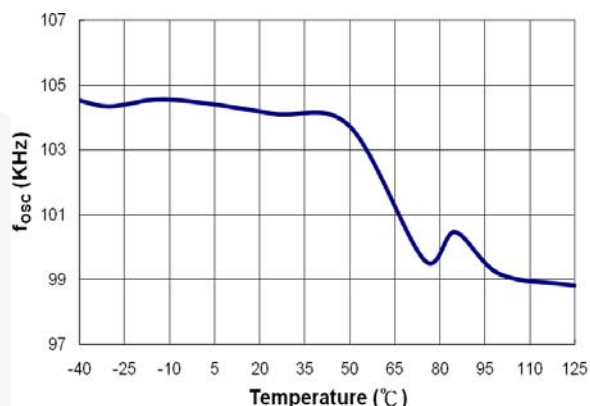


Figure 12.  $f_{osc}$  vs. Temperature

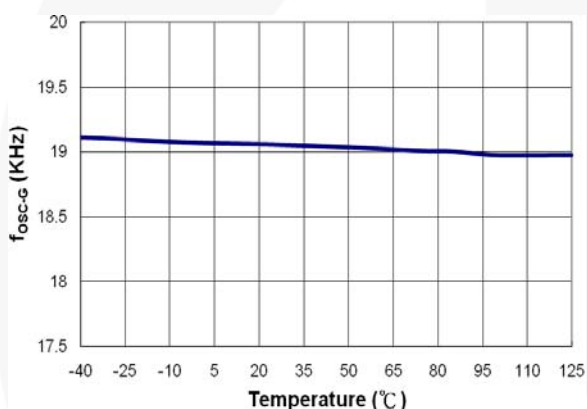


Figure 13.  $f_{osc-G}$  vs. Temperature

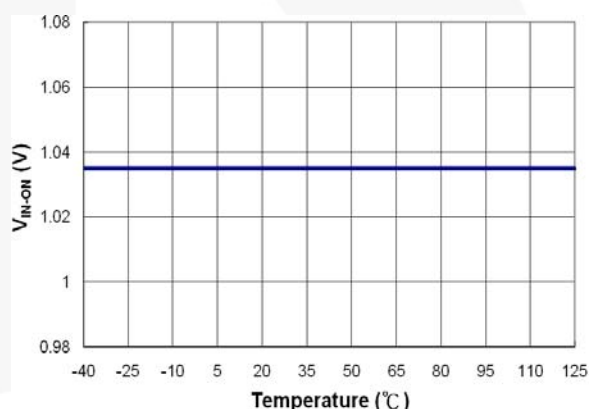


Figure 14.  $V_{IN-ON}$  vs. Temperature

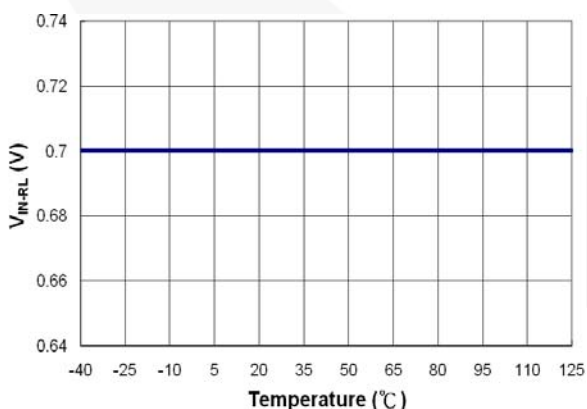


Figure 15.  $V_{IN-RL}$  vs. Temperature

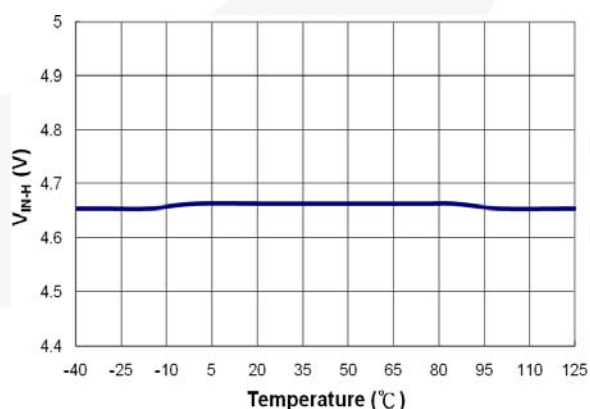


Figure 16.  $V_{IN-H}$  vs. Temperature

## Typical Characteristics

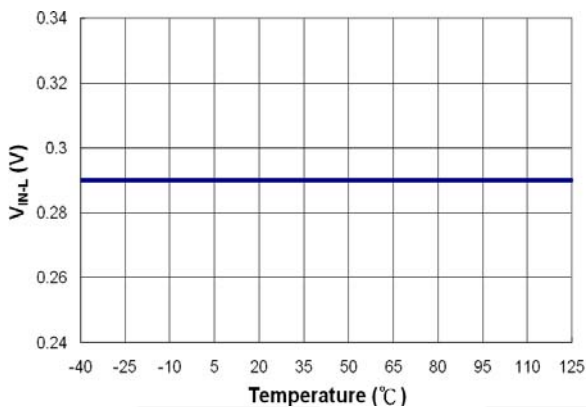


Figure 17. V<sub>IN-L</sub> vs. Temperature

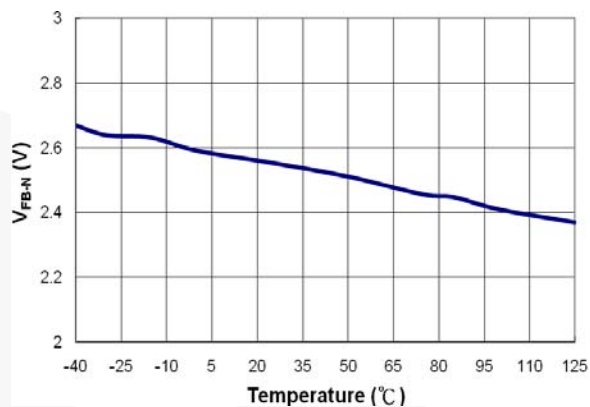


Figure 18. V<sub>FB-N</sub> vs. Temperature

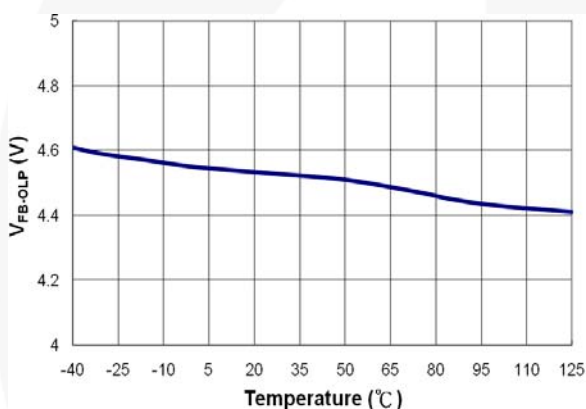


Figure 19. V<sub>FB-OLP</sub> vs. Temperature

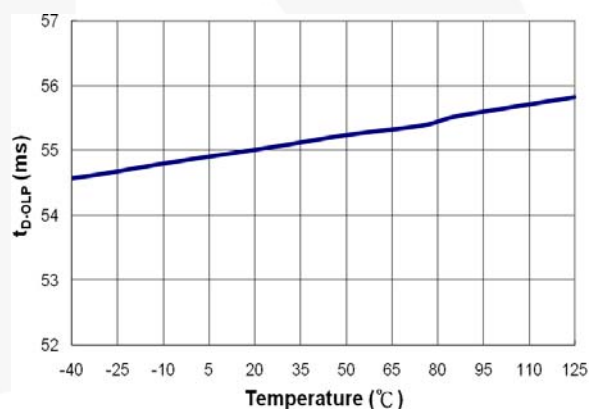


Figure 20. t<sub>D-OLP</sub> vs. Temperature

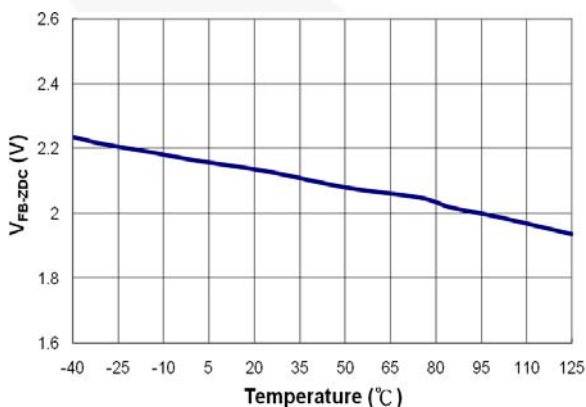


Figure 21. V<sub>FB-ZDC</sub> vs. Temperature

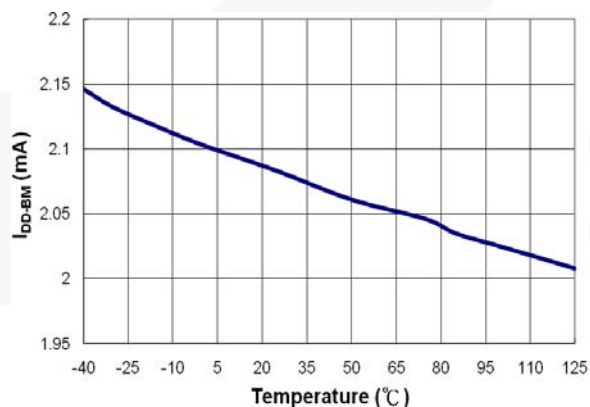


Figure 22. I<sub>DD-BM</sub> vs. Temperature

## Functional Description

### Startup Operation

For startup, the HV pin is connected to the line input or bulk capacitor through the external resistor  $R_{HV}$ , as shown in Figure 23. Typical startup current drawn from the HV pin is 3.5mA and it charges the  $V_{DD}$  capacitor through the resistor  $R_{HV}$ . The startup current turns off when the  $V_{DD}$  capacitor voltage reaches  $V_{DD-ON}$ . The  $V_{DD}$  capacitor maintains  $V_{DD}$  until the auxiliary winding of the transformer provides the operating current.

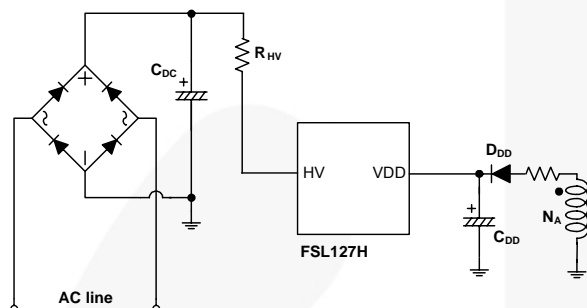


Figure 23. Startup Circuit

### Slope Compensation

FSL127H is designed for flyback power converter. The peak-current-mode control is used to optimize system performance. Slope compensation is added to stabilize the current loop. The FSL127H inserts a synchronized, positively sloped ramp at each switching cycle.

### Soft Start

The FSL127H has internal soft-start circuit that slowly increases the SenseFET current after startup. The typical soft-start time is 5ms, during which the  $V_{Limit}$  level is increased in six steps to smoothly establish the required output voltage, as shown in Figure 24. It also helps prevent transformer saturation and reduces stress on the secondary diode during startup.

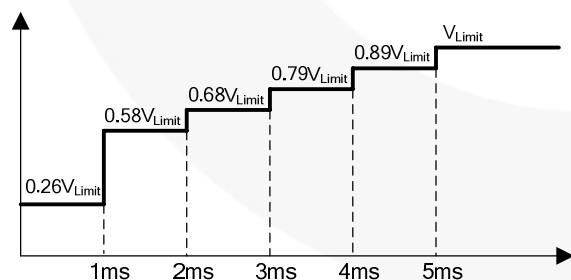


Figure 24. Soft-Start Function

### Green-Mode Operation

The FSL127H uses feedback voltage ( $V_{FB}$ ) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 25, such that the switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is 100kHz. Once  $V_{FB}$  decreases below  $V_{FB-N}$  (2.5V), the PWM frequency starts to linearly decrease from 100kHz to 18kHz to reduce the switching losses. As  $V_{FB}$  decreases below  $V_{FB-G}$  (2.4V), the switching frequency is fixed at 18kHz and FSL127H enters “deep” green mode to reduce the standby power consumption. As  $V_{FB}$  decreases below  $V_{FB-ZDC}$  (2.1V), FSL127H enters burst-mode operation. When  $V_{FB}$  drops below  $V_{FB-ZDC}$ , FSL127H stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once  $V_{FB}$  rises above  $V_{FB-ZDC}$ , switching resumes. Burst mode alternately enables and disables switching, thereby reducing switching loss to improve power saving, as shown in Figure 26.

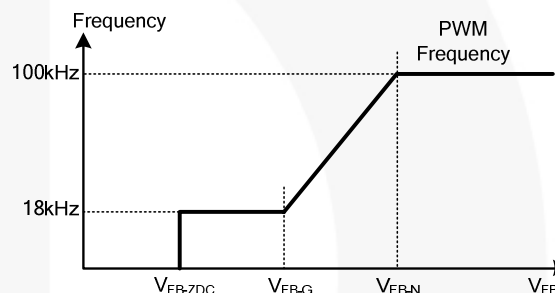


Figure 25. PWM Frequency

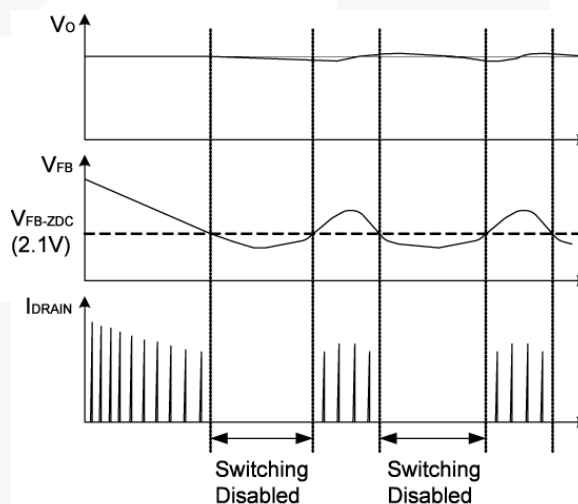


Figure 26. Burst Mode Operation

## Constant Power Control

To limit the output power of the converter constantly, high/low line compensation is included. Sensing the converter input voltage through the VIN pin, the high/low line compensation function generates a relative peak-current-limit threshold voltage for constant power control, as shown in Figure 27.

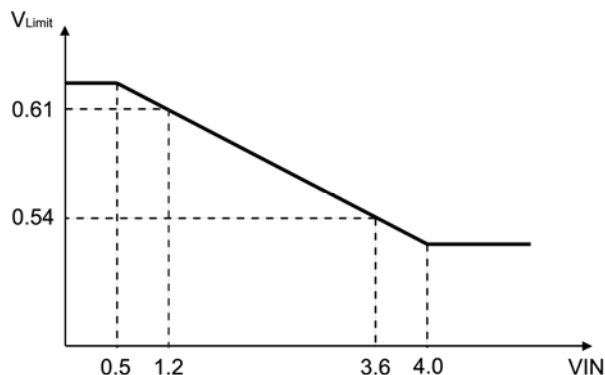


Figure 27. Constant Power Control

## Protections

The FSL127H provides protection functions to prevent the power supply and the load from being damaged. The protection features include:

### Latch / Auto Recovery Function

The FSL127H provides additional protections by the VIN pin, such as pull-HIGH latch and pull-LOW auto recovery that depend on the application. As shown in Figure 28, when VIN level is higher than 4.7V, FSL127H is latched until the VDD is discharged. FSL127H is in auto recovery when the VIN level is lower than 0.3V.

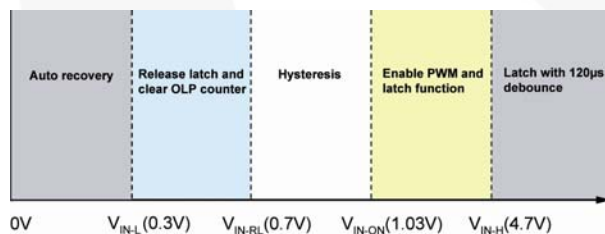


Figure 28. VIN Pin Function

### Open-Loop / Overload Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator (KA431 shown) is broken, as shown in Figure 29, or over-current or output short occurs; there is no current flowing through the opto-coupler transistor, which pulls up the feedback voltage to 6V. When the feedback voltage is above 4.6V for longer than 56ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value longer than 56ms due to the overload condition.

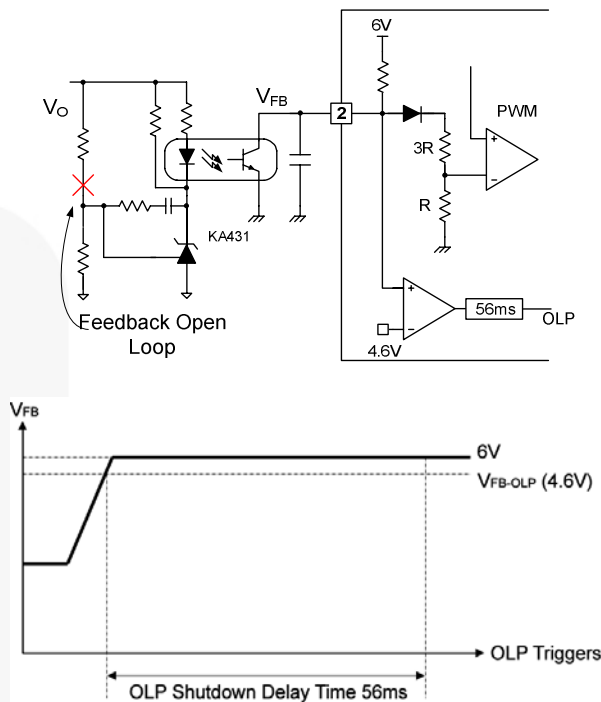


Figure 29. OLP Operation

### VDD Over-Voltage Protection (OVP)

VDD over-voltage protection prevents IC damage caused by over voltage on the VDD pin. The OVP is triggered when VDD reaches 28V. It has a debounce time (typically 130µs) to prevent false trigger by switching noise.

### Over-Temperature Protection (OTP)

The SenseFET and the control IC are integrated, making it easier to detect the temperature of the SenseFET. When the temperature exceeds approximately 142°C, thermal shutdown is activated.

## Typical Application Circuit

Application	Fairchild Devices	Input Voltage Range	Output
Adapter	FSL127H	90~264V <sub>AC</sub>	12V/0.85A (10.2W)

### Features

- High efficiency (>76.74% at full load) meeting Energy Star V2.0 regulation with enough margin
- Standby power <100mW at no-load condition
- Provides full protection functions, including:

OVP	OTP	OLP	VIN-H	VIN-L
Latch	Latch	Auto Restart	Latch	Auto Restart

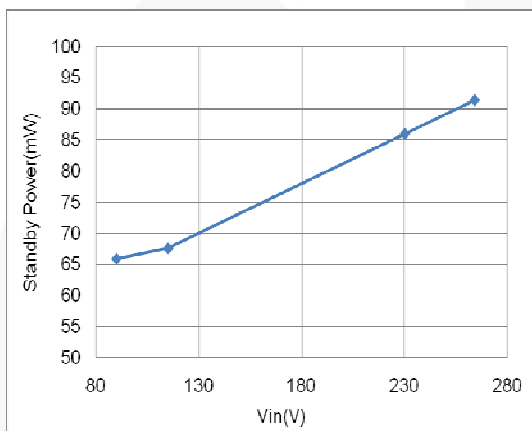


Figure 30. Measured Standby Power

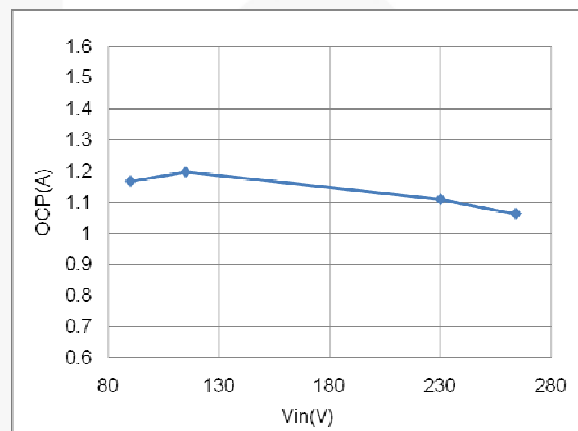


Figure 31. Over-Current Protection

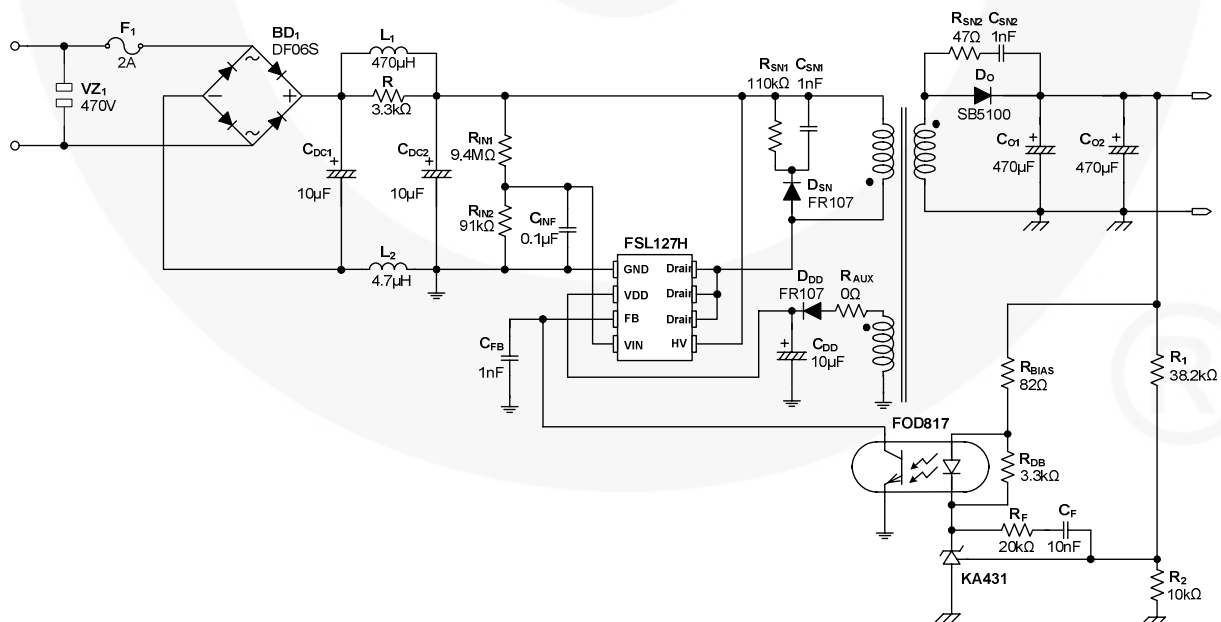


Figure 32. Schematic of Typical Application Circuit

## Typical Application Circuit (Continued)

### Transformer Specification

- Core: EE16
- Bobbin: EE16

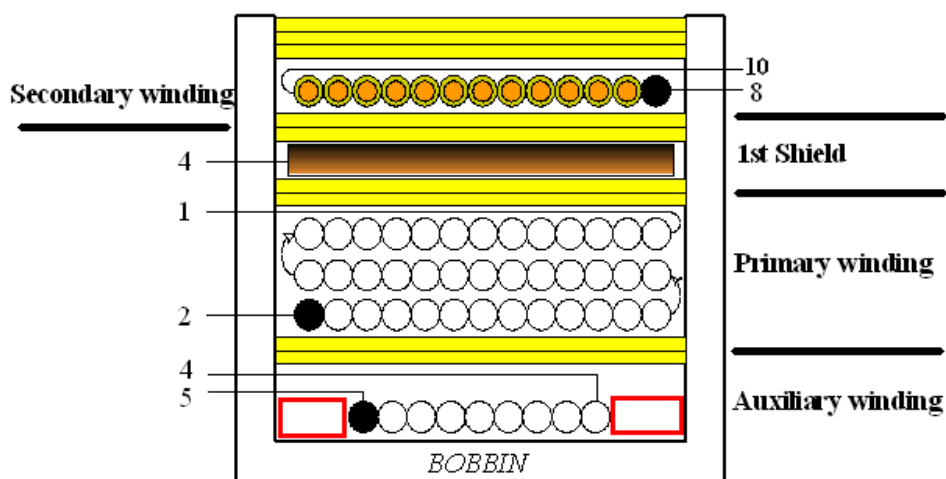
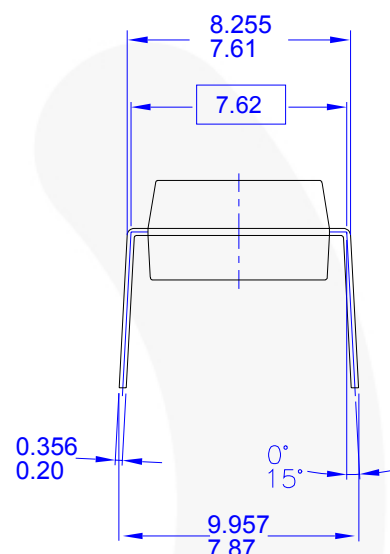
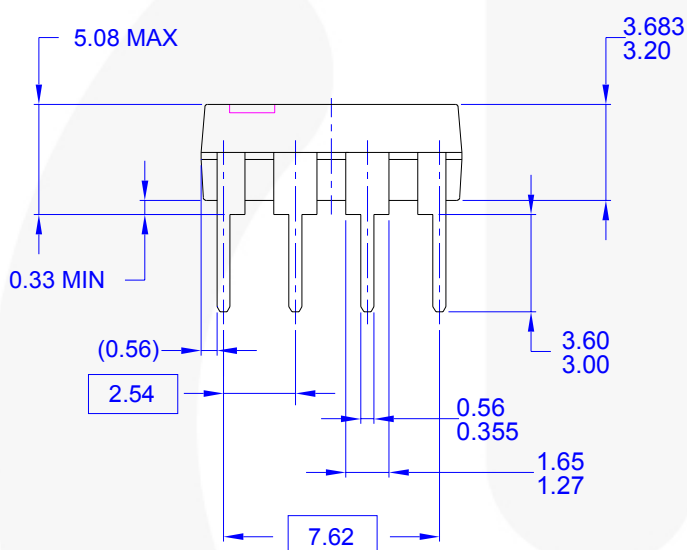


Figure 33. Transformer Diagram

NO.	TERMINAL		WIRE	Ts
	S	F		
W1	5	4	2UEW 0.3*1	13
W2	2	1	2UEW 0.26*1	75
W3	4		COPPER SHIELD	1.2
W4	8	10	TEX-E 0.35*1	13
			CORE ROUNDING TAPE	3
Primary-Side Inductance=880μH ±5%				
Primary-Side Effective Leakage<20μH ±5%				

Technical drawing of a rectangular component with dimensions:

- Overall width: 9.83 (nominal), 9.00 (actual)
- Overall height: 6.67 (nominal), 6.096 (actual)
- Top edge features: 8 (left), 5 (right)
- Bottom edge features: 1 (left), 4 (right)
- Internal features: A circle on the left and a vertical dashed line on the right.



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**Figure 34. 8-pin Dual In-Line Package (DIP)**

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