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February 2013

FSFA2100 — Fairchild Power Switch (FPS™) for Half-Bridge PWM Converters

Features

- Optimized for Complementary Driven Half-Bridge Soft-Switching Converters
- Can be Applied to Various Topologies: Asymmetric PWM Half-Bridge Converters, Asymmetric PWM Flyback Converters, Asymmetric PWM Forward Converters, Active Clamp Flyback Converters
- High Efficiency through Zero-Voltage-Switching (ZVS)
- Internal SuperFET™s with Fast-Recovery Type Body Diode (t_{rr}=120 ns)
- Fixed Dead Time (200 ns) Optimized for MOSFETs
- Up to 300 kHz Operating Frequency
- Internal Soft-Start
- Pulse-by-Pulse Current Limit
- Burst-Mode Operation for Low Standby Power Consumption
- Protection Functions: Over-Voltage Protection (OVP), Over-Load Protection (OLP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD)

Applications

- PDP and LCD TVs
- Desktop PCs and Servers
- Adapters
- Telecom Power Supplies

Description

The growing demand for higher power density and low profile in power converter designs has forced designers to increase switching frequencies. Operation at higher frequencies considerably reduces the size of passive components, such as transformers and filters. However, switching losses have been an obstacle to high-frequency operation. To reduce switching losses and allow high-frequency operation, Pulse Width Modulation (PWM) with soft-switching techniques have been developed. These techniques allow switching devices to be softly commutated, which dramatically reduces the switching losses and noise.

FSFA2100 is an integrated PWM controller and SuperFET™ specifically designed for Zero-Voltage-Switching (ZVS) half-bridge converters with minimal external components. The internal controller includes an oscillator, under-voltage-lockout, leading-edge blanking (LEB), optimized high-side and low-side gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation and self-protection circuitry. Compared with discrete MOSFET and PWM controller solution, FSFA2100 can reduce total cost; component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability.

Ordering Information

Part Number	Operating Junction Temperature	$R_{DS(ON\_MAX)}$	Maximum Output Power without Heatsink (V_{IN}=350~400 V)(1,2)	Maximum Output Power with Heatsink (V_{IN}=350~400 V)(1,2)	Package
FSFA2100	-40 to +130°C	0.38 Ω	200 W	450 W	9-SIP

Notes:

1. The junction temperature can limit the maximum output power.
2. Maximum practical continuous power in an open-frame design at 50°C ambient.

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Circuit Diagram

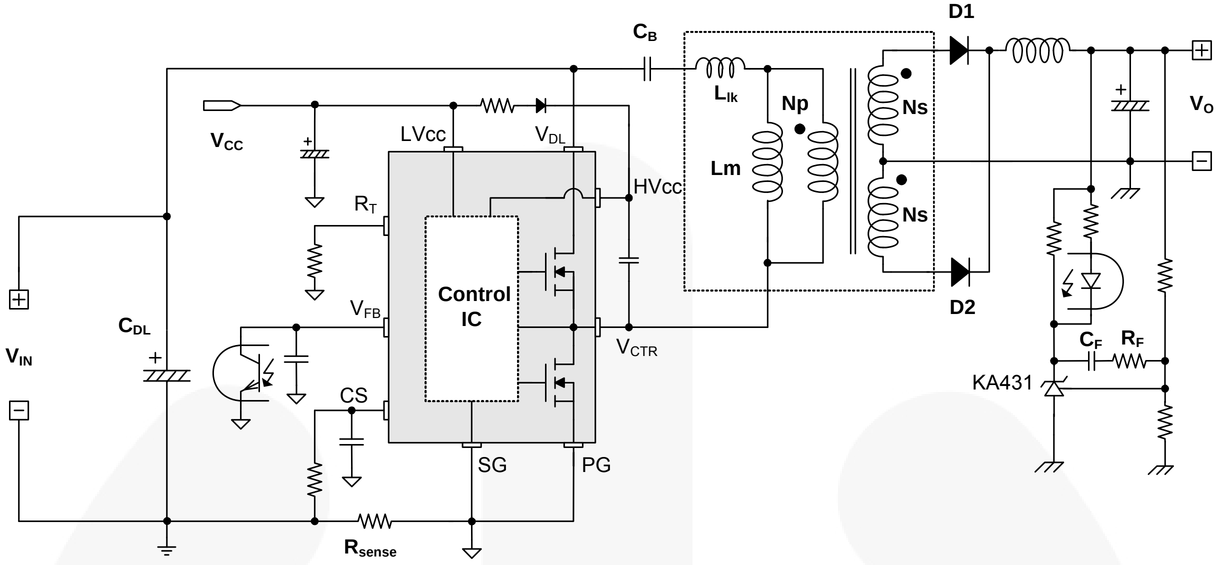


Figure 1. Typical Application Circuit for an Asymmetric PWM Half-Bridge Converter

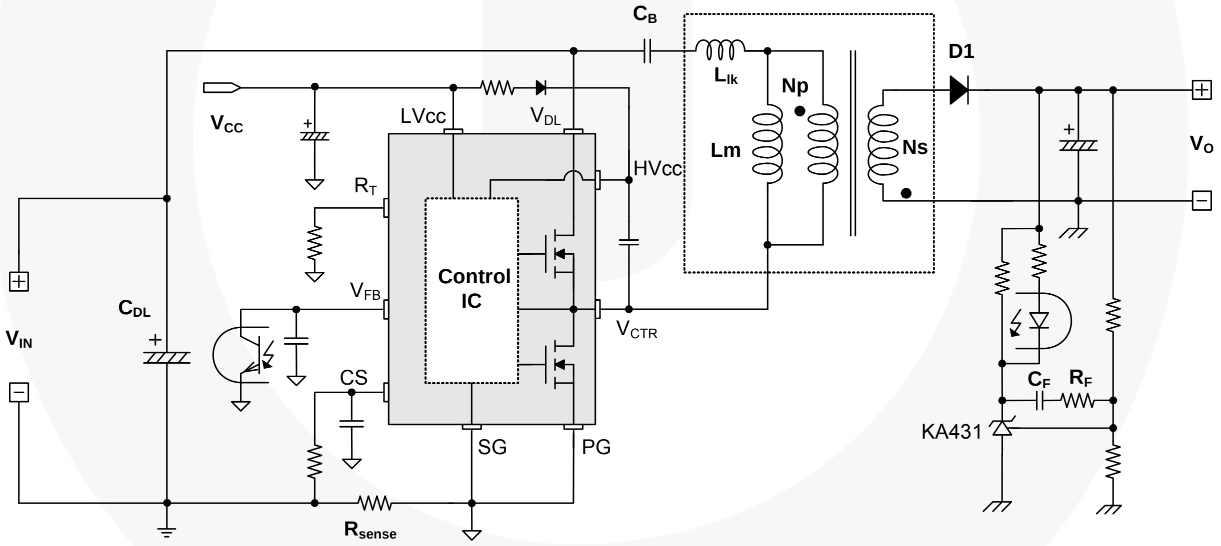


Figure 2. Typical Application Circuit for an Asymmetric PWM Flyback Converter

Block Diagram

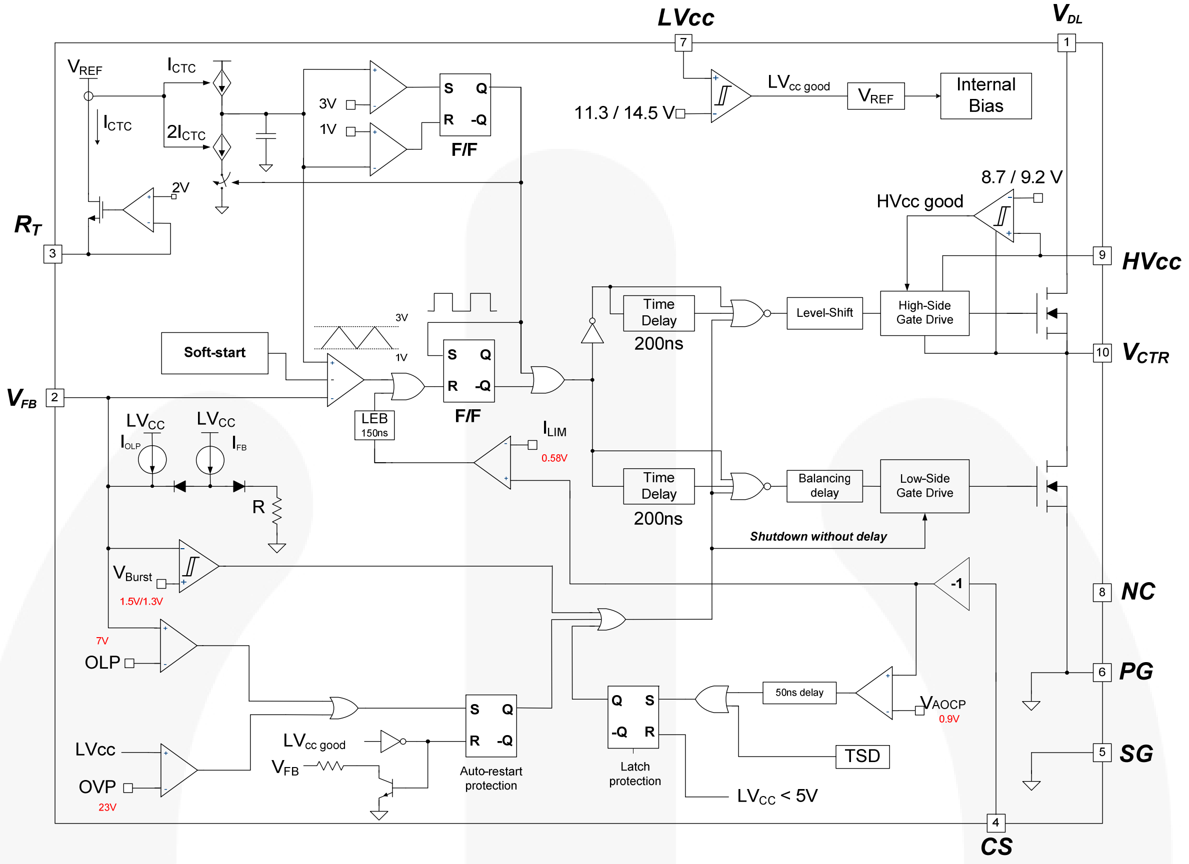


Figure 3. Internal Block Diagram

Pin Configuration

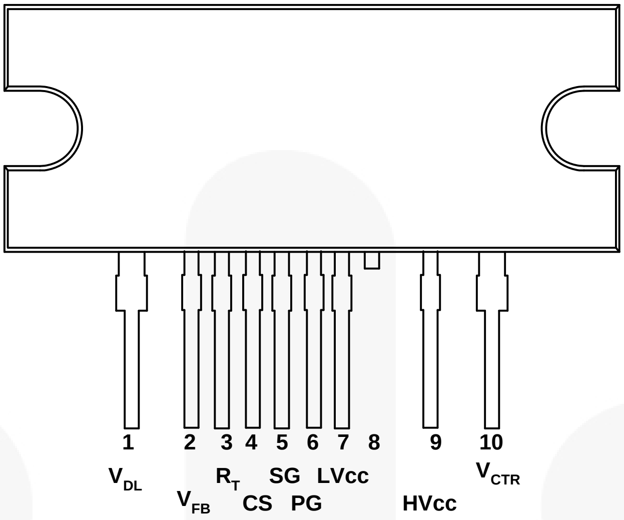


Figure 4. Package Diagram

Pin Definitions

Pin #	Name	Description
1	V_{DL}	This is the drain of the high-side MOSFET, typically connected to the input DC link voltage.
2	V_{FB}	This pin is connected to the inverting input of the PWM comparator internally and to the opto-coupler externally. The duty cycle is determined by the voltage on this pin.
3	R_T	This pin programs the switching frequency using a resistor.
4	CS	This pin senses the current flowing through the low-side MOSFET. Typically, negative voltage is applied on this pin.
5	SG	This pin is the control ground.
6	PG	This pin is the power ground. This pin is connected to the source of the low-side MOSFET.
7	LV_{CC}	This pin is the supply voltage of the control IC.
8	NC	No connection.
9	HV_{CC}	This is the supply voltage of the high-side gate-drive circuit IC.
10	V_{CTR}	This is the drain of the low-side MOSFET. Typically, a transformer is connected to this pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C unless otherwise specified.

Symbol	Parameter		Min.	Max.	Unit
V_{DS}	Maximum Drain-to-Source Voltage (V_{DL}-V_{CTR} and V_{CTR-PG})		600		V
LV_{CC}	Low-Side Supply Voltage		-0.3	25.0	V
HV_{CC} to V_{CTR}	High-Side V_{CC} Pin to Low-Side Drain Voltage		-0.3	25.0	V
HV_{CC}	High-Side Floating Supply Voltage		-0.3	625.0	V
V_{FB}	Feedback Pin Input Voltage		-0.3	LV_{CC}	V
V_{CS}	Current Sense (CS) Pin Input Voltage		-5.0	1.0	V
V_{RT}	R_T Pin Input Voltage		-0.3	5.0	V
dV_{CTR}/dt	Allowable Low-Side MOSFET Drain Voltage Slew Rate			50	V/ns
P_D	Total Power Dissipation(3)			12.0	W
T_J	Maximum Junction Temperature(4)			+150	°C
	Recommended Operating Junction Temperature(4)		-40	+130	
T_{STG}	Storage Temperature Range		-55	+150	°C
MOSFET Section					
V_{DGR}	Drain Gate Voltage (R_{GS}=1MΩ)		600		V
V_{GS}	Gate Source (GND) Voltage			±30	V
I_{DM}	Drain Current Pulsed			33	A
I_D	Continuous Drain Current	T_C=25°C		11	A
		T_C=100°C		7	
Package Section					
Torque	Recommended Screw Torque		5~7		kgf·cm

Notes:
3. Per MOSFET when both MOSFETs are conducting.
4. The maximum value of the recommended operating junction temperature is limited by thermal shutdown.

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JC}	Junction-to-Case Center Thermal Impedance (Both MOSFETs Conducting)	10.44	ºC/W
θ_{JA}	Junction-to-Ambient Thermal Impedance	80	ºC/W

Electrical Characteristics

T_A=25°C and LV_{CC}=17 V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MOSFET Section						
BV_{DSS}	Drain-to-Source Breakdown Voltage	I_D=200 μA, T_A=25°C	600			V
		I_D=200 μA, T_A=125°C		650		
$R_{DS(ON)}$	On-State Resistance	V_{GS}=10 V, I_D=5.5 A		0.32	0.38	Ω
t_{rr}	Body Diode Reverse Recovery Time(5)	V_{GS}=0 V, I_{Diode}=11.0 A, dI_{Diode}/dt=100 A/μs		120		ns
C_{ISS}	Input Capacitance(5)	V_{DS}=25 V, V_{GS}=0 V, f=1.0 MHz		1148		pF
C_{OSS}	Output Capacitance(5)			671		pF
Supply Section						
I_{LK}	Offset Supply Leakage Current	$HV_{CC}=V_{CTR}$=600 V			50	μA
I_QHV_{CC}	Quiescent HV_{CC} Supply Current	(HV_{CC}UV+) - 0.1 V		50	120	μA
I_QLV_{CC}	Quiescent LV_{CC} Supply Current	(LV_{CC}UV+) - 0.1 V		100	200	μA
I_OHV_{CC}	Operating HV_{CC} Supply Current (RMS Value)	f_{OSC}=100 KHz, V_{FB} > 3 V HV_{CC}=17 V		6	9	mA
		No switching, V_{FB} < 1V HV_{CC}=17 V		100	200	μA
I_OLV_{CC}	Operating LV_{CC} Supply Current (RMS Value)	f_{OSC}=100 KHz, V_{FB} > 3 V		7	11	mA
		No Switching, V_{FB} < 1 V		2	4	mA
UVLO Section						
LV_{CC}UV+	LV_{CC} Supply Under-Voltage Positive Going Threshold (LV_{CC} Start)		13.0	14.5	16.0	V
LV_{CC}UV-	LV_{CC} Supply Under-Voltage Negative Going Threshold (LV_{CC} Stop)		10.2	11.3	12.4	V
LV_{CC}UVH	LV_{CC} Supply Under-Voltage Hysteresis			3.2		V
HV_{CC}UV+	HV_{CC} Supply Under-Voltage Positive Going Threshold (HV_{CC} Start)		8.2	9.2	10.2	V
HV_{CC}UV-	HV_{CC} Supply Under-Voltage Negative Going Threshold (HV_{CC} Stop)		7.8	8.7	9.6	V
HV_{CC}UVH	HV_{CC} Supply Under-Voltage Hysteresis			0.5		V
Oscillator and Feedback Section						
V_{RT}	V-I Converter Threshold Voltage		1.5	2.0	2.5	V
f_{OSC}	Output Oscillation Frequency	R_T=27 KΩ	94	100	106	KHz
D_{MAX}	Maximum Duty Cycle	V_{FB}=4 V	45	50	55	%
D_{MIN}	Minimum Duty Cycle	V_{FB}=0 V			0	%
V_{FB}^{MAX}	Maximum Feedback Voltage for D_{MAX}	D_{MAX} ≥ 48%	2.7	3.0	3.3	V
I_{FB}	Feedback Source Current	V_{FB}=0 V	370	470	570	μA
V_{BH}	Burst Mode High-Threshold Voltage		1.34	1.50	1.66	V
V_{BL}	Burst Mode Low-Threshold Voltage		1.16	1.30	1.44	V
V_{BHY}	Burst Mode Hysteresis Voltage		0.1	0.2	0.3	V
t_{SS}	Internal Soft-Start Time	f_{OSC}=100 kHz	10	15	20	ms

Continued on the following page…

Electrical Characteristics (Continued)

T_A=25°C and LV_{CC}=17 V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Protection Section						
I_{OLP}	OLP Delay Current	V_{FB}=5 V	3.8	5.0	6.2	µA
V_{OLP}	OLP Protection Voltage	V_{FB} > 6 V	6.3	7.0	7.7	V
V_{OVP}	LV_{CC} Over-Voltage Protection	LV_{CC} > 21 V	21	23	25	V
V_{AOCP}	AOCP Threshold Voltage	ΔV/Δt=-1 V/µs	-1.0	-0.9	-0.8	V
t_{BAO}	AOCP Blanking Time(5)	$V_{CS} < V_{AOCP}$; ΔV/Δt=-1 V/µs		50		ns
t_{DA}	Delay Time (Low-Side) from V_{AOCP} to Switch Off(5)	ΔV/Δt=-1 V/µs		250	400	ns
V_{LIM}	Pulse-by-Pulse Current Limit Threshold Voltage	ΔV/Δt=-0.1 V/µs	-0.64	-0.58	-0.52	V
t_{BL}	Pulse-by-Pulse Current Limit Blanking Time	$V_{CS} < V_{LIM}$; ΔV/Δt=-0.1 V/µs		150		ns
t_{DL}	Delay Time (Low-Side) from V_{LIM} to Switch Off(5)	ΔV/Δt=-0.1 V/µs		450		ns
T_{SD}	Thermal Shutdown Temperature(5)		110	130	150	°C
I_{SU}	Protection Latch Sustain LV_{CC} Supply Current	LV_{CC}=7.5 V		100	150	µA
V_{PRSET}	Protection Latch Reset LV_{CC} Supply Voltage		5			V
Dead-Time Control Section						
D_T	Dead Time(6)			200		ns

Notes:

5. This parameter, although guaranteed, is not tested in production.
6. These parameters, although guaranteed, are tested only in EDS (wafer test) process.

Typical Performance Characteristics

These characteristic graphs are normalized at T_A=25°C.

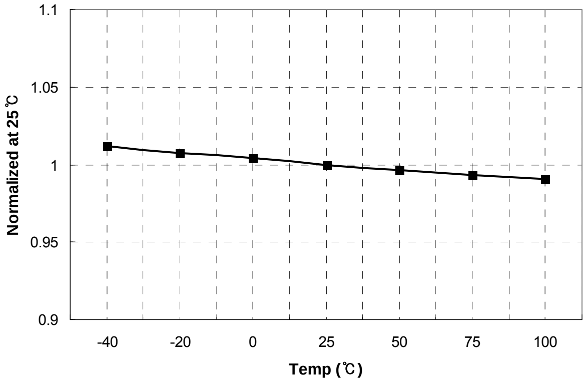


Figure 5. Maximum Duty Cycle vs. Temperature

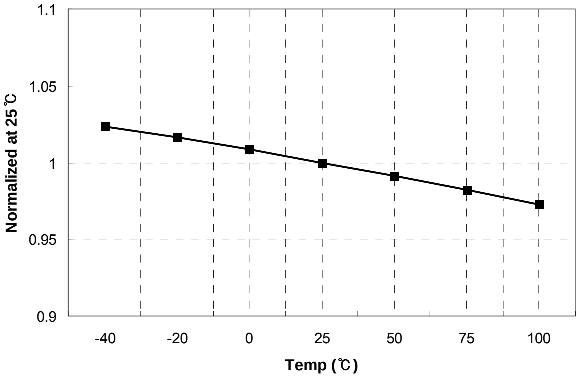


Figure 6. Switching Frequency vs. Temperature

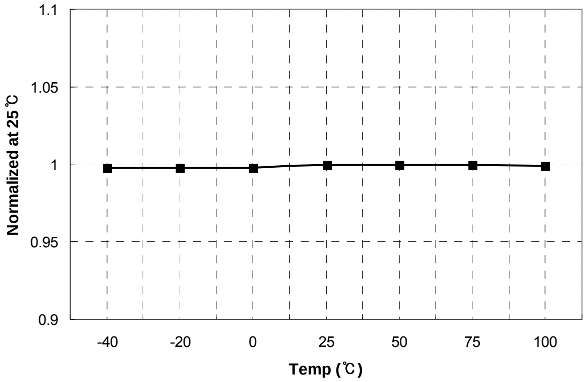


Figure 7. High-Side V_{CC} (HV_{CC}) Start vs. Temperature

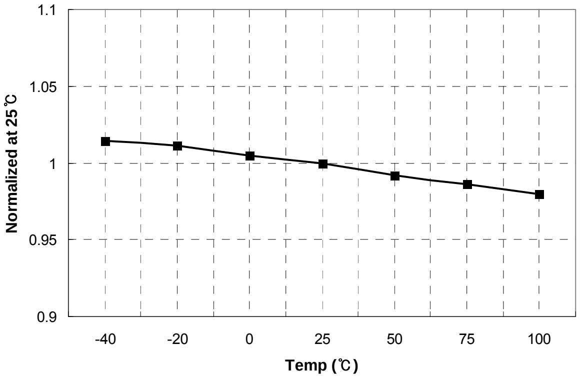


Figure 8. High-Side V_{CC} (HV_{CC}) Stop vs. Temperature

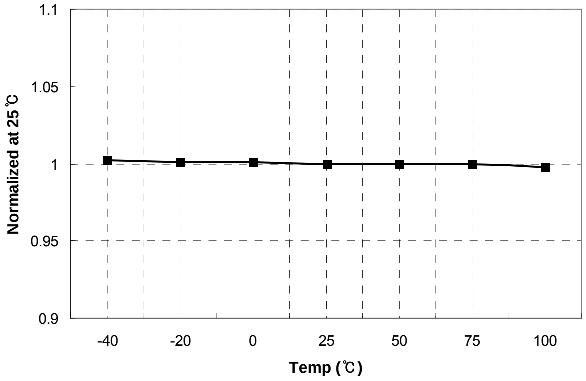


Figure 9. Low-Side V_{CC} (LV_{CC}) Start vs. Temperature

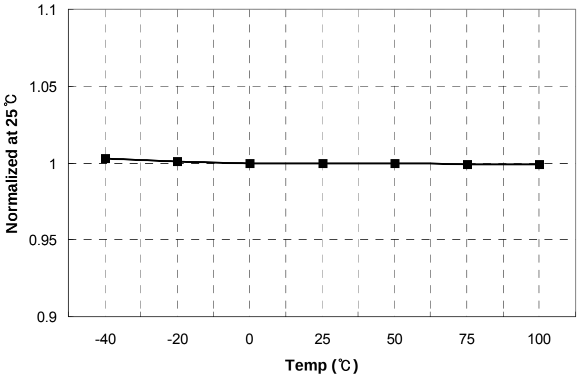


Figure 10. Low-Side V_{CC} (LV_{CC}) Stop vs. Temperature

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A=25°C.

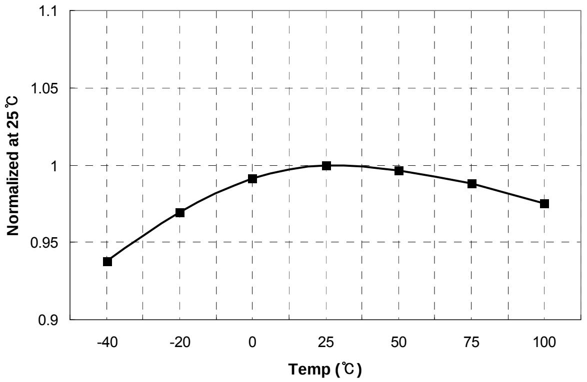


Figure 11. OLP Delay Current vs. Temperature

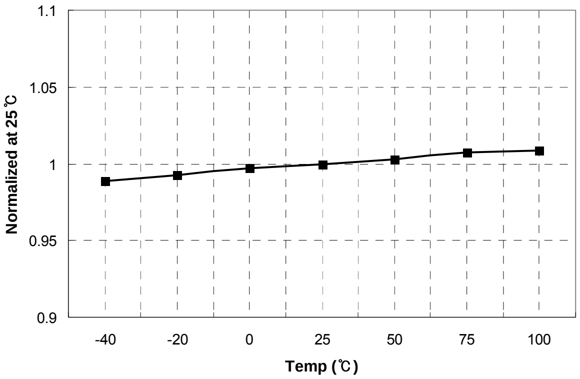


Figure 12. OLP Voltage vs. Temperature

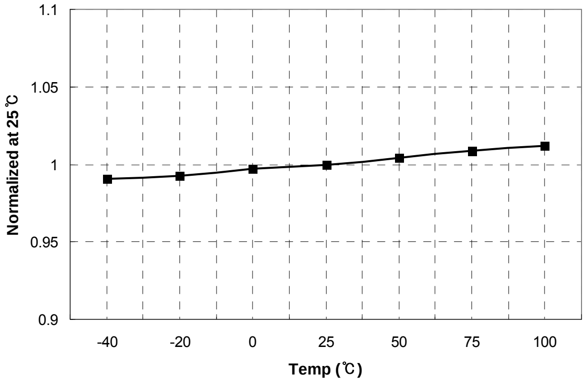


Figure 13. LV_{CC} OVP Voltage vs. Temperature

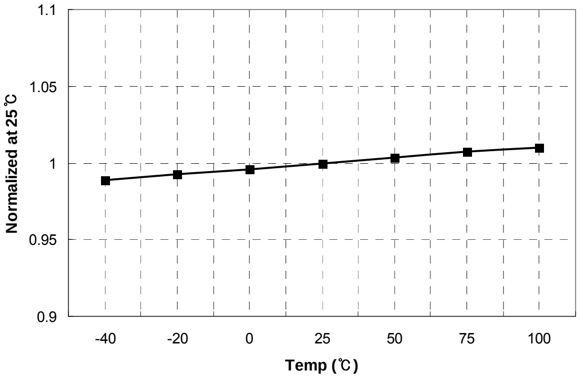


Figure 14. R_T Voltage vs. Temperature

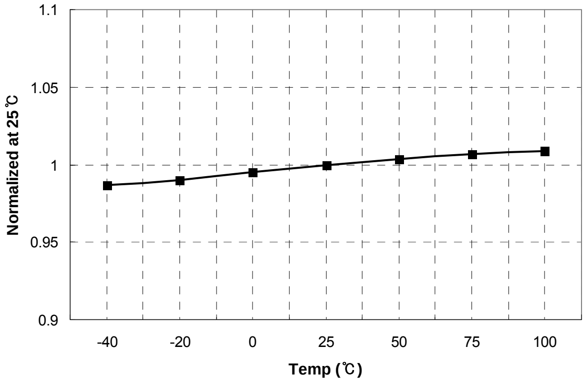


Figure 15. V_{BH} Voltage vs. Temperature

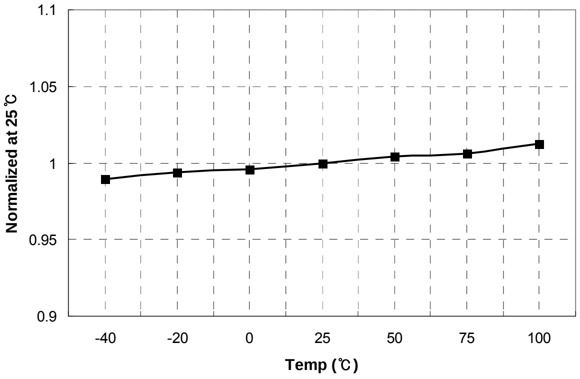


Figure 16. V_{LIM} Voltage vs. Temperature

Functional Description

1. Internal Oscillator: FSFA2100 employs a current-controlled oscillator as shown in Figure 17. Internally, the voltage of the R_T pin is regulated at 2 V and the charging/discharging current for the oscillator capacitor C_T is determined by the current flowing out of the R_T pin (I_{CTC}). When the R_T pin is pulled down to the ground with a resistor R_{SET}, the switching frequency is fixed as:

$$f_S = \frac{27k\Omega}{R_{SET}} \times 100(kHz) \qquad (1)$$

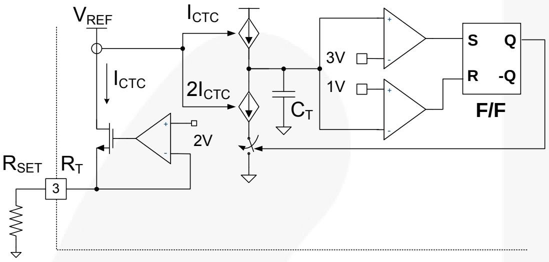


Figure 17. Current Controlled Oscillator

2. PWM Control: Figure 18 shows the typical control circuit configuration. The opto-coupler transistor should be connected to the V_{FB} pin in parallel with the feedback capacitor to control the duty cycle.

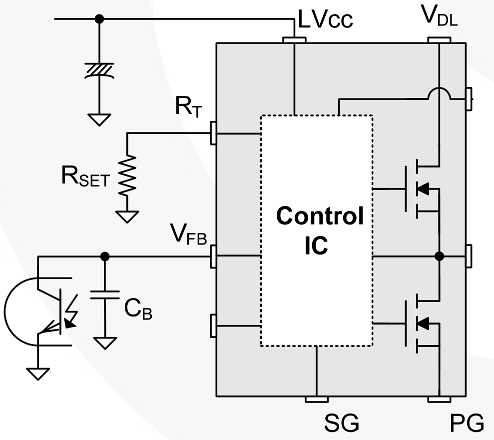


Figure 18. PWM Control Configuration

Figure 19 shows the internal block diagram for PWM operation. Duty cycle is controlled by comparing the feedback voltage to the triangular signal with a range from 1 V to 3 V.

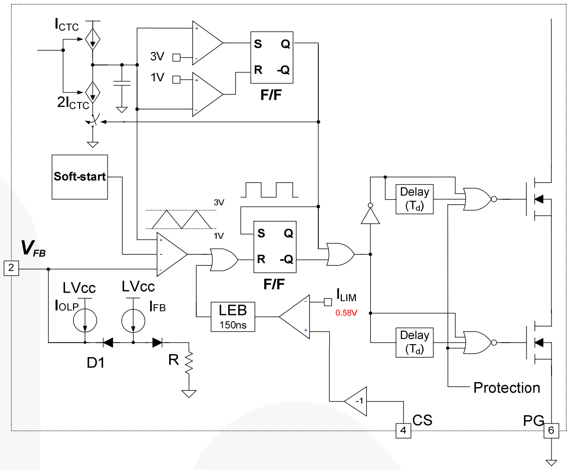


Figure 19. Internal PWM Block Diagram

3. Protection Circuits: The FSFA2100 has Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD) self-protective functions. The OLP and OVP are auto-restart mode protections, while the AOCP and TSD are latch-mode protections, as shown in Figure 20.

Auto-restart mode protection: Once the fault condition is detected, the switching is terminated and the MOSFETs remain off. When LV_{CC} falls down to LV_{CC} stop voltage of around 11V, the protection is reset. The FPS resumes normal operation when LV_{CC} reaches the start voltage of about 14 V.

Latch-mode protection: Once this protection is triggered, the switching is terminated and the MOSFETs remain off. The latch is reset only when LV_{CC} is discharged below 5 V.

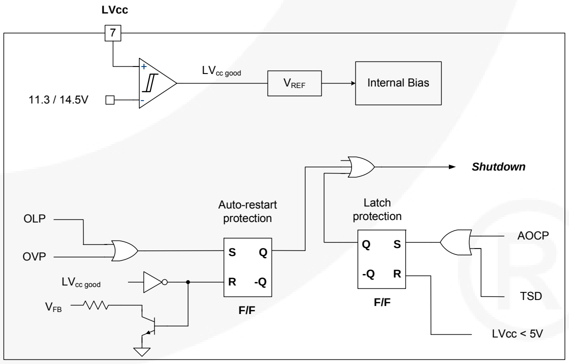


Figure 20. Protection blocks

Low-side MOSFET current should be sensed for Pulse-by-pulse current limit and AOCP. The FSFA2100 senses drain current as a negative voltage, as shown in Figure 21 and Figure 22. Half-wave sensing allows low-power dissipation in the sensing resistor, while full-wave sensing has less noise in the sensing signal.

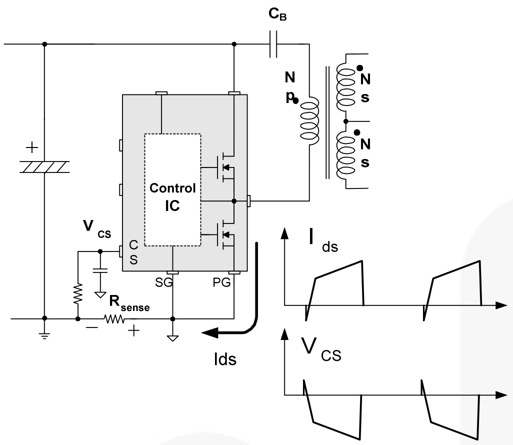


Figure 21. Half-Wave Sensing

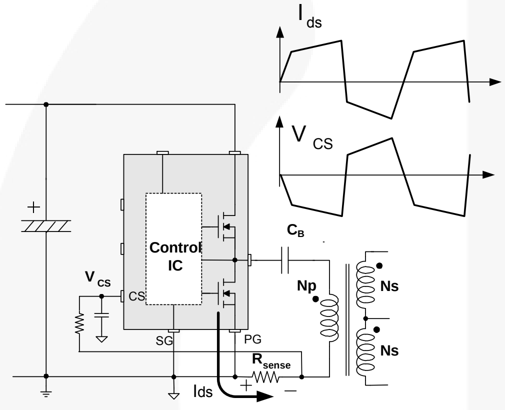


Figure 22. Full-Wave Sensing

3.1 Pulse-by-Pulse Current Limit: In normal operation, the duty cycle of the low-side MOSFET is determined by comparing the internal triangular signal with the feedback voltage. However, the low-side MOSFET is forced to turn off when the current sense pin voltage reaches -0.58 V. This operation limits the drain current below a pre-determined level to avoid the destruction of the MOSFETs.

3.2 Abnormal Over-Current Protection (AOCP): If one of the secondary rectifier diodes is short-circuited, large current with extremely high di/dt can flow through the MOSFET before OCP or OLP is triggered. AOCP is triggered with a very short shutdown delay time when the sensed voltage drops below -0.9 V. This protection is latch mode and reset only when LV_{CC} is pulled below 5 V.

3.3 Overload Protection (OLP): Overload is defined as the load current exceeding its nominal level due to an unexpected abnormal event. In this situation, a protection circuit should trigger to protect the power supply. However, even when the power supply is in the normal condition, the OLP circuit can be triggered during the load transition. To avoid this undesired operation, the OLP circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the MOSFET is limited; and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the nominal voltage. This reduces the current through the opto-coupler diode, which also reduces the opto-coupler transistor current, increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, D1, which is illustrated in Figure 19, is blocked and the OLP current source starts to charge C_B slowly, as shown in Figure 23. In this condition, V_{FB} continues increasing until it reaches 7V, then the switching operation is terminated, as shown in Figure 23. The delay time for shutdown is the time required to charge C_B from 3V to 7V with 5μA, as given by:

$$t_{delay} = \frac{(7V - 3V)\times C_B}{5\mu A} \qquad (2)$$

A 30 ~ 50ms delay time is typical for most applications.

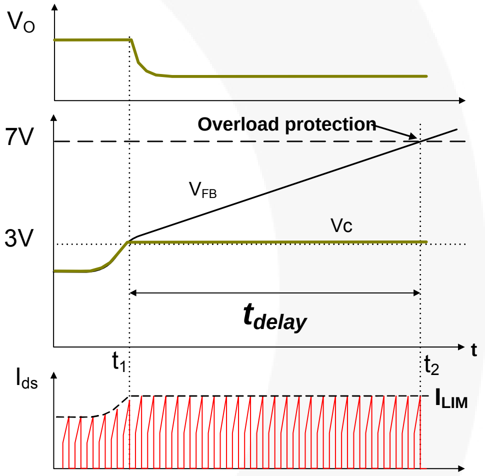


Figure 23. Overload Protection

3.4 Over-Voltage Protection (OVP): When the LV_{CC} reaches 23V, OVP is triggered. This protection is enabled when using an auxiliary winding of the transformer to supply LV_{CC} to FPS.

3.5 Thermal Shutdown (TSD): The MOSFETs and the control IC are built in one package. This allows the control IC to detect the abnormal over-temperature of the MOSFET. If the temperature exceeds approximately 130°C, the thermal shutdown triggers.

4. Soft-Start: At startup, the duty cycle starts increasing slowly to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. Soft-start time is internally implemented for 15 ms (when the operating frequency is set to 100 kHz.) In addition, to help the soft-start operation, a capacitor and a resistor would be connected on the R_T pin externally, as shown in Figure 24. Before the power supply is powered on, the capacitor C_{SS} remains fully discharged. After power-on, C_{SS} becomes charged progressively by the current through the R_T pin, which determines the operating frequency. The current through the R_T pin is inversely proportional to the total impedance of the connected resistors. The total impedance at startup is lower than that of the normal operation because R_{SS} is added on R_{SET} in parallel, which means the operating frequency decreases continuously from higher to nominal. Eventually C_{SS} is fully charged to the R_T pin voltage and the operating frequency is determined by R_{SET} only.

During the charging time of C_{SS}, the operating frequency is higher than during normal operation. In asymmetric half-bridge converters, a switching period contains powering and commutation periods. The energy cannot be transferred to the output side during commutation period. Since the DC link voltage applied to the V_{DL} pin and the leakage inductance of the main transformer are fixed, the powering period over the switching period is shorter in high switching frequencies. As C_{SS} is charged, the switching frequency decreases and the powering period over the switching period increases as well. It is helpful to start SMPS softly with the internal soft-start time together.

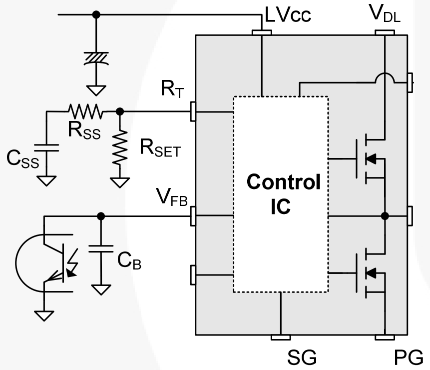


Figure 24. External Soft-Start Circuit

5. Startup: Due to the imbalance of the turn-off resistance between the high- and low-side MOSFETs, the voltage across the DC blocking capacitor cannot be predicted at startup. Additionally, the high-side MOSFET starts with a large duty cycle since the duty cycle of the low-side MOSFET increases step-by-step during soft-start time. Therefore, in the case where high voltage is already charged in the DC blocking capacitor due to the higher turn-off resistance of the high-side MOSFET before startup, a large primary current could flow through the high-side MOSFET during turn-on time after startup.

For the high-side MOSFET, a long duty cycle and high applied voltage make an excessive primary current. When the high-side MOSFET turns off, the primary current flows back to the DC link capacitor through the body diode of the low-side MOSFET. It keeps the same status even after turning on and off the low-side MOSFET. When the high-side MOSFET turns on again, a huge current can flow from the DC link capacitor through the channel of the high-side MOSFET and body diode of the low-side one due to the reverse recovery. It may induce unexpected noise into CS pin.

To avoid this issue, the voltage across the DC blocking capacitor must be low enough. In general, two resistors with several MHz can be added on the drain-to-source terminals of each MOSFET to divide the DC link voltage.

6. Burst Operation: To minimize power dissipation in standby mode, the FSFA2100 enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 25, the device automatically enters burst mode when the feedback voltage drops below V_{BL} (1.3 V). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BH} (1.5 V), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the MOSFETs, thereby reducing switching loss in standby mode.

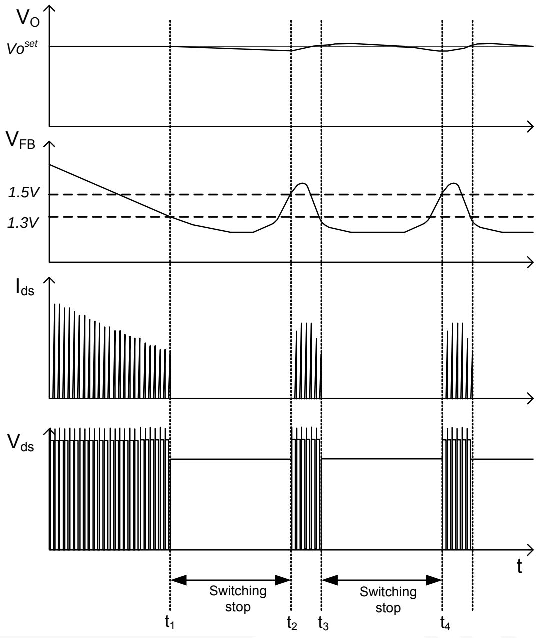


Figure 25. Burst-Mode Operation

Typical Application Circuit (Asymmetric PWM Half-Bridge Converter)

Application	FPS™ Device	Input Voltage Range	Rated Output Power	Output Voltage (Rated Current)
LCD TV	FSFA2100	400 V	200 W	25 V-8 A

Features

- High Efficiency (>93% at 400 V_{IN} input)
- Reduced EMI Noise through Zero-Voltage-Switching (ZVS)
- Enhanced System Reliability with Various Protection Functions
- Internal Soft-Start (15 ms)

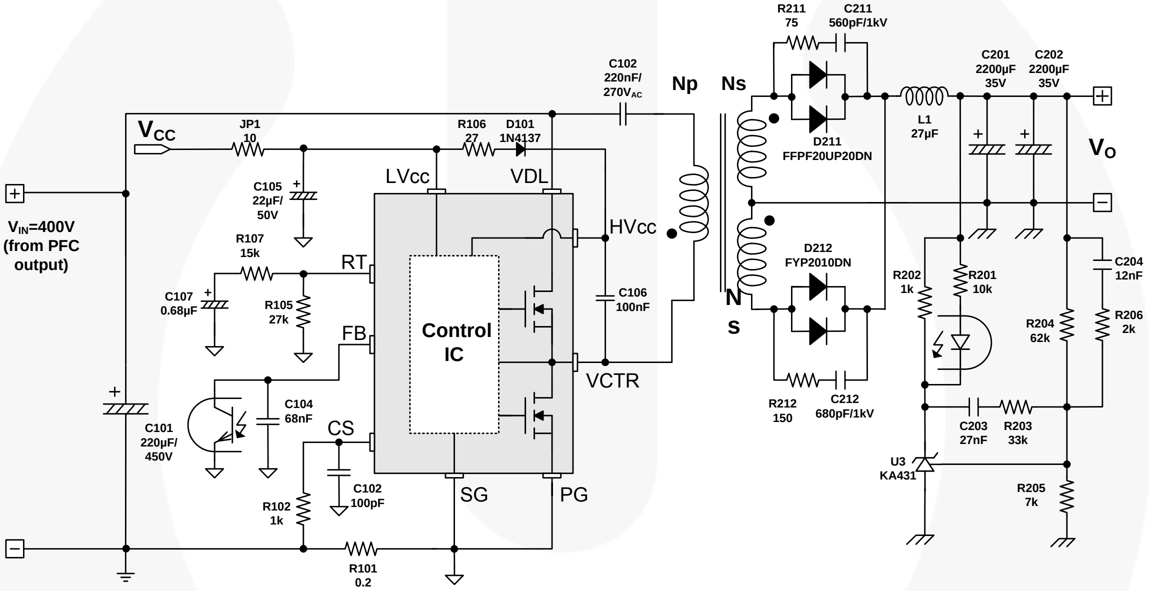


Figure 26. Typical Application Circuit

Typical Application Circuit (Continued)

- Core: EER3542 (Ae=107 mm^2)
- Bobbin: EER3542 (Horizontal)

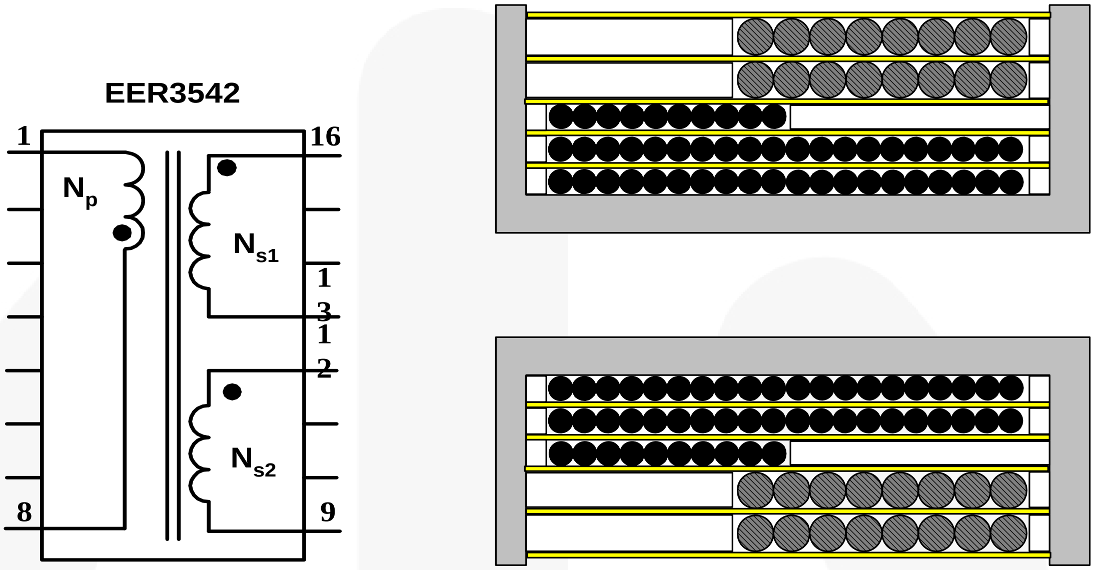
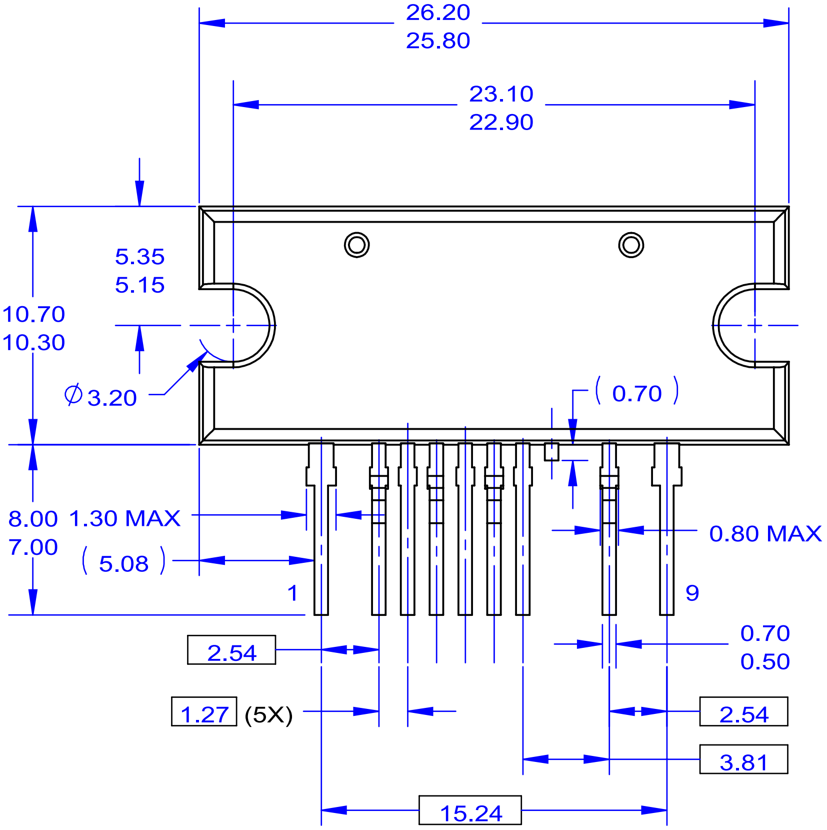


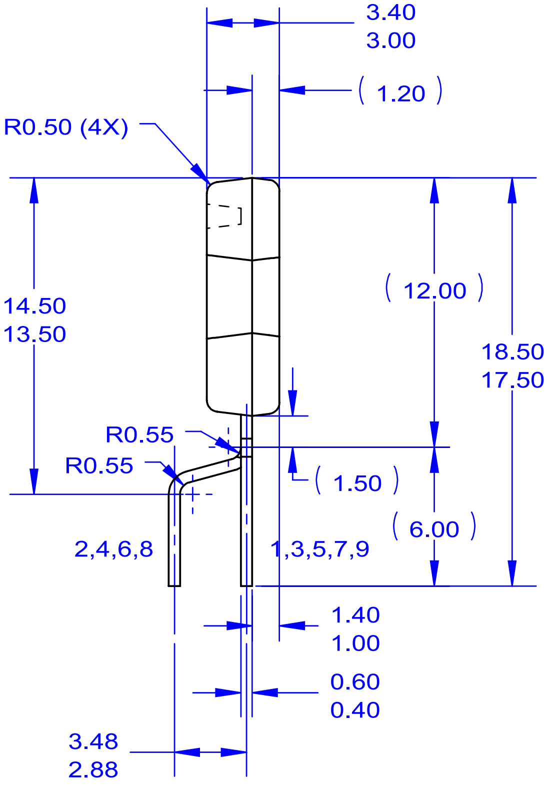
Figure 27. Core and Winding

	Pin (S → F)	Wire	Turns	Winding Method
N_p	8 → 1	0.12φ×30 (Litz Wire)	50	Solenoid Winding
N_{s1}	16 → 13	0.1φ×100 (Litz Wire)	8	Solenoid Winding
N_{s2}	12 → 9	0.1φ×100 (Litz Wire)	8	Solenoid Winding

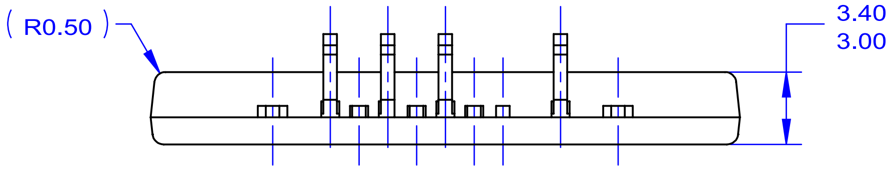
	Pin	Specification	Remark
Inductance	1–8	630 µH ± 5%	100 kHz, 1 V
Leakage	1–8	45 µH ± 10%	Short One of the Secondary Windings



FRONT VIEW



RIGHT SIDE VIEW



BOTTOM VIEW

FAIRCHILD ™

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