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July 2015

FQT7N10L

N-Channel QFET[®] MOSFET

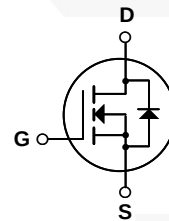
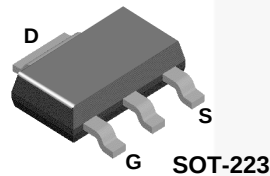
100 V, 1.7 A, 350 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 1.7 A, 100 V, $R_{DS(on)}=350\text{ m}\Omega(\text{Max.})$ @ $V_{GS}=10\text{ V}$, $I_D=0.85\text{ A}$
- Low Gate Charge (Typ. 5.8 nC)
- Low C_{rss} (Typ. 10 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQT7N10L	Unit
V_{DSS}	Drain-Source Voltage	100	V
I_D	Drain Current - Continuous ($T_A = 25^\circ\text{C}$)	1.7	A
	- Continuous ($T_A = 70^\circ\text{C}$)	1.36	A
I_{DM}	Drain Current - Pulsed (Note 1)	6.8	A
V_{GSS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	50	mJ
I_{AR}	Avalanche Current (Note 1)	1.7	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.2	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$)	2.0	W
	- Derate above 25°C	0.016	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	62.5	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)

FQT7N10L N-Channel MOSFET

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	--	--	V
$\Delta V_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.1	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 80\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.85\text{ A}$	--	0.275	0.35	Ω
		$V_{GS} = 5\text{ V}, I_D = 0.85\text{ A}$	--	0.300	0.38	
g_{FS}	Forward Transconductance	$V_{DS} = 30\text{ V}, I_D = 0.85\text{ A}$ (Note 4)	--	2.75	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	220	290	pF
C_{oss}	Output Capacitance		--	55	72	pF
C_{rss}	Reverse Transfer Capacitance		--	12	15	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 7.3\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	9	30	ns
t_r	Turn-On Rise Time		--	100	210	ns
$t_{d(off)}$	Turn-Off Delay Time		--	17	45	ns
t_f	Turn-Off Fall Time		--	50	110	ns
Q_g	Total Gate Charge	$V_{DS} = 80\text{ V}, I_D = 7.3\text{ A},$ $V_{GS} = 5\text{ V}$ (Note 4, 5)	--	4.6	6.0	nC
Q_{gs}	Gate-Source Charge		--	1.0	--	nC
Q_{gd}	Gate-Drain Charge		--	2.6	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	1.7	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	6.8	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.7\text{ A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 7.3\text{ A},$	--	70	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	140	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 26\text{ mH}, I_{AS} = 1.7\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 7.3\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

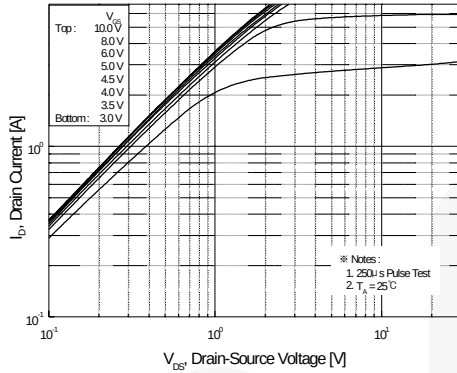


Figure 1. On-Region Characteristics

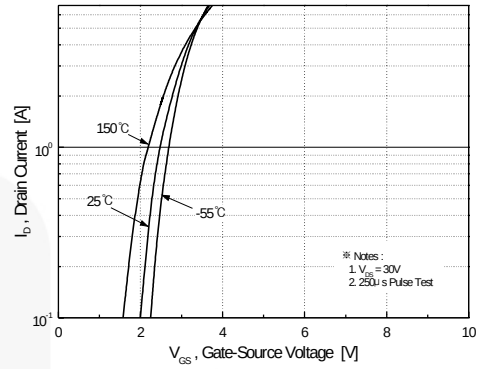


Figure 2. Transfer Characteristics

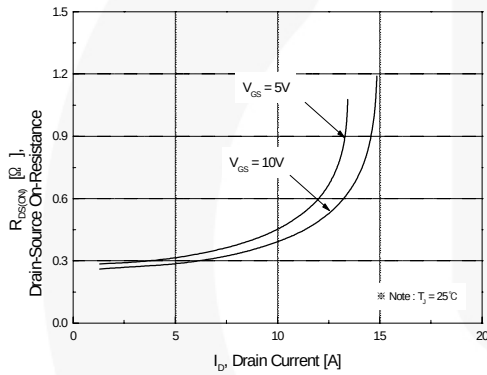


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

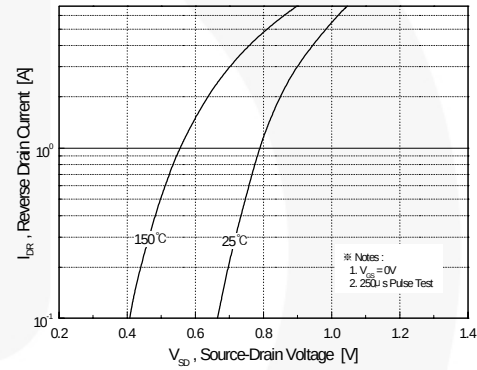


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

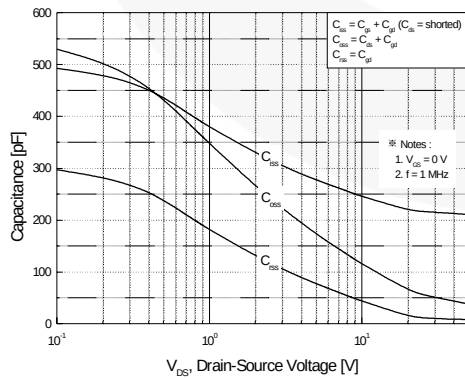


Figure 5. Capacitance Characteristics

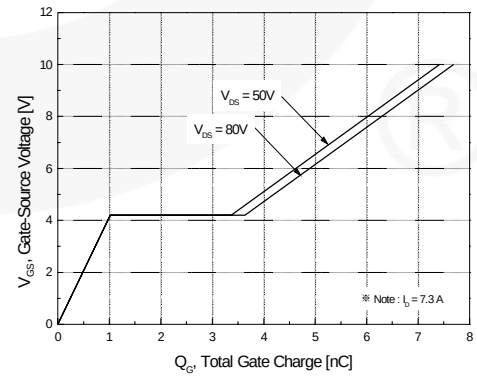


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

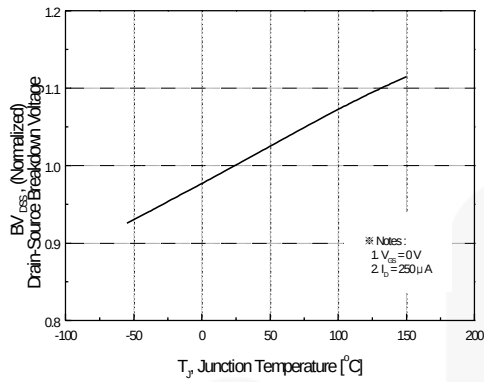


Figure 7. Breakdown Voltage Variation vs. Temperature

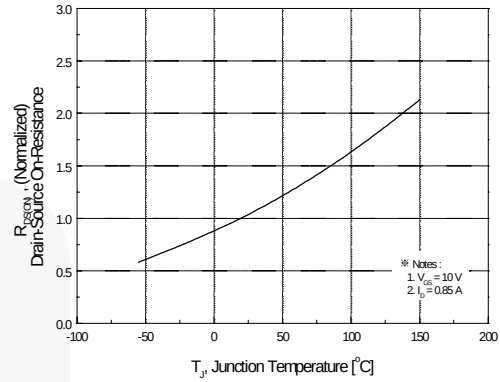


Figure 8. On-Resistance Variation vs. Temperature

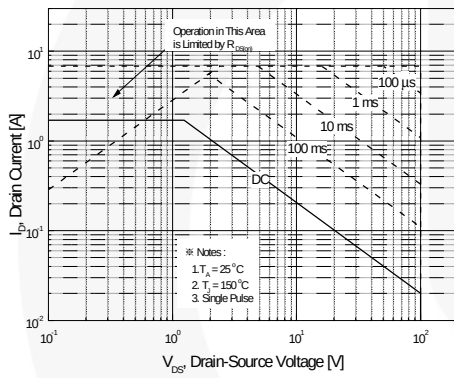


Figure 9. Maximum Safe Operating Area

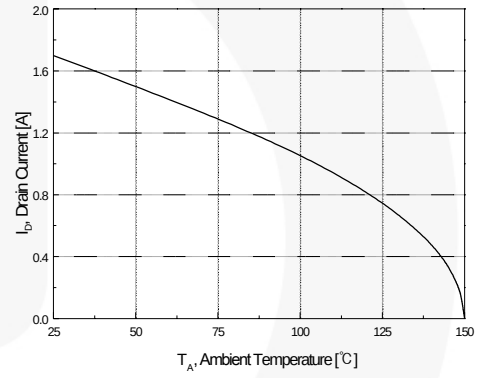


Figure 10. Maximum Drain Current vs. Ambient Temperature

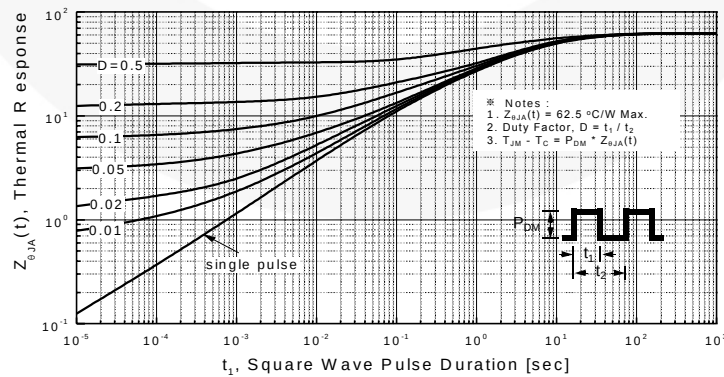
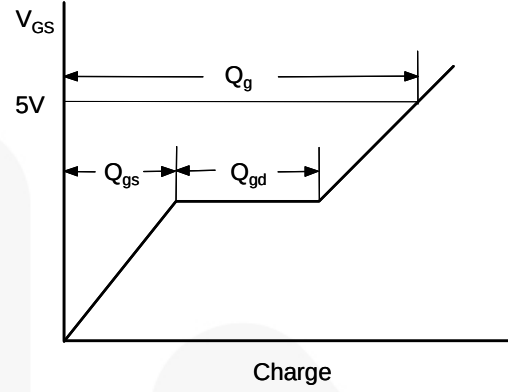
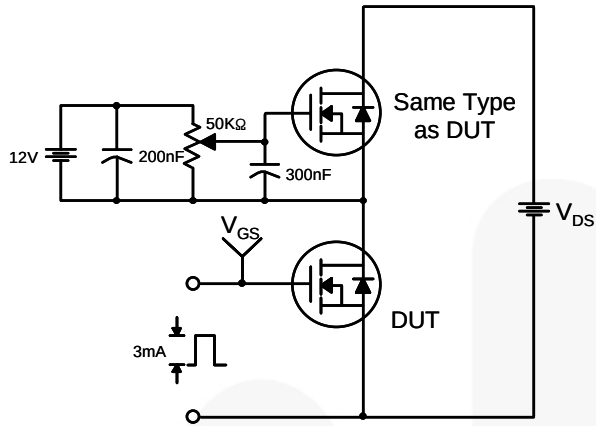
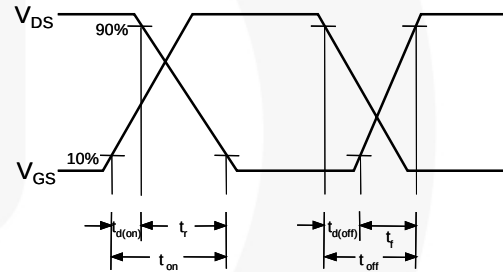
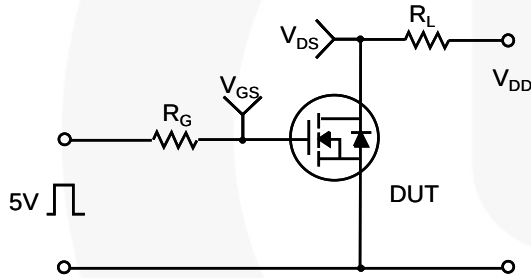


Figure 11. Transient Thermal Response Curve

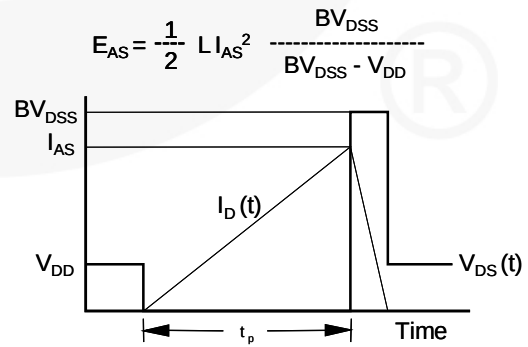
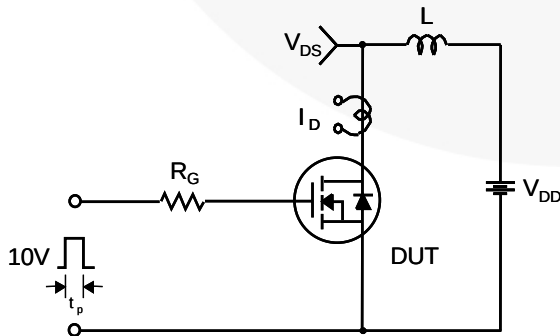
Gate Charge Test Circuit & Waveform



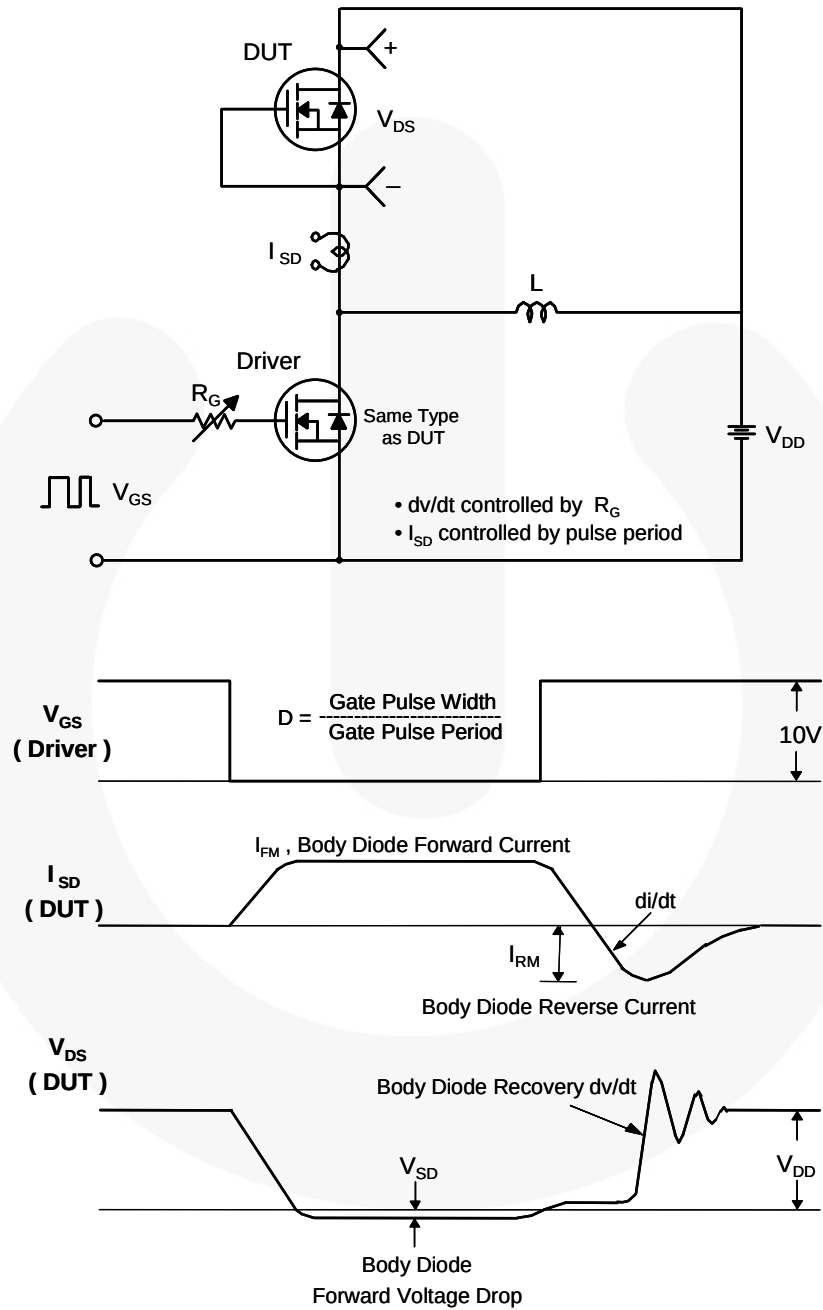
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms





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