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# FQB34P10TM\_F085

## 100V P-Channel MOSFET

March 2016  
QFET™

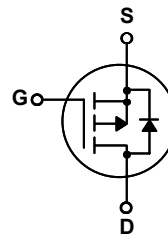
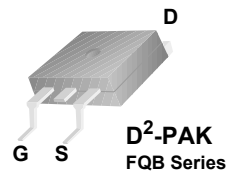
### General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

### Features

- -33.5A, -100V,  $R_{DS(on)} = 0.06\Omega$  @  $V_{GS} = -10V$
- Low gate charge ( typical 85 nC)
- Low  $C_{rss}$  ( typical 170 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating
- Qualified to AEC Q101
- RoHS Compliant



### Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	FQB34P10TM_F085	Units
$V_{DSS}$	Drain-Source Voltage	-100	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	-33.5	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	-23.5	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	-134	A
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	2200	mJ
$I_{AR}$	Avalanche Current (Note 1)	-33.5	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	15.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-6.0	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	3.75	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	155	W
	- Derate above $25^\circ\text{C}$	1.03	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.97	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C/W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

FQB34P10TM\_F085 100V P-Channel MOSFET

**Electrical Characteristics** $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-100	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	-0.1	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -80\text{ V}, T_C = 150^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -16.75\text{ A}$	--	0.049	0.06	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -16.75\text{ A}$ (Note 4)	--	23	--	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2240	2910	pF
$C_{oss}$	Output Capacitance		--	730	950	pF
$C_{rss}$	Reverse Transfer Capacitance		--	170	220	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -50\text{ V}, I_D = -33.5\text{ A},$ $R_G = 25\text{ }\Omega$  (Note 4, 5)	--	25	60	ns
$t_r$	Turn-On Rise Time		--	250	510	ns
$t_{d(off)}$	Turn-Off Delay Time		--	160	330	ns
$t_f$	Turn-Off Fall Time		--	210	430	ns
$Q_g$	Total Gate Charge	$V_{DS} = -80\text{ V}, I_D = -33.5\text{ A},$ $V_{GS} = -10\text{ V}$  (Note 4, 5)	--	85	110	nC
$Q_{gs}$	Gate-Source Charge		--	15	--	nC
$Q_{gd}$	Gate-Drain Charge		--	45	--	nC

**Drain-Source Diode Characteristics and Maximum Ratings**

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	-33.5	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-134	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -33.5 A	--	--	-4.0	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -33.5 A, dI <sub>F</sub> / dt = 100 A/μs (Note 4)	--	160	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.88	--	μC

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 3.9\text{ mH}, I_{AS} = -33.5\text{ A}, V_{DD} = -25\text{ V}, R_G = 25\text{ }\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq -33.5\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

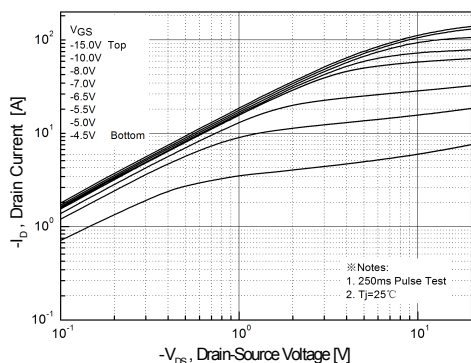


Figure 1. On-Region Characteristics

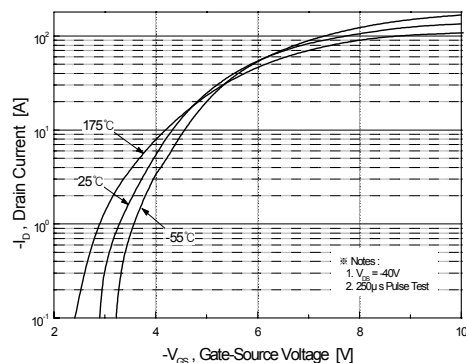


Figure 2. Transfer Characteristics

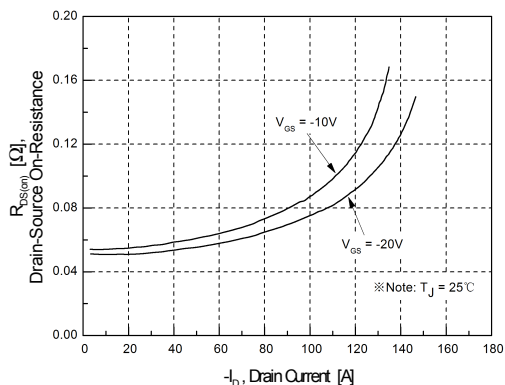


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

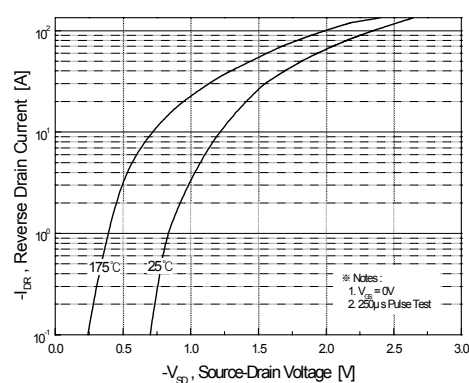


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

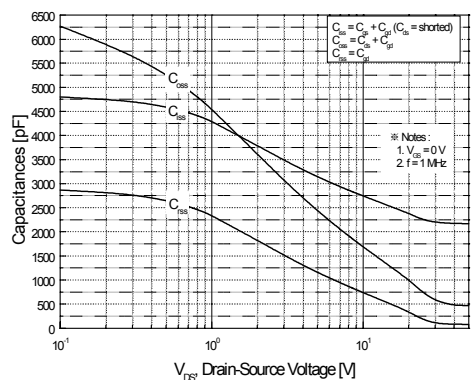


Figure 5. Capacitance Characteristics

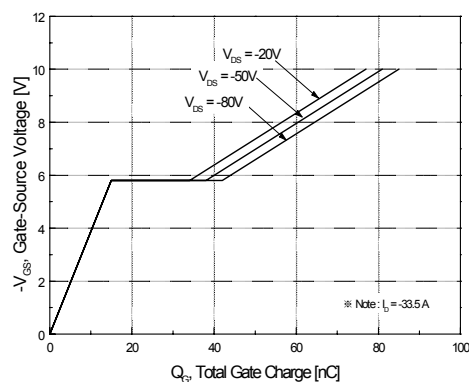
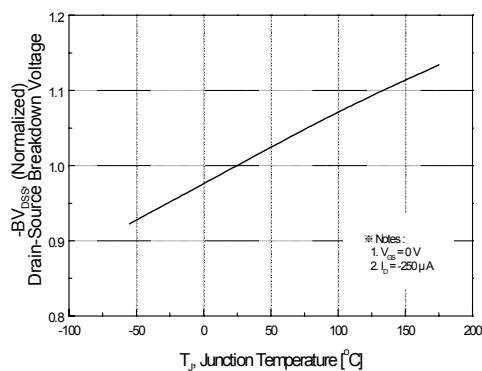
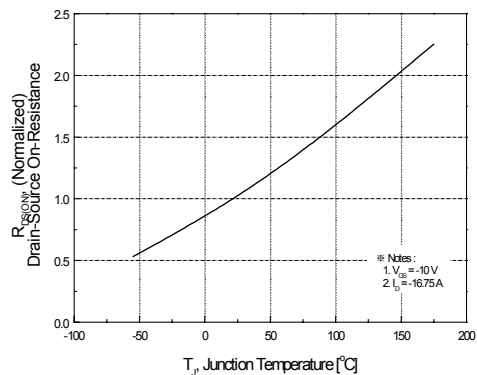


Figure 6. Gate Charge Characteristics

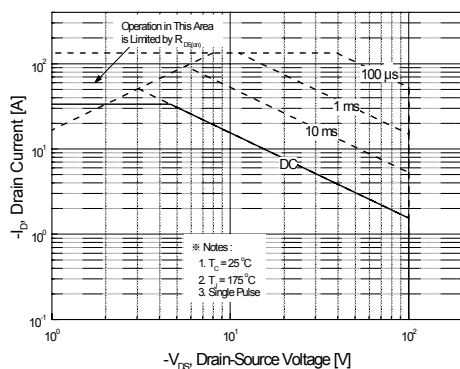
## Typical Characteristics (Continued)



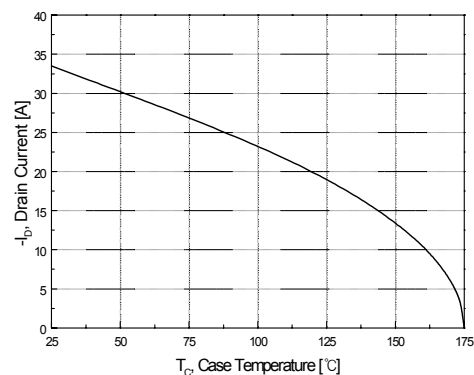
**Figure 7. Breakdown Voltage Variation vs. Temperature**



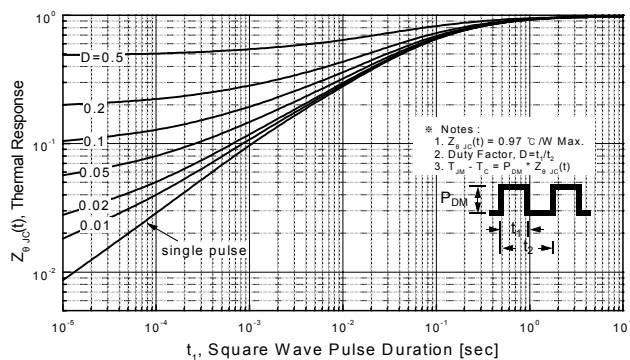
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

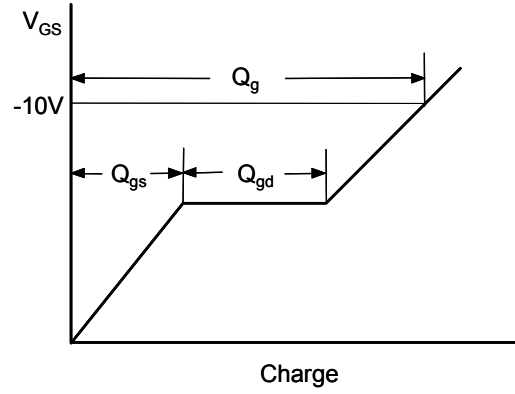
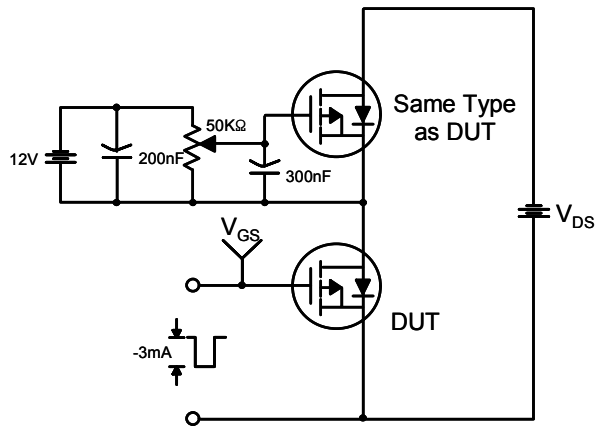


**Figure 10. Maximum Drain Current vs. Case Temperature**

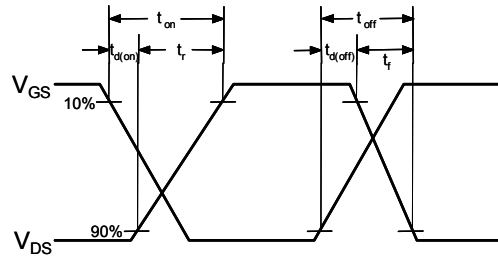
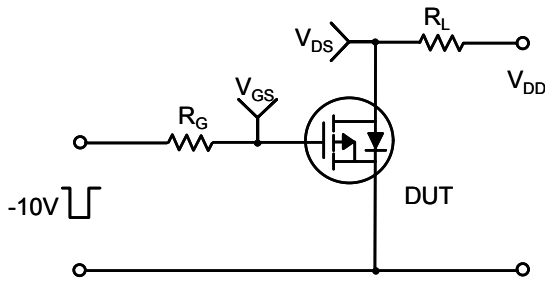


**Figure 11. Transient Thermal Response Curve**

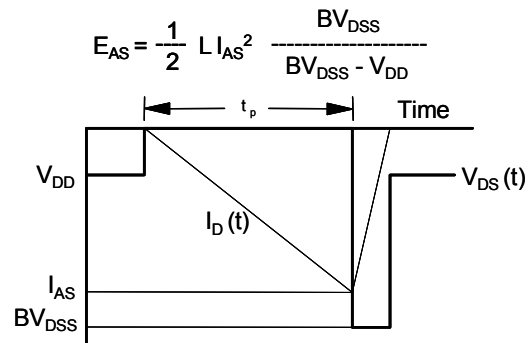
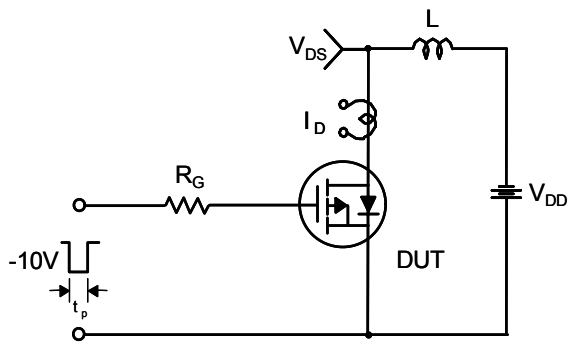
### Gate Charge Test Circuit & Waveform



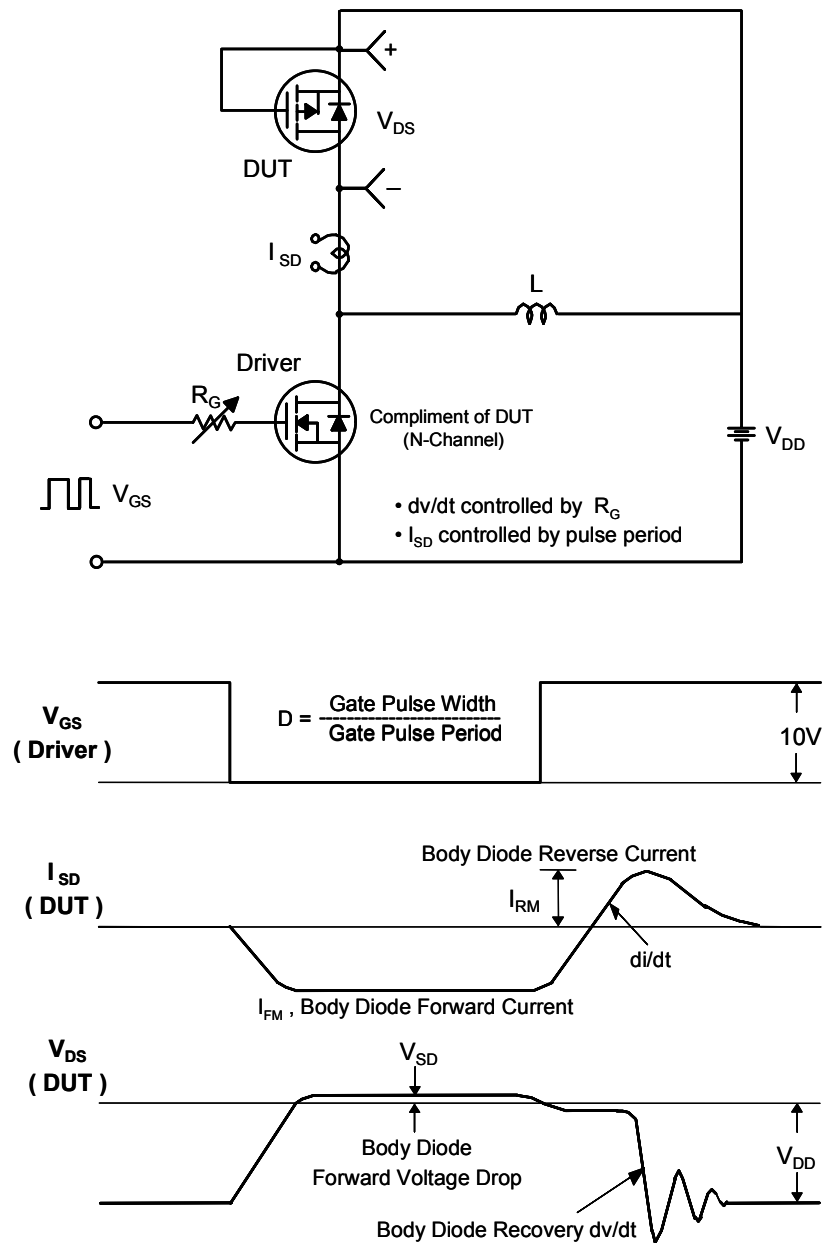
### Resistive Switching Test Circuit & Waveforms

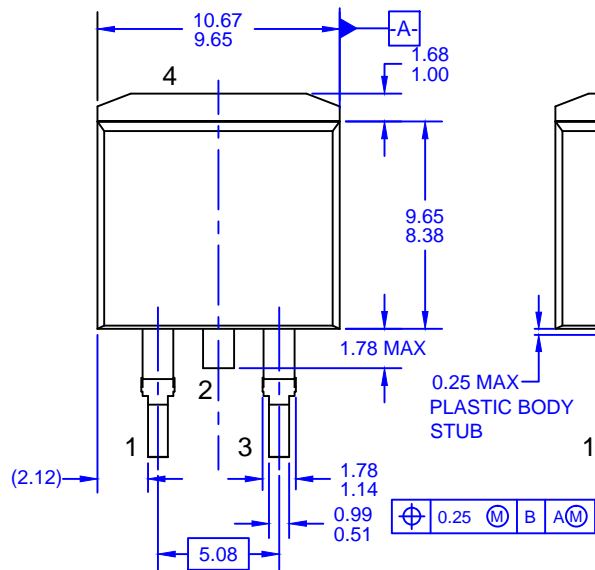


### Unclamped Inductive Switching Test Circuit & Waveforms

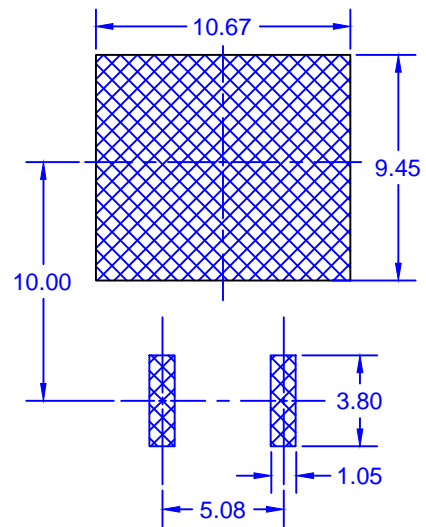


Peak Diode Recovery dv/dt Test Circuit & Waveforms

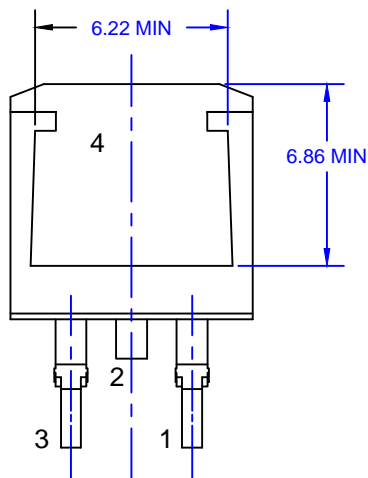




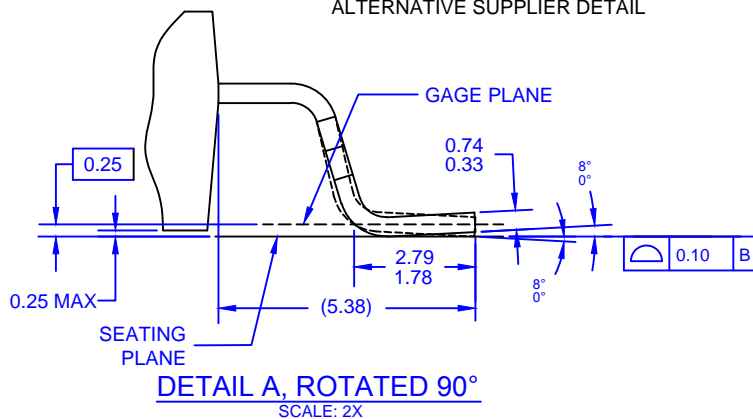
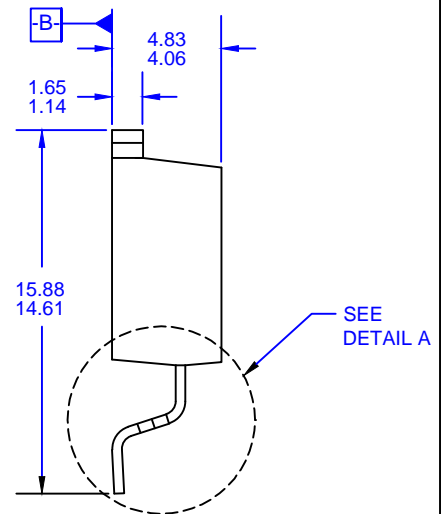
FRONT VIEW - DIODE PRODUCTS VERSION  
ALTERNATIVE SUPPLIER DETAIL



LAND PATTERN RECOMMENDATION  
UNLESS NOTED, ALL DIMS TYPICAL



BACK VIEW - DIODE PRODUCTS VERSION  
ALTERNATIVE SUPPLIER DETAIL



DETAIL A, ROTATED 90°  
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) REFERENCE JEDEC, TO-263, VARIATION AB.
- C) DIMENSIONING AND TOLERANCING PER DIMENSIONING AND TOLERANCING PER ASME Y14.5 - 2009.
- D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
- E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
- F) FILENAME: TO263A02REV8





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