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October 2015

FJN4301R

PNP Epitaxial Silicon Transistor with Bias Resistor

Features

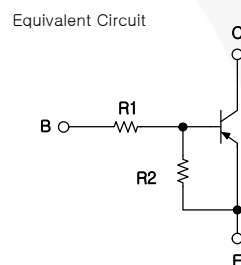
- 100 mA Output Current Capability
- Built-in Bias Resistor ($R_1 = 4.7 \text{ k}\Omega$, $R_2 = 4.7 \text{ k}\Omega$)

Applications

- Switching, Interface, and Driver Circuits
- Inverters
- Digital Applications in Industrial Segments

Description

Transistors with built-in resistors can be excellent space- and cost-saving solutions by reducing component count and simplifying circuit design.



Ordering Information

| Part Number | Top Mark | Package | Packing Method |
|-------------|----------|----------|----------------|
| FJN4301RTA | R4301 | TO-92 3L | Ammo |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Value | Unit |
|-----------|---------------------------|------------|------------------|
| V_{CBO} | Collector-Base Voltage | -50 | V |
| V_{CEO} | Collector-Emitter Voltage | -50 | V |
| V_{EBO} | Emitter-Base Voltage | -10 | V |
| I_C | Collector Current | -100 | mA |
| T_J | Junction Temperature | 150 | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature | -55 to 150 | $^\circ\text{C}$ |

Thermal Characteristics⁽¹⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Value | Unit |
|-----------------|---|-------|----------------------|
| P_D | Power Dissipation | 300 | mW |
| | Derate Above $T_A = 25^\circ\text{C}$ | 2.4 | mW/ $^\circ\text{C}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 416 | $^\circ\text{C/W}$ |

Note:

1. PCB size: FR-4 76 x 114 x 0.6T mm³ (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------|--------------------------------------|---|------|------|------|---------------|
| BV_{CBO} | Collector-Base Breakdown Voltage | $I_C = -10\ \mu\text{A}$, $I_E = 0$ | -50 | | | V |
| BV_{CEO} | Collector-Emitter Breakdown Voltage | $I_C = -100\ \mu\text{A}$, $I_B = 0$ | -50 | | | V |
| I_{CBO} | Collector Cut-Off Current | $V_{CB} = -40\ \text{V}$, $I_E = 0$ | | | -0.1 | μA |
| h_{FE} | DC Current Gain | $V_{CE} = -5\ \text{V}$, $I_C = -10\ \text{mA}$ | 20 | | | |
| $V_{CE(sat)}$ | Collector-Emitter Saturation Voltage | $I_C = -10\ \text{mA}$, $I_B = -0.5\ \text{mA}$ | | | -0.3 | V |
| f_T | Current Gain Bandwidth Product | $V_{CE} = -10\ \text{V}$, $I_C = -5\ \text{mA}$ | | 200 | | MHz |
| C_{ob} | Output Capacitance | $V_{CB} = -10\ \text{V}$, $I_E = 0$, $f = 1.0\ \text{MHz}$ | | 5.5 | | pF |
| $V_I(\text{off})$ | Input-Off Voltage | $V_{CE} = -5\ \text{V}$, $I_C = -100\ \mu\text{A}$ | | | -0.5 | V |
| $V_I(\text{on})$ | Input-On Voltage | $V_{CE} = -0.3\ \text{V}$, $I_C = -20\ \text{mA}$ | -3 | | | V |
| R_1 | Input Resistor | | 3.2 | 4.7 | 6.2 | k Ω |
| R_1/R_2 | Resistor Ratio | | 0.9 | 1.0 | 1.1 | |

Typical Performance Characteristics

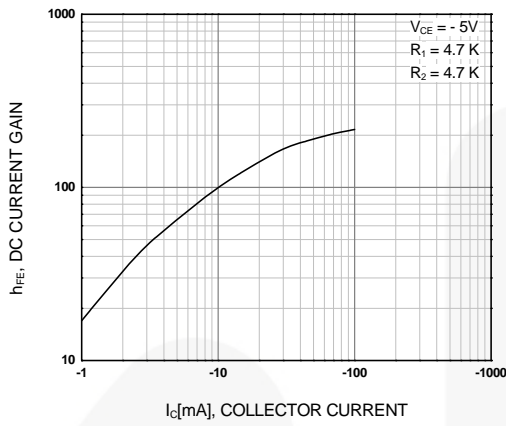


Figure 1. DC Current Gain

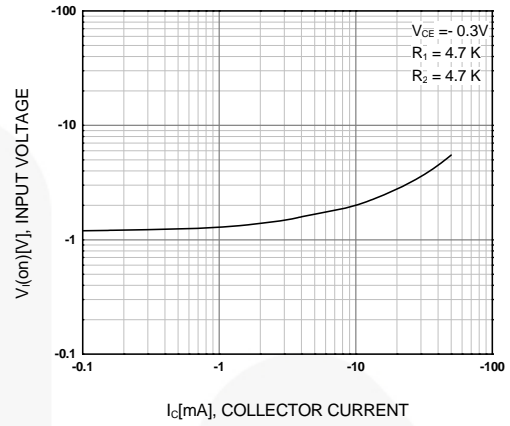


Figure 2. Input-On Voltage

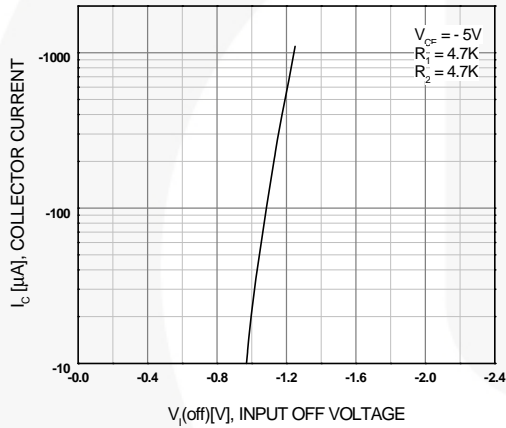


Figure 3. Input-Off Voltage

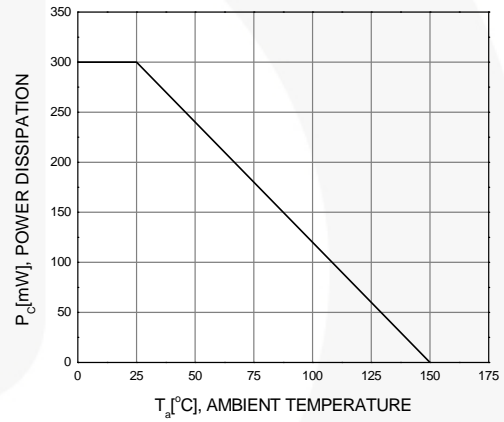
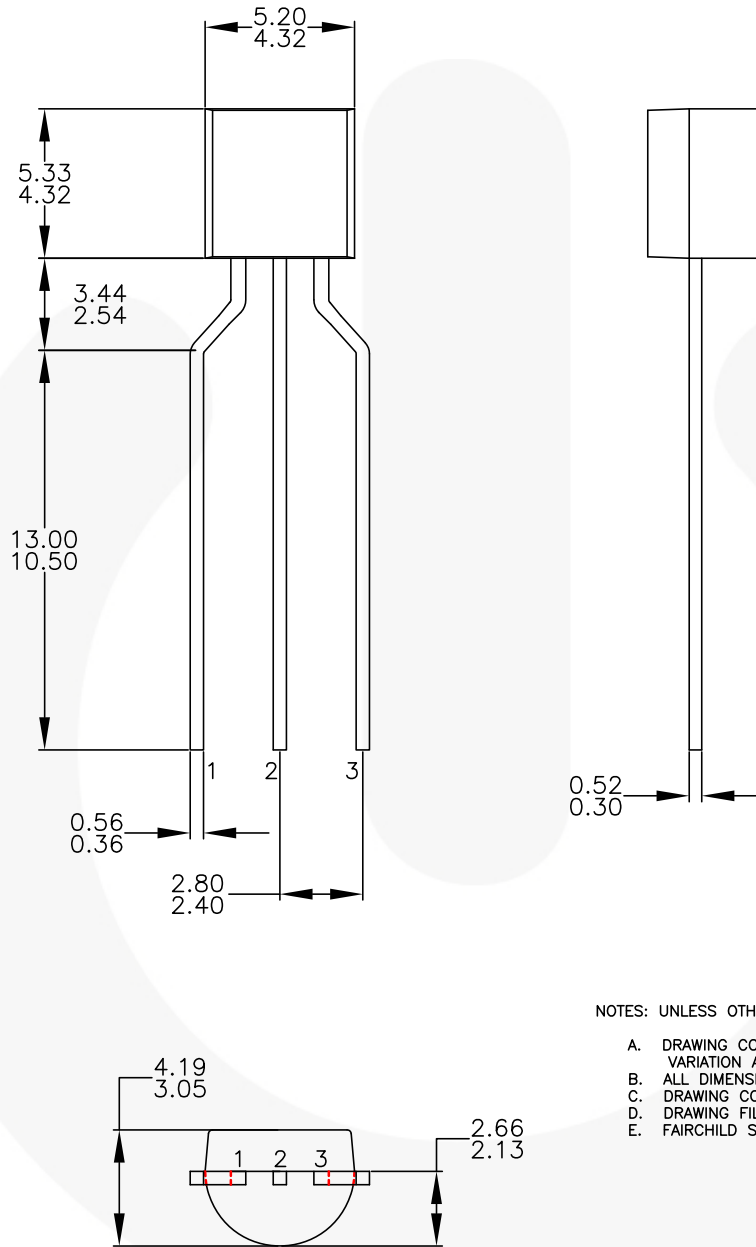


Figure 4. Power Derating

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREV3.
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Figure 5. 3-LEAD, TO-92, MOLDED 0.200 IN-LINE SPACING LD FORM



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