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February 2017

FDS4675_F085
40V P-Channel PowerTrench® MOSFET

General Description

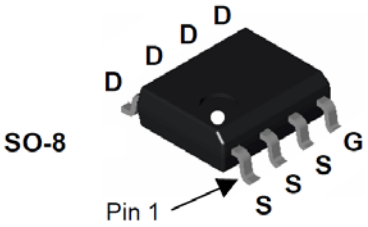
This P-Channel MOSFET is a rugged gate version of On Semiconductor's advanced PowerTranch process. It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5 V – 20 V).

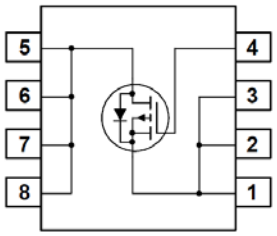
Applications

- Power management
- Load switch
- Battery protection

Features

- -11 A, -40 V $R_{DS(ON)}$ = 0.013 Ω @ V_{GS} = -10 V
  $R_{DS(ON)}$ = 0.017 Ω @ V_{GS} = -4.5 V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- Qualified to AEC Q101
- RoHS Compliant





Absolute Maximum Ratings T_A = 25℃ unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		-40	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current	Continuous	-11 (Note 1a)	A
		Pulsed	-50	A
P_D	Power Dissipation for Single Operation		2.4 (steady state) (Note 1a)	W
			1.4 (Note 1b)	W
			1.2 (Note 1c)	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	℃

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5 (steady state), 50 (10 sec) (Note 1a)	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125 (Note 1c)	℃/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	25 (Note 1)	℃/W

Package Marking and Ordering Information

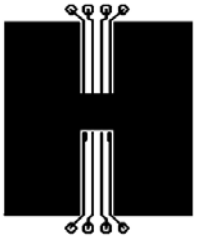
Device Marking	Device	Reel Size	Tape width	Quantity
FDS4675	FDS4675_F085	**13”**	12mm	2500 units

Electrical Characteristics T_A = 25℃ unless otherwise noted

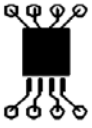
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25℃		-34		mV/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -32 V, V_{GS} = 0 V			-1	μA
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.4	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = -250μA, Referenced to 25℃		4.6		mV/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -11 A		10	13	mΩ
		V_{GS} = -4.5 V, I_D = -9.5 A		13	17	
		V_{GS} = -10 V, I_D = -11 A, T_J = 125℃		15	21	
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -11 A		44		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = -20 V, V_{GS} = 0 V, f = 1 MHz		4350		pF
C_{OSS}	Output Capacitance			622		pF
C_{RSS}	Reverse Transfer Capacitance			290		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -20 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		40	64	ns
t_r	Turn-On Rise Time			49	79	ns
$t_{d(off)}$	Turn-Off Delay Time			100	160	ns
t_f	Turn-Off Fall Time			60	96	ns
Q_g	Total Gate Charge	V_{DS} = -20 V, I_D = -11 A, V_{GS} = -4.5 V		40	56	nC
Q_{gs}	Gate-Source Charge			11		nC
Q_{gd}	Gate-Drain Charge			13		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 A, I_S = -2.1 A (Note 2)		-0.7	-1.2	V

Notes:

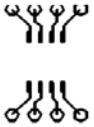
1. $R_{\theta JA}$ is the sum of the junction to case and case to ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1in² pad of 2 oz copper



b) 105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

Typical Characteristics

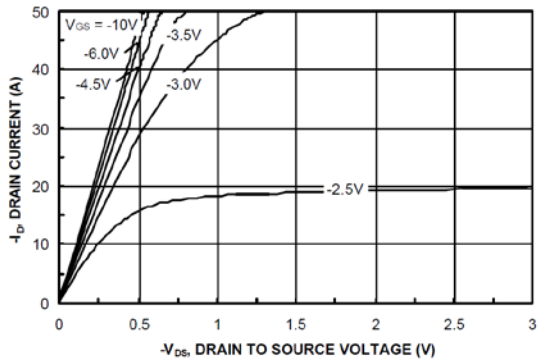


Figure 1. On-Region Characteristics

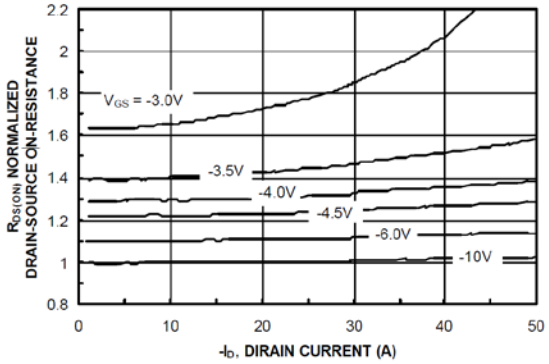


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

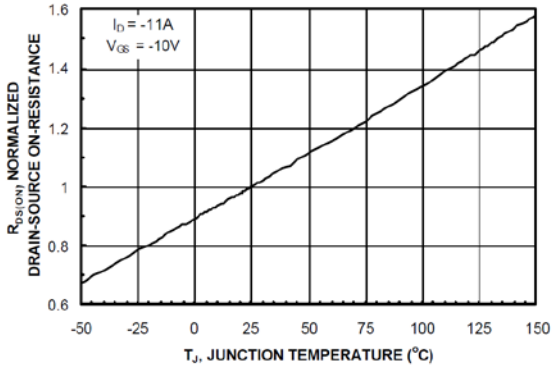


Figure 3. On-Resistance Variation with Temperature

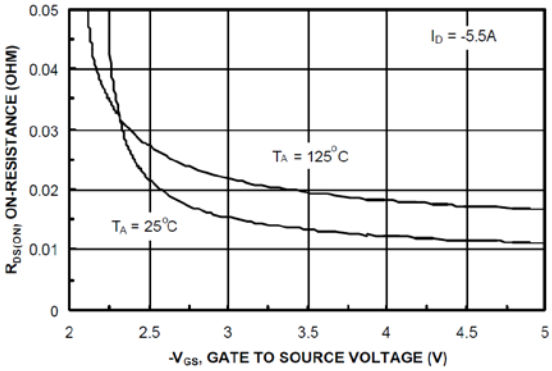


Figure 4. On-Resistance Variation with Gate to Source Voltage

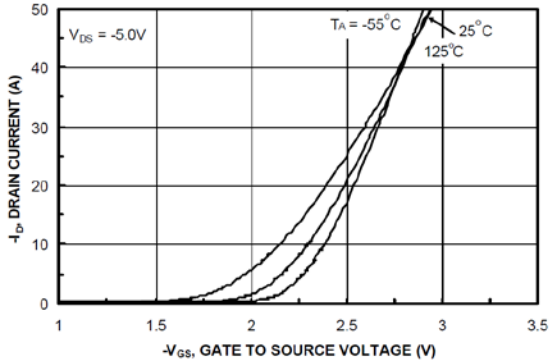


Figure 5. Transfer Characteristics

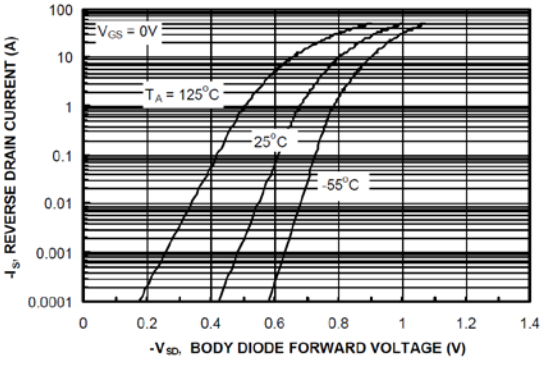


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

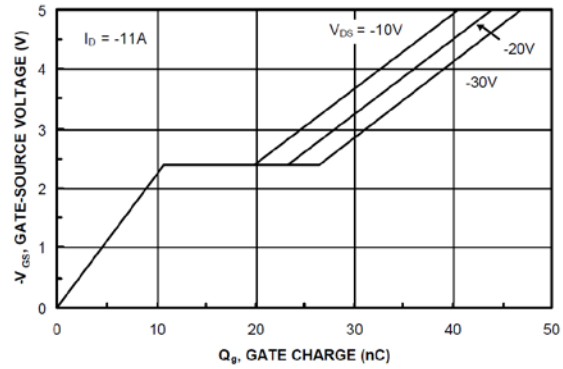


Figure 7. Gate Charge Characteristics

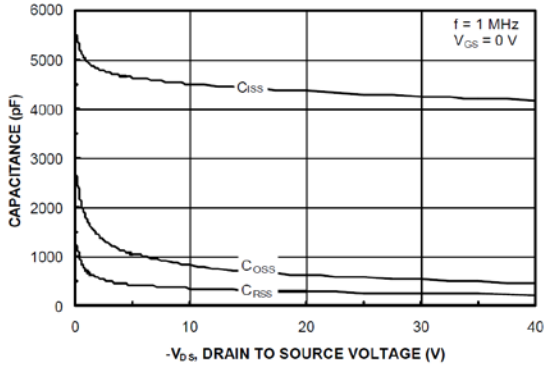


Figure 8. Capacitance Characteristics

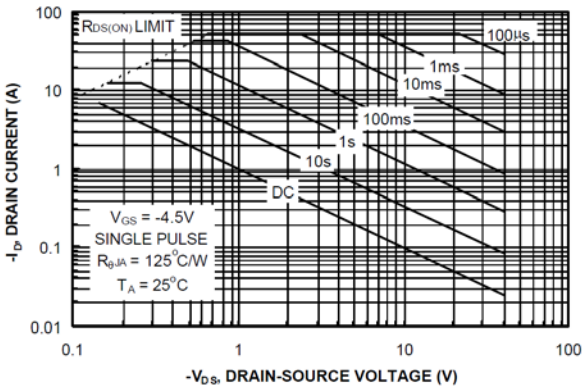


Figure 9. Maximum Safe Operating Area

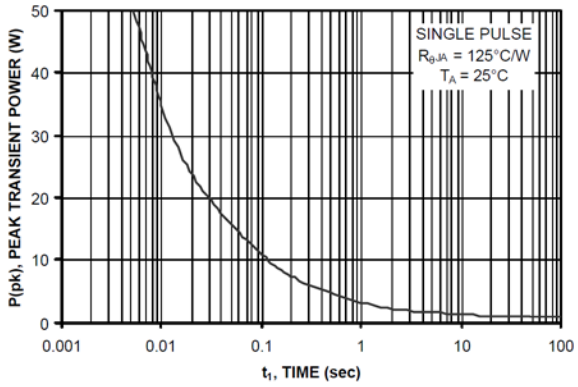


Figure 10. Single Pulse Maximum Power Dissipation

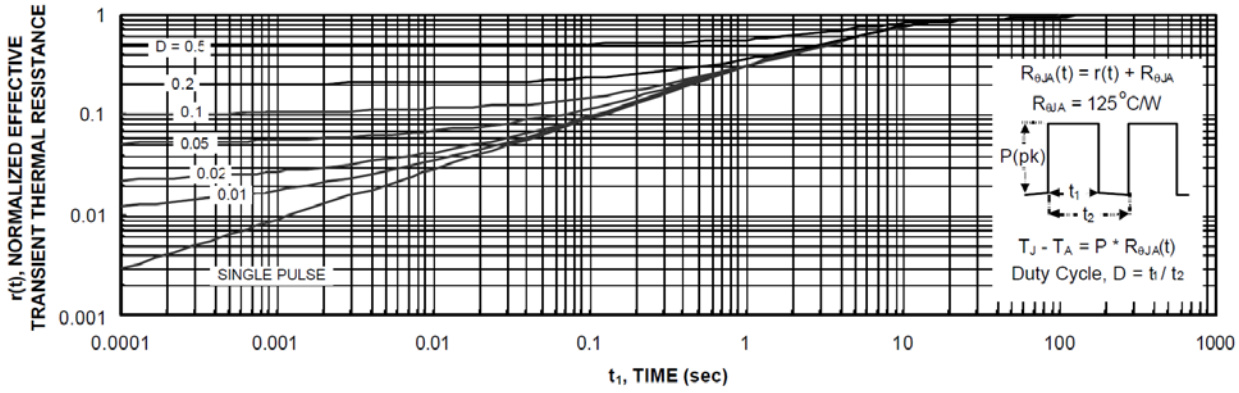
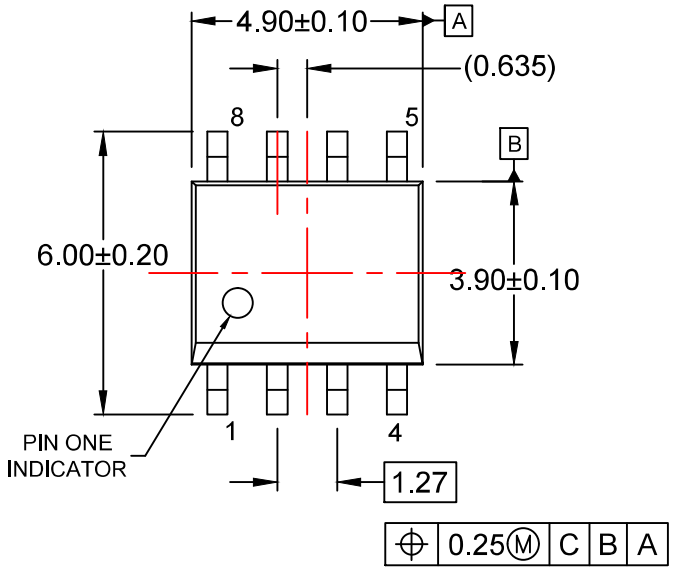
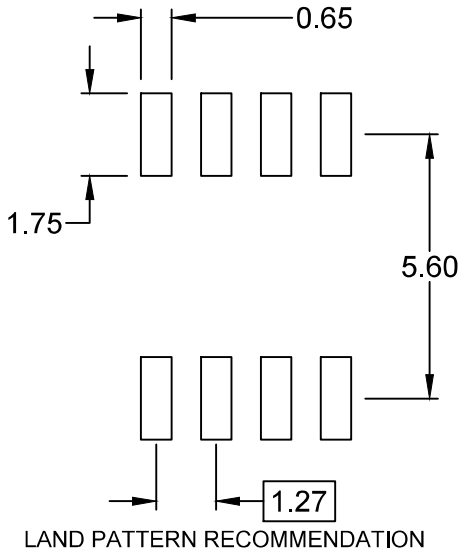


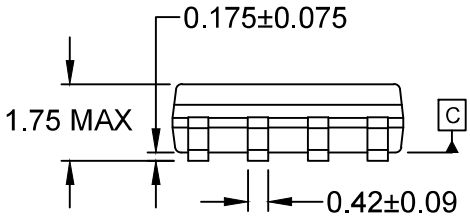
Figure 11. Transient Thermal Response Curve

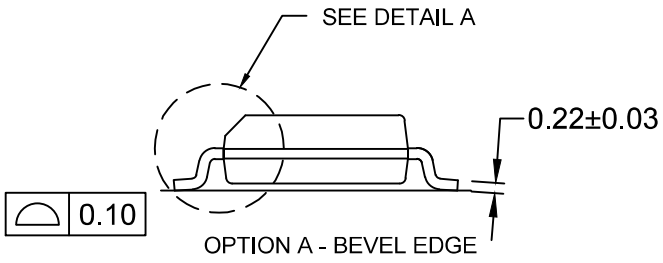
Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.



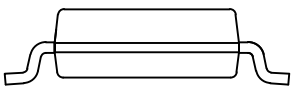


LAND PATTERN RECOMMENDATION

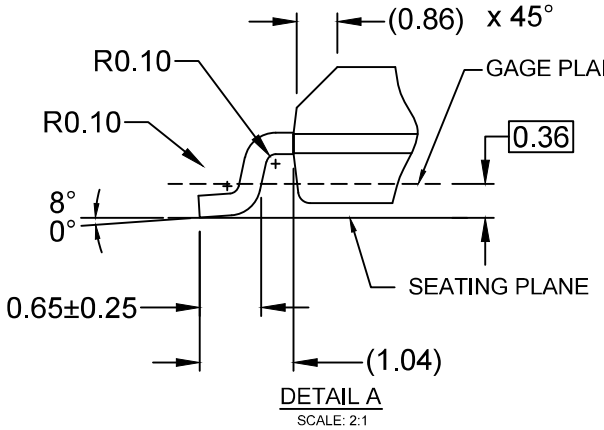




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

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