MOSFET - Power, Single N-Channel
40 V, 1.1 mΩ, 240 A

FDBL9406L-F085

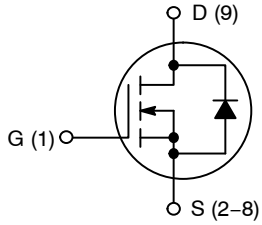
ON Semiconductor®

www.onsemi.com

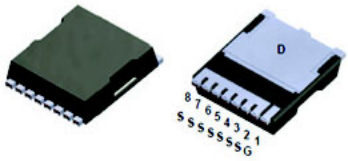
Features

- Small Footprint (TOLL) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	1.1 mΩ @ 10 V	80 A
	1.78 mΩ @ 4.5 V	



N−CHANNEL MOSFET



MO−299A
CASE 100CU

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	240	A
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	P_D	300	W
	Steady State	T_C = 100°C		150	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	43	A
	Steady State	T_A = 100°C		31	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	P_D	3.5	W
	Steady State	T_A = 100°C		1.7	
Pulsed Drain Current	T_C = 25°C, t_p = 10 μs		I_{DM}	2755	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	100	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 85 A; L = 60 μH)			E_{AS}	217	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

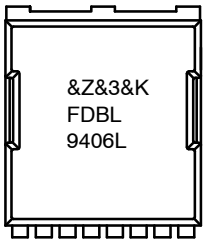
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{\theta JC}$	0.5	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	43	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Current is limited by bondwire configuration.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDBL9406L	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	40	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$		–	19.3	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V, T_J = 25°C	–	–	1	μA
		V_{GS} = 0 V, V_{DS} = 40 V, T_J = 175°C	–	–	1	mA
Zero Gate Voltage Drain Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	–	–	±100	nA
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 μA	1	1.9	3	V
Threshold Temperature Coefficient	$V_{GS(th)}/T_J$		–	−6.5	–	mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 80 A	–	0.9	1.1	mΩ
		V_{GS} = 4.5 V, I_D = 40 A	–	1.25	1.78	
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 20 V	–	8600	–	pF
Output Capacitance	C_{oss}		–	2380	–	pF
Reverse Transfer Capacitance	C_{rss}		–	106	–	pF
Gate Resistance	R_g	V_{GS} = 0.5 V, f = 1 MHz	–	2	–	Ω
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 32 V, I_D = 80 A	–	58	–	nC
		V_{GS} = 10 V, V_{DS} = 32 V, I_D = 80 A	–	121	–	
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to 1 V	–	7	–	
Gate−to−Source Gate Charge	Q_{gs}	V_{DD} = 32 V, I_D = 80 A	–	26	–	
Gate−to−Drain “Miller” Charge	Q_{gd}		–	19	–	
Plateau Voltage	V_{GP}		–	3.2	–	V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	22	–	ns
Turn-On Rise Time	t_r		–	22	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	134	–	ns
Turn-Off Fall Time	t_f		–	44	–	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
Source−to−Drain Diode Voltage	V_{SD}	I_{SD} = 80 A, V_{GS} = 0 V	–	0.81	1.25	V
		I_{SD} = 40 A, V_{GS} = 0 V	–	0.77	1.2	V
Reverse Recovery Time	T_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/μs, I_S = 80 A	–	77	–	ns
Charge Time	t_a		–	38	–	
Discharge Time	t_b		–	39	–	
Reverse Recovery Charge	Q_{RR}		–	95	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

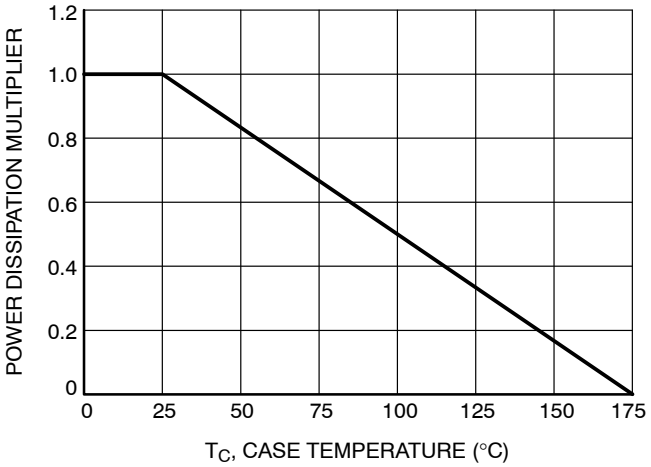


Figure 1. Normalized Power Dissipation vs. Case Temperature

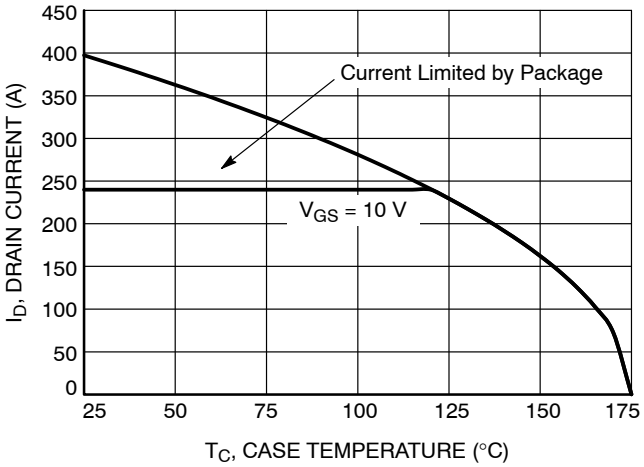


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

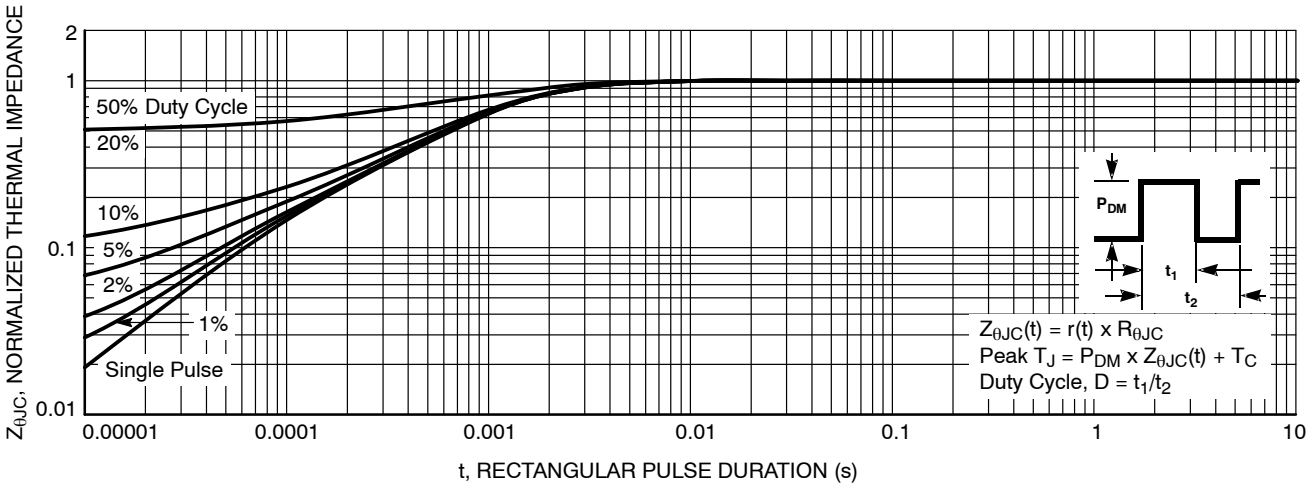


Figure 3. Normalized Maximum Transient Thermal Impedance

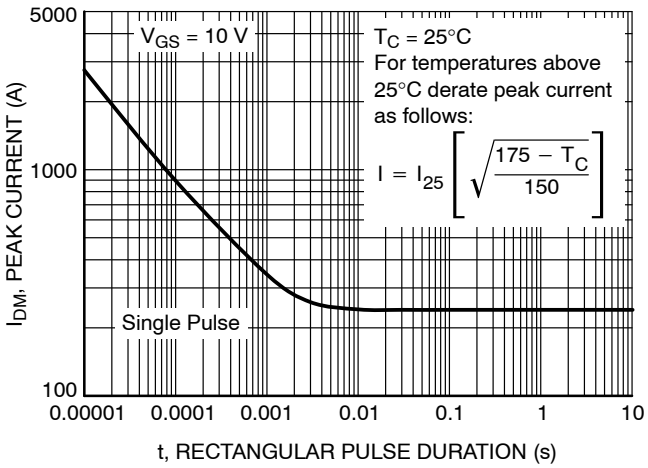


Figure 4. Peak Current Capability

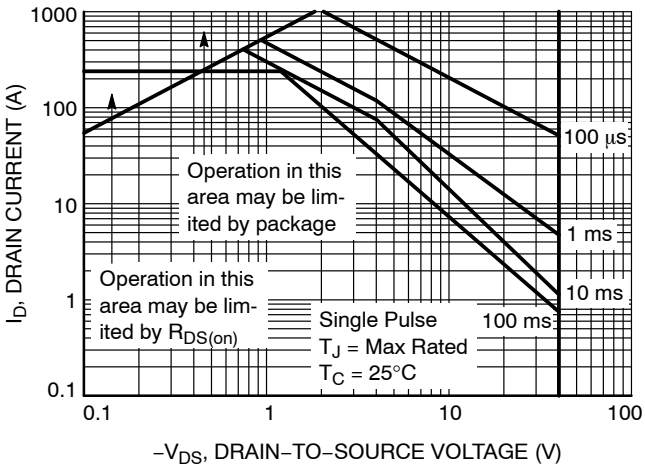


Figure 5. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS

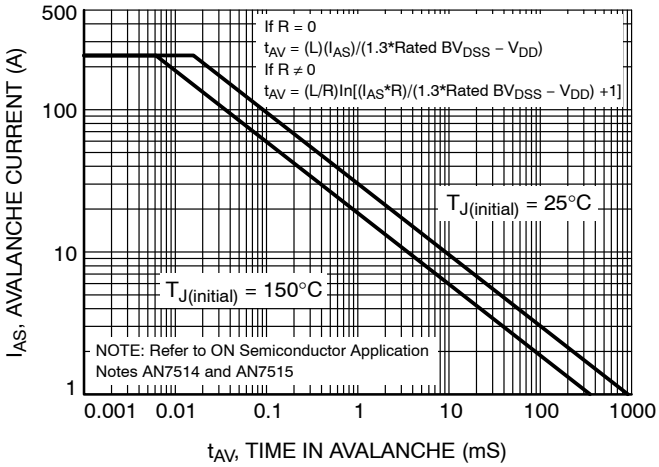


Figure 6. Unclamped Inductive Switching Capability

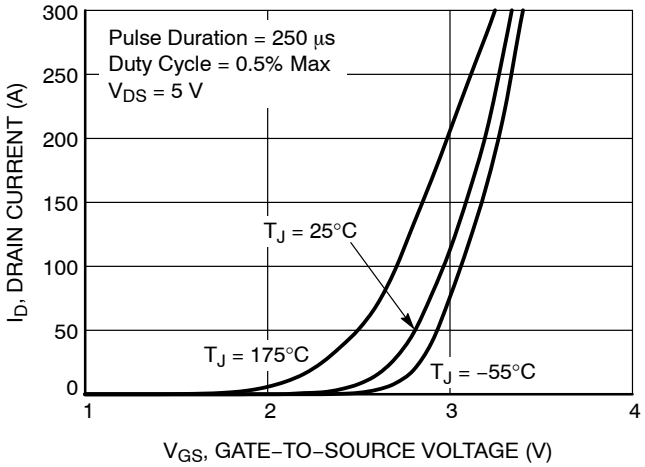


Figure 7. Transfer Characteristics

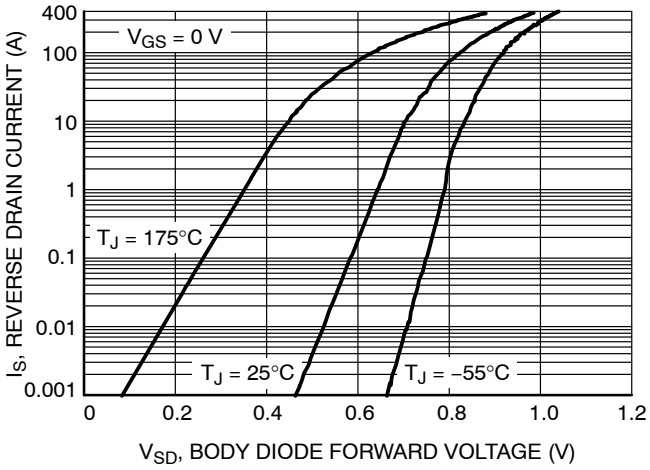


Figure 8. Forward Diode Characteristics

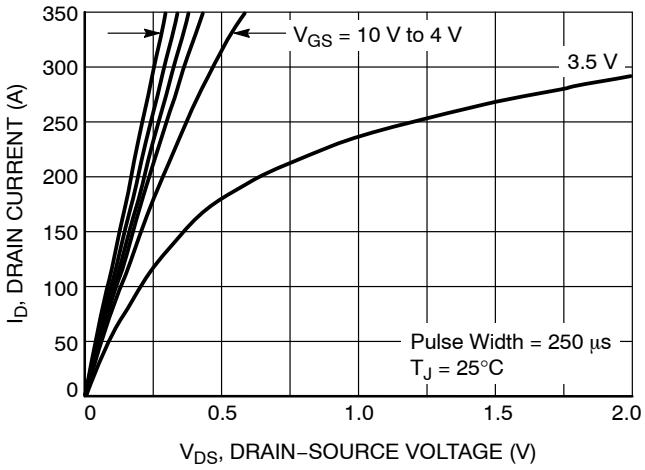


Figure 9. Saturation Characteristics

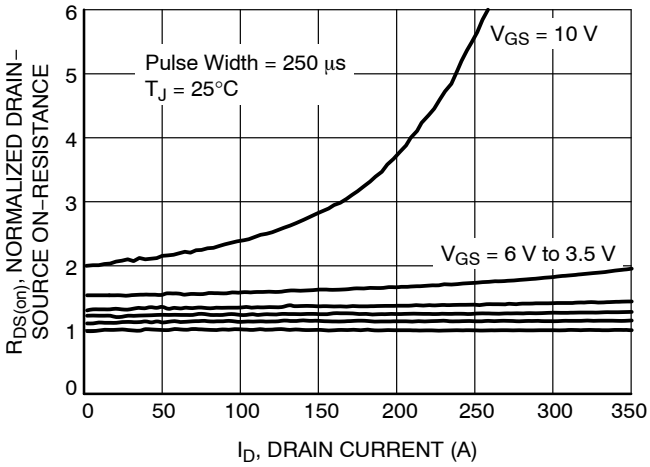


Figure 10. Normalized $R_{DS(on)}$ vs. Drain Current

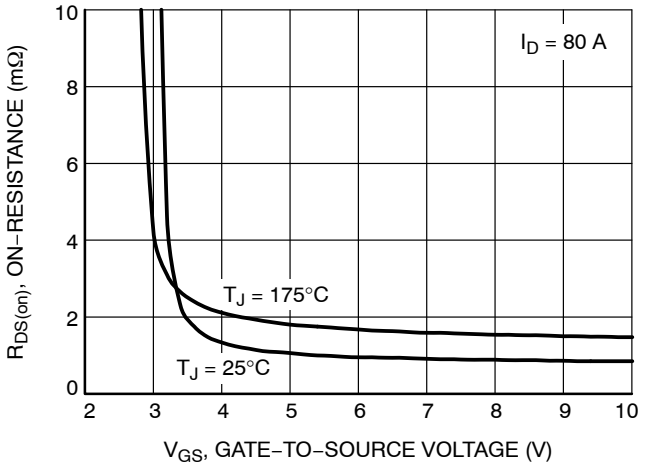


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

TYPICAL CHARACTERISTICS

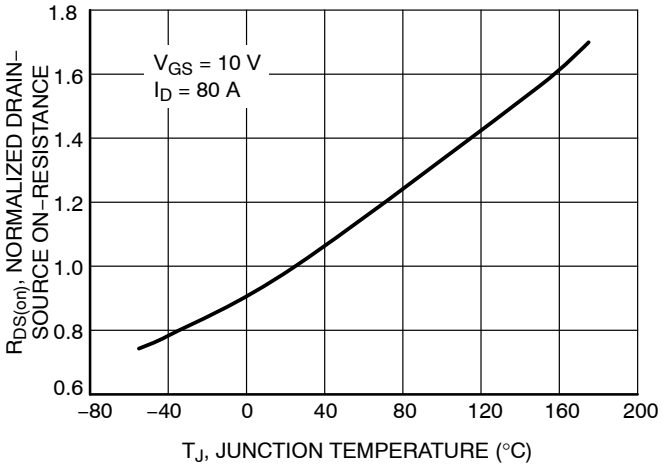


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

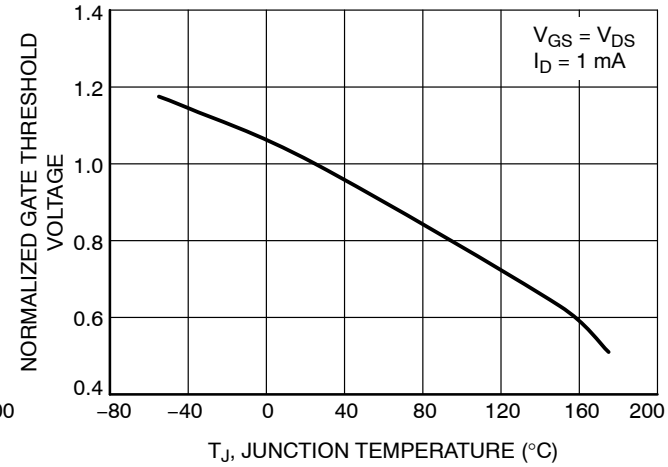


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

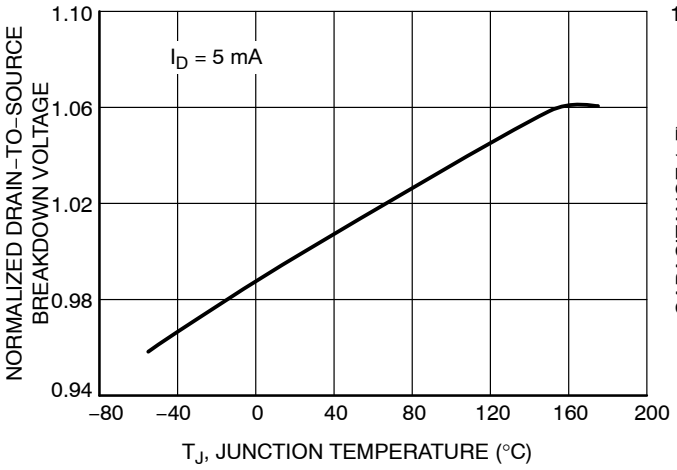


Figure 14. Normalized Drain−to−Source Breakdown Voltage vs. Junction Temperature

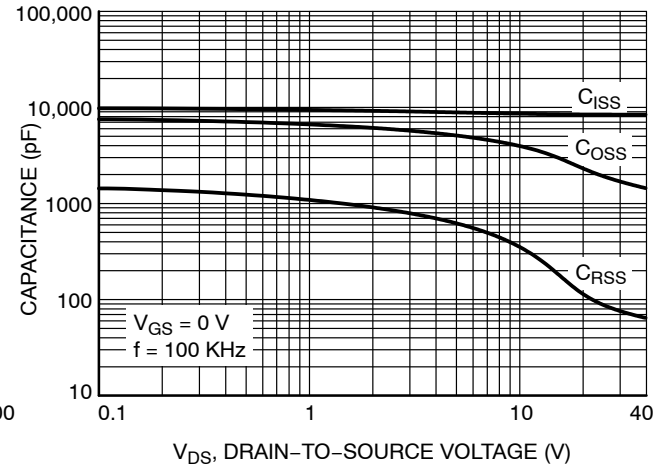


Figure 15. Capacitance vs. Drain−to−Source Voltage

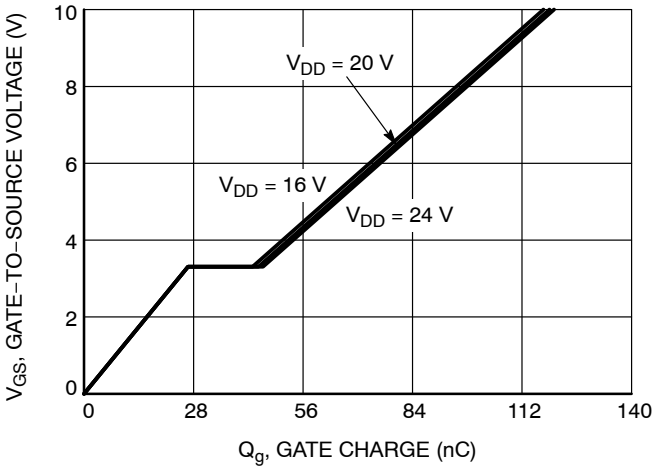
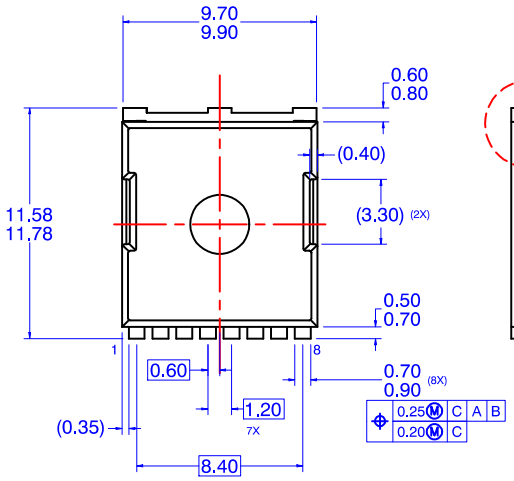


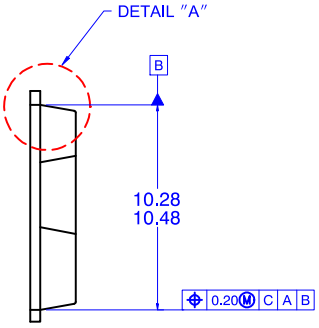
Figure 16. Gate Charge vs. Gate−to−Source Voltage

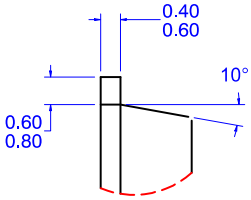
PACKAGE DIMENSIONS

H−PSOF8L 11.68x9.80
CASE 100CU
ISSUE O

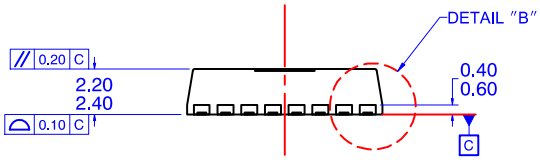


TOP VIEW

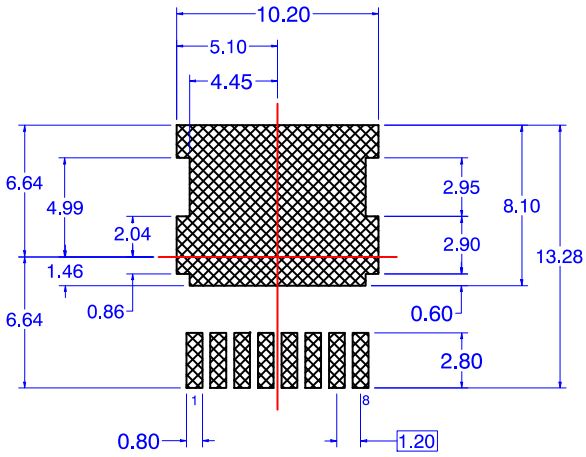




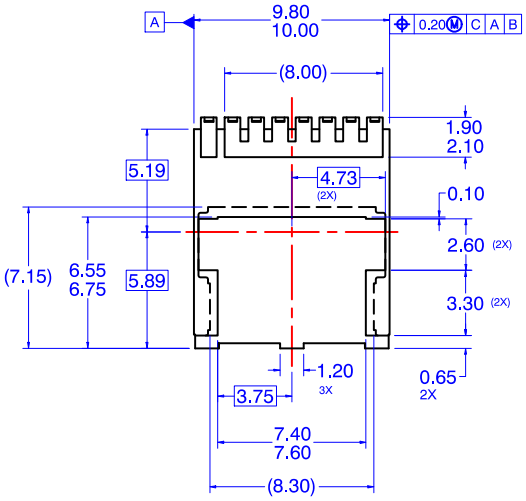
DETAIL "A"



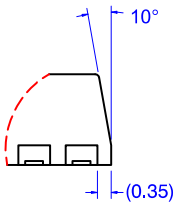
SIDE VIEW



LAND PATTERN
RECOMMENDATION



BOTTOM VIEW



DETAIL "B"

NOTES: UNLESS OTHERWISE SPECIFIED
A) PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A, DATED NOVEMBER 2009.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Quantity
FDBL9406L−F085	FDBL9406L	H−PSOF8L (Pb-Free / Halogen Free)	13″	24 mm	2000 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

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