

# **MOSFET – N-Channel, POWERTRENCH®**

**60 V, 80 A, 5.6 mΩ**

## **FDB86569-F085**

### **Features**

- Typical  $R_{DS(on)}$  = 4.4 mΩ at  $V_{GS} = 10$  V,  $I_D = 80$  A
- Typical  $Q_{g(tot)}$  = 35 nC at  $V_{GS} = 10$  V,  $I_D = 80$  A
- UIS Capability
- These Device is Pb-Free and is RoHS Compliant
- Qualified to AEC-Q101

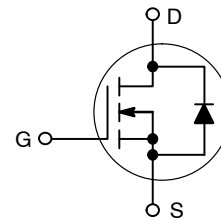
### **Applications**

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

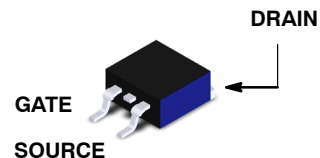


**ON Semiconductor®**

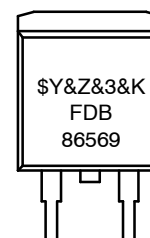
[www.onsemi.com](http://www.onsemi.com)



**D2PAK-3  
CASE 418AJ  
FDB SERIES**



### **MARKING DIAGRAM**



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FDB86569	= Specific Device Code

### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

## FDB86569–F085

### MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , Unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain to Source Voltage	60	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous ( $V_{GS} = 10\text{ V}$ ) (Note 1) $T_C = 25^\circ\text{C}$	80	A
	Pulsed Drain Current $T_C = 25^\circ\text{C}$	See Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	41	mJ
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	94	W
	– Derate Above $25^\circ\text{C}$	0.63	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	$-55$ to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	1.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 15\text{ }\mu\text{H}$ ,  $I_{AS} = 74\text{ A}$ ,  $V_{DD} = 60\text{ V}$  during inductor charging and  $V_{DD} = 0\text{ V}$  during time in avalanche.
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

### PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB86569	FDB86569–F085	D <sup>2</sup> –PAK (TO–263)	330 mm	24 mm	800 Units

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

**OFF CHARACTERISTICS**

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	60			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS} = 60\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $T_J = 25^\circ\text{C}$			1	$\mu\text{A}$
		$V_{DS} = 60\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $T_C = 175^\circ\text{C}$ (Note 1)			1	mA
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA

**ON CHARACTERISTICS**

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	2.0	2.8	4.0	V
$R_{DS(ON)}$	Drain to Source On Resistance	$I_D = 80\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $T_J = 25^\circ\text{C}$		4.4	5.6	$\text{m}\Omega$
		$I_D = 80\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $T_C = 175^\circ\text{C}$ (Note 1)		8.5	10.8	$\text{m}\Omega$

**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = 30\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$		2520		pF
$C_{oss}$	Output Capacitance			690		pF
$C_{rss}$	Reverse Transfer Capacitance			47		pF
$R_g$	Gate Resistance	$f = 1\ \text{MHz}$		2.0		$\Omega$
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{GS} = 0\ \text{V}$ to 10 V, $V_{DD} = 30\ \text{V}$ , $I_D = 80\ \text{A}$		35	52	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0\ \text{V}$ to 2 V, $V_{DD} = 30\ \text{V}$ , $I_D = 80\ \text{A}$		4.8		nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 30\ \text{V}$ , $I_D = 80\ \text{A}$		14		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			7.4		nC

**RESISTIVE SWITCHING CHARACTERISTICS**

$t_{ON}$	Turn-On Time	$V_{DD} = 30\ \text{V}$ , $I_D = 80\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $R_{GEN} = 6\ \Omega$			53	ns
$t_{d(ON)}$	Turn-On Delay			15		ns
$t_r$	Rise Time			20		ns
$t_{d(OFF)}$	Turn-Off Delay			22		ns
$t_f$	Fall Time			8		ns
$t_{OFF}$	Turn-Off Time				45	ns

**DRAIN–SOURCE DIODE CHARACTERISTICS**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 80\ \text{A}$ , $V_{GS} = 0\ \text{V}$			1.25	V
		$I_{SD} = 40\ \text{A}$ , $V_{GS} = 0\ \text{V}$			1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 80\ \text{A}$ , $dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$ , $V_{DD} = 48\ \text{V}$		52	68	ns
$Q_{RR}$	Reverse Recovery Charge			43	65	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. The maximum value is specified by design at  $T_J = 175^\circ\text{C}$ . Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

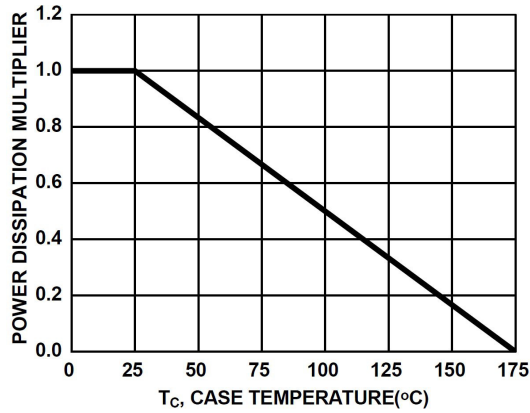


Figure 1. Normalized Power Dissipation vs. Case Temperature

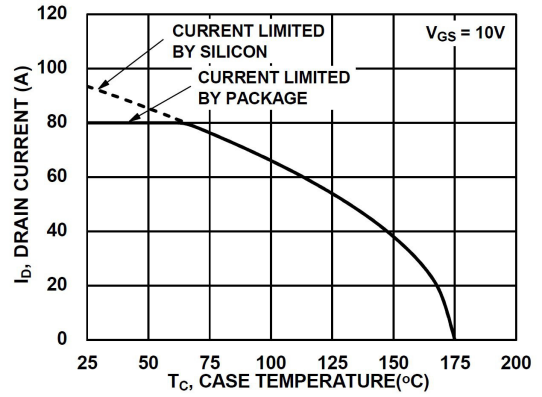


Figure 2. Maximum Continuous Drain Current vs Case Temperature

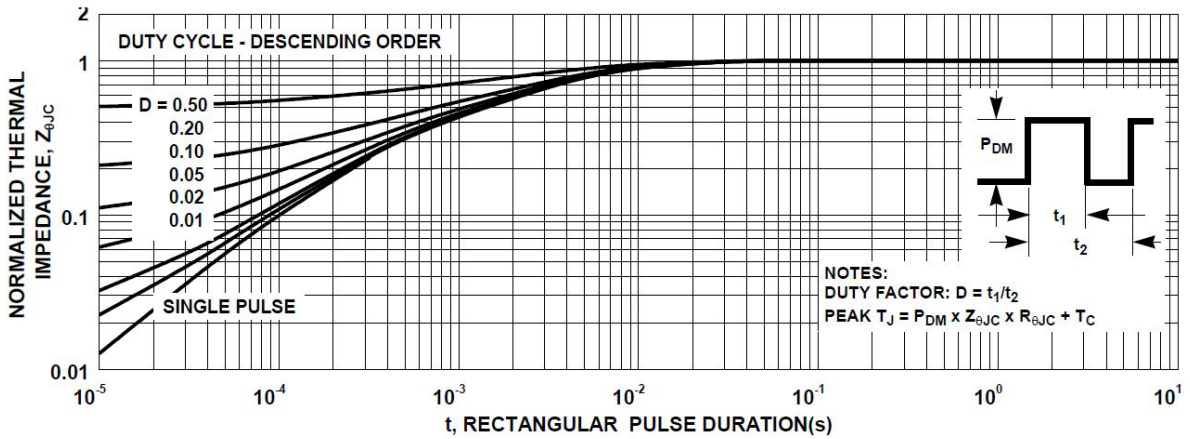


Figure 3. Normalized Maximum Transient Thermal Impedance

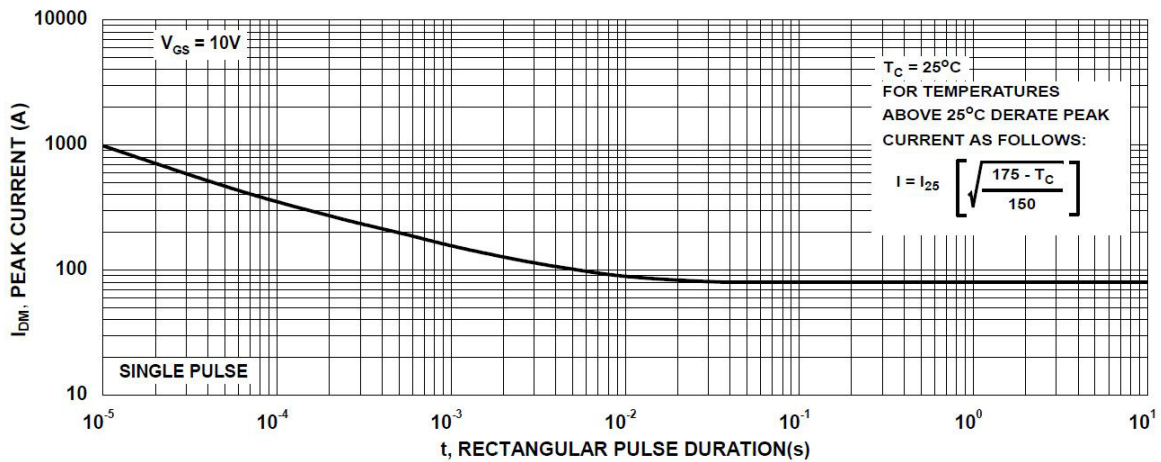


Figure 4. Peak Current Capability

## TYPICAL CHARACTERISTICS (Continued)

NOTE: Refer to ON Semiconductor Application Notes [AN-7514](#) and [AN-7515](#)

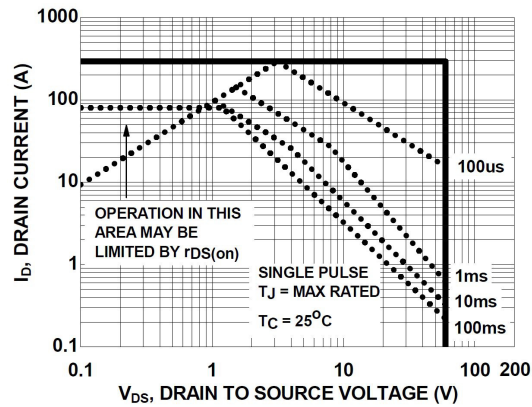


Figure 5. Forward Bias Safe Operating Area

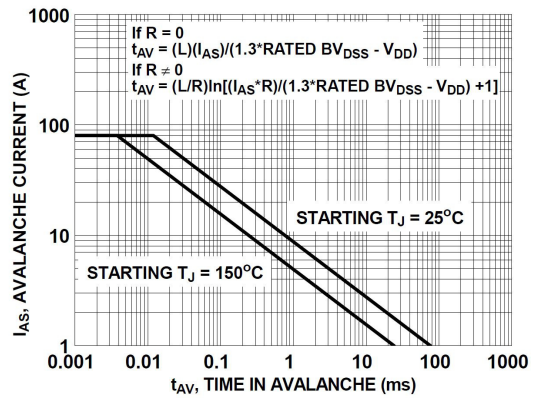


Figure 6. Unclamped Inductive Switching Capability

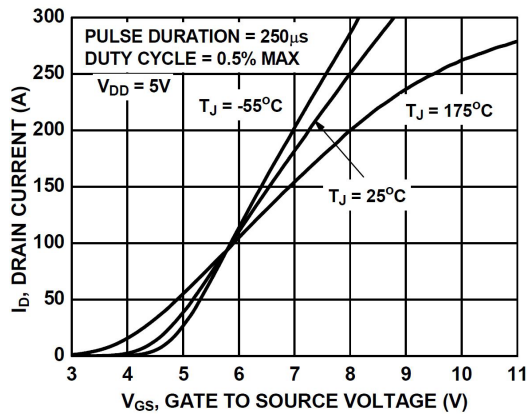


Figure 7. Transfer Characteristics

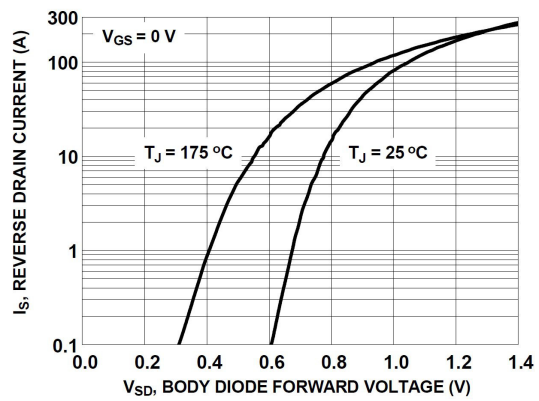


Figure 8. Forward Diode Characteristics

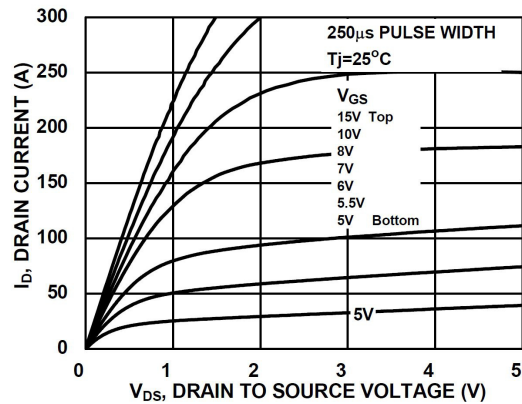


Figure 9. Saturation Characteristics

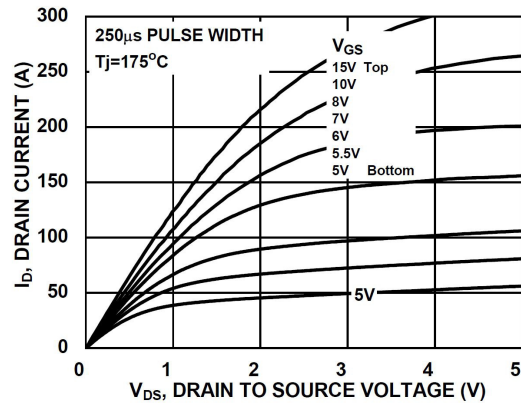


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (Continued)

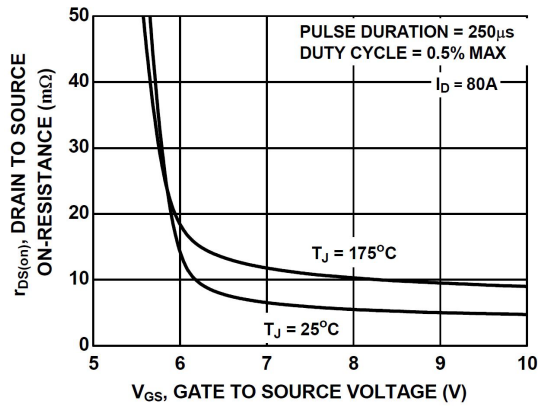


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

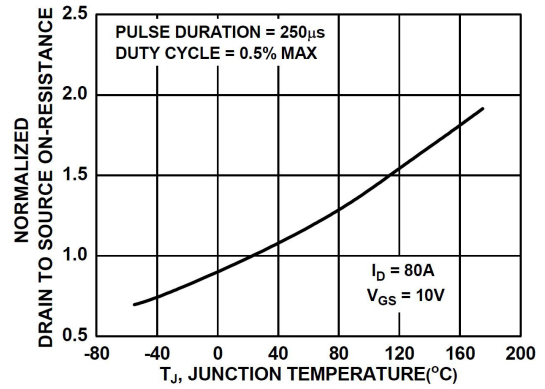


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

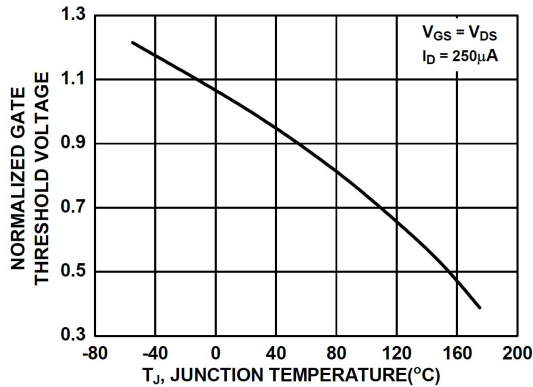


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

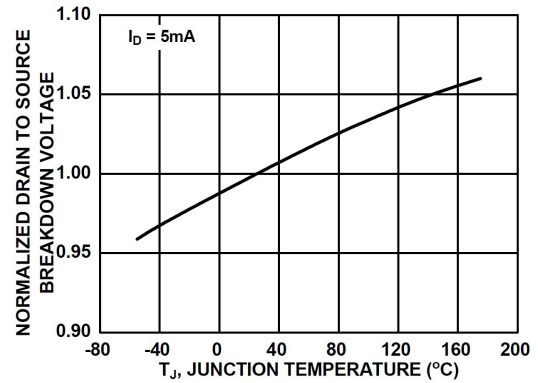


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

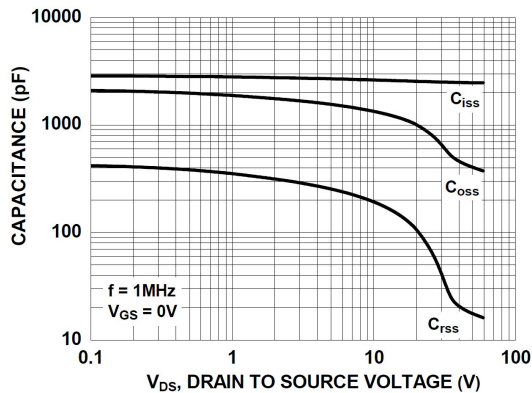


Figure 15. Capacitance vs. Drain to Source Voltage

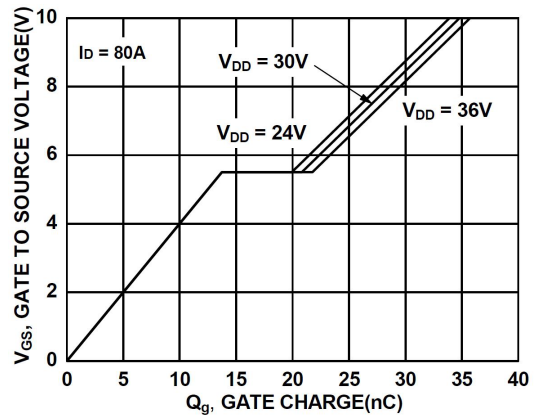
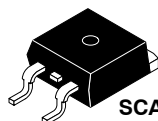


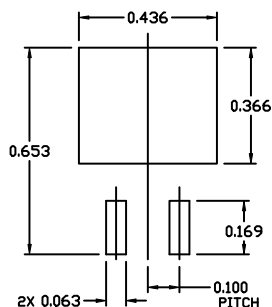
Figure 16. Gate Charge vs. Gate to Source Voltage



SCALE 1:1

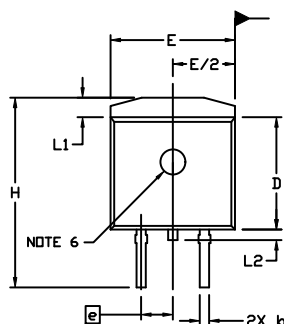
**D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)**  
CASE 418AJ  
ISSUE F

DATE 11 MAR 2021



**RECOMMENDED  
MOUNTING FOOTPRINT**

For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM1.

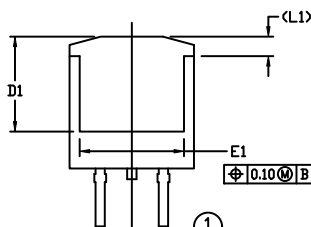
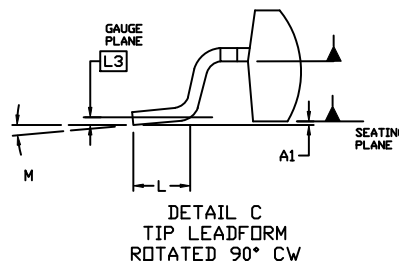
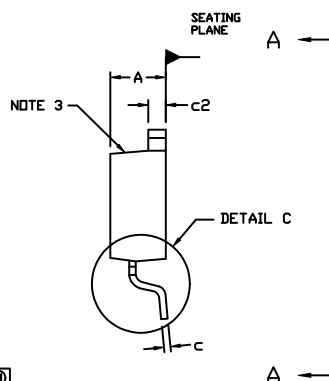


0.100 BSC 0.100 BSC

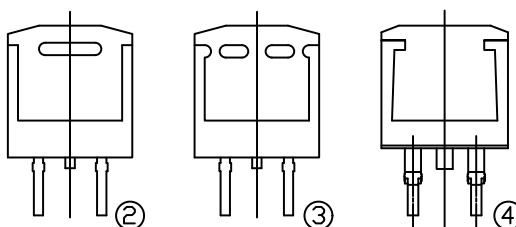
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC	---	2.54 BSC	---
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC	---	0.25 BSC	---
M	0°	8°	0°	8°

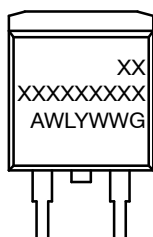


VIEW A-A

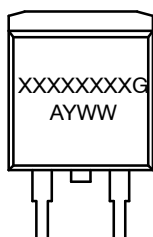


VIEW A-A  
OPTIONAL CONSTRUCTIONS

**GENERIC MARKING DIAGRAMS\***



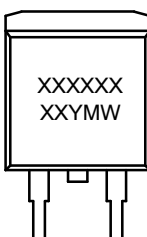
IC



Standard



Rectifier



SSG

XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
W = Week Code (SSG)  
M = Month Code (SSG)  
G = Pb-Free Package  
AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

<b>DOCUMENT NUMBER:</b>	<b>98AON56370E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)</b>	<b>PAGE 1 OF 1</b>

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)



# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[onsemi:](#)

[FDB86569-F085](#)