MOSFET – N-Channel, SUPERFET® II, Easy-Drive

600 V, 29 A, 125 mΩ

FCH125N60E

ON Semiconductor®

www.onsemi.com

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
600 V	125 mΩ @ 10 V	29 A

Description

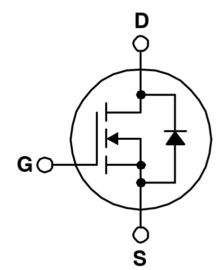
SUPERFET II MOSFET is ON Semiconductor's brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SUPERFET II MOSFET easy−drive series offers slightly slower rise and fall times compared to the SUPERFET II MOSFET series. Noted by the "E" part number suffix, this family helps manage EMI issues and allows for easier design implementation. For faster switching in applications where switching losses must be at an absolute minimum, please consider the SUPERFET II MOSFET series.

Features

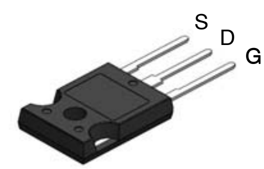
- Typ. $R_{DS(on)}$ = 102 mΩ
- 650 V @ T_J = 150°C
- Ultra Low Gate Charge (Typ. Q_g = 75 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 258 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Telecom / Sever Power Supplies
- Industrial Power Supplies

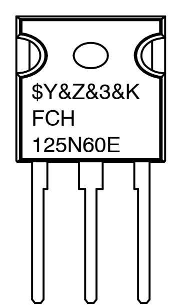


N-CHANNEL MOSFET



TO−247−3LD
CASE 340CK

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FCH125N60E	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FCH125N60E	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage	– DC	±20	V
		– AC (f > 1 Hz)	±30	
I_D	Drain Current:	– Continuous (T_C = 25°C)	29	A
		– Continuous (T_C = 100°C)	18	
I_{DM}	Drain Current:	– Pulsed (Note 1)	87	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		720	mJ
I_{AR}	Avalanche Current (Note 1)		6	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		2.78	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	278	W
		– Derate Above 25°C	2.2	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to + 150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 6.0 A, R_G = 25 Ω, Starting T_J = 25 °C.
3. $I_{SD} \le$ 14.5 A, di/dt ≤ 200 A/μs, $V_{DD} \le$ 380 V, Starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH125N60E	FCH125N60E	TO−247	Tube	N/A	N/A	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FCH125N60E	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.45	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 10 mA, V_{GS} = 0 V, T_J = 25°C	600	–	–	V
		I_D = 10 mA, V_{GS} = 0 V, T_J = 150°C	650	–	–	
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	–	0.7	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 480 V, V_{GS} = 0 V, T_C = 125 °C	–	2	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	–	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 14.5 A	–	102	125	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 14.5 A	–	25	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	–	2250	2990	pF
C_{oss}	Output Capacitance		–	60	80	pF
C_{rss}	Reverse Transfer Capacitance		–	17	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	–	258	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 380 V, I_D = 14.5 A, V_{GS} = 10 V (Note 4)	–	75	95	nC
Q_{gs}	Gate to Source Gate Charge		–	10	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	33	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	3.5	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380 V, I_D = 14.5 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	–	23	56	ns
t_r	Turn−On Rise Time		–	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		–	106	222	ns
t_f	Turn−Off Fall Time		–	23	56	ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	29	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	87	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 14.5 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 14.5 A, dI_F/dt = 100 A/μs	–	376	–	ns
Q_{rr}	Reverse Recovery Charge		–	6.5	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

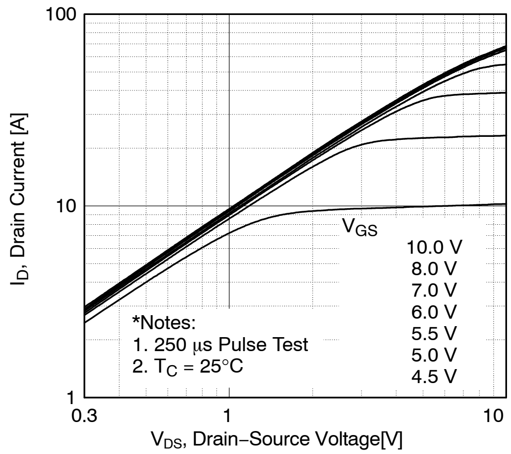


Figure 1. On−Region Characteristics

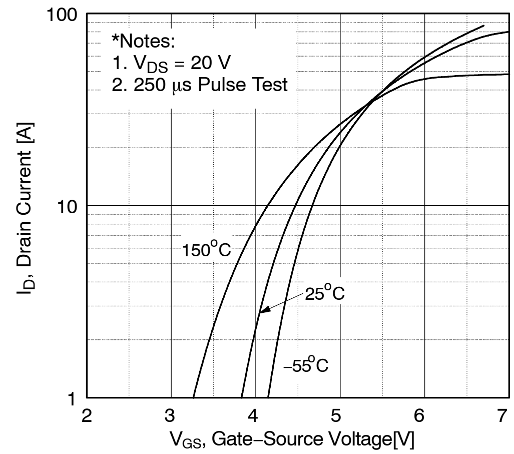


Figure 2. Transfer Characteristics

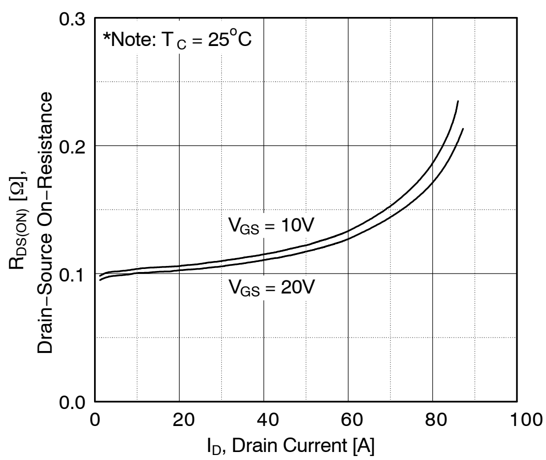


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

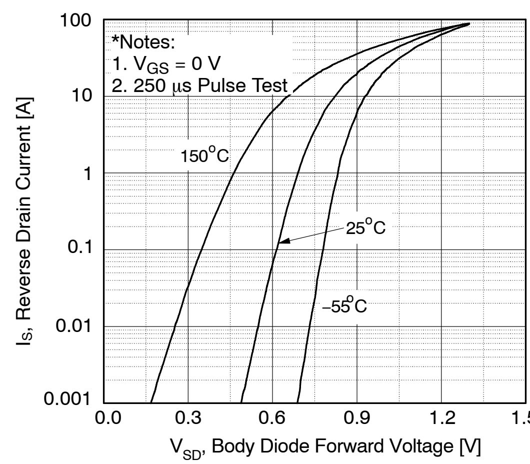


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

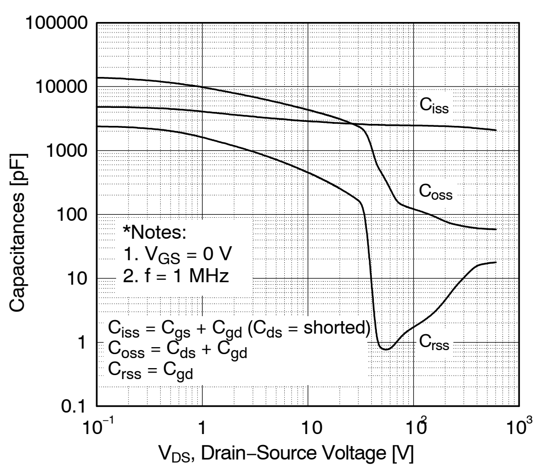


Figure 5. Capacitance Characteristics

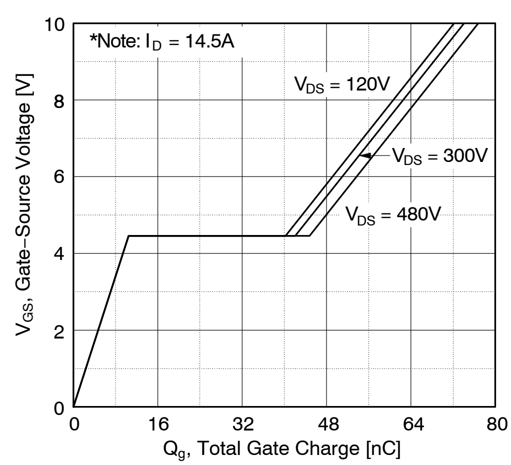


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

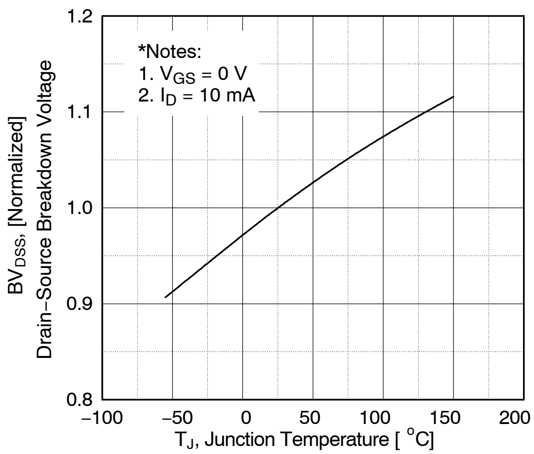


Figure 7. Breakdown Voltage Variation vs. Temperature

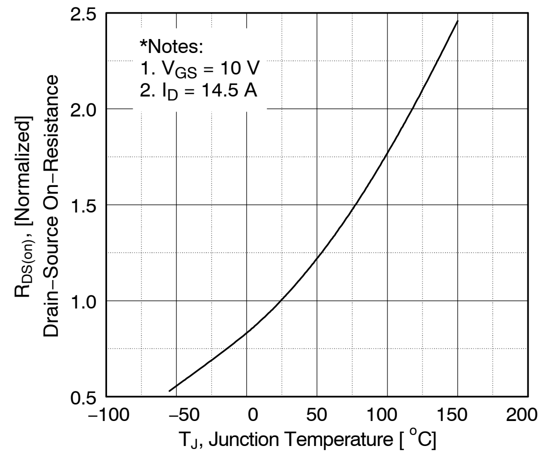


Figure 8. On−Resistance Variation vs. Temperature

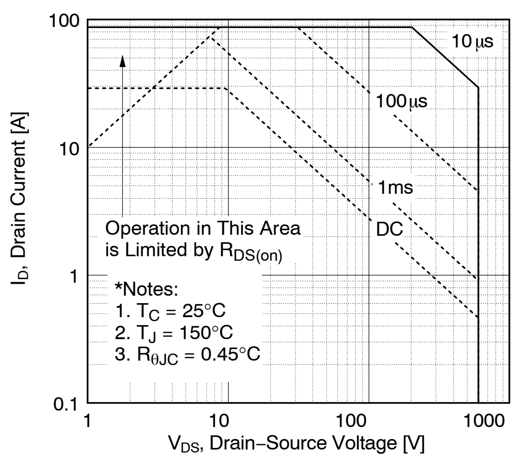


Figure 9. Maximum Safe Operating Area

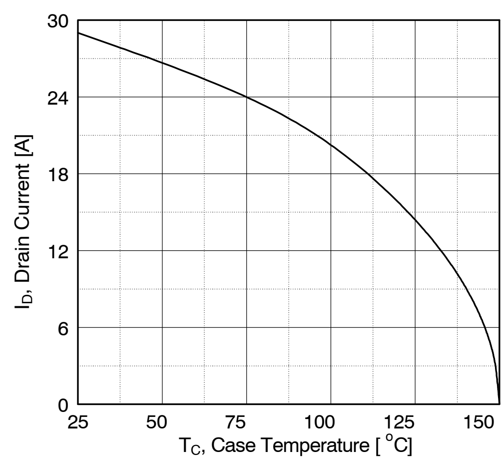


Figure 10. Maximum Drain Current vs. Case Temperature

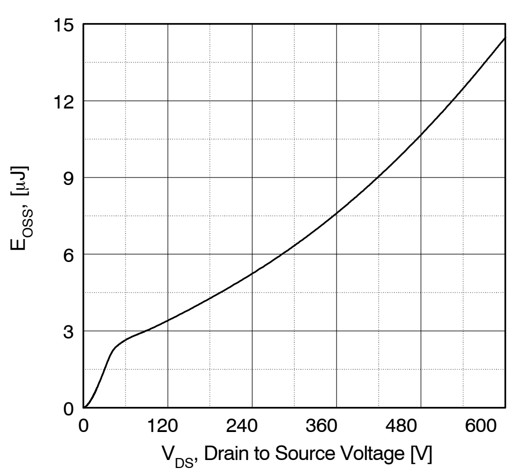


Figure 11. Eoss vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS

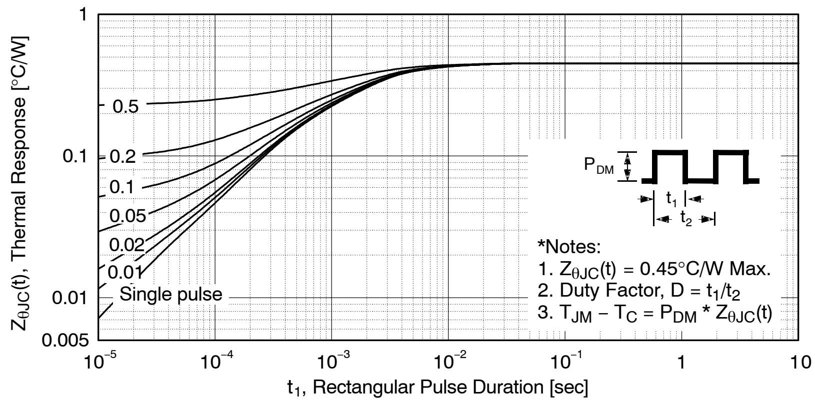


Figure 12. Transient Thermal Response Curve

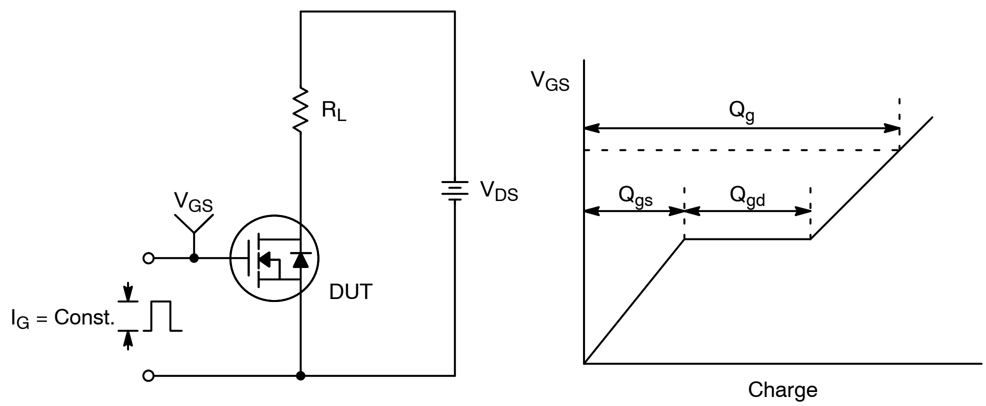


Figure 13. Gate Charge Test Circuit & Waveform

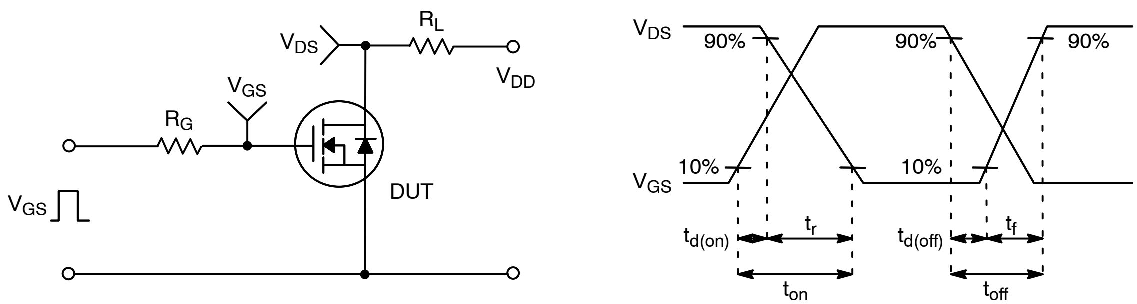


Figure 14. Resistive Switching Test Circuit & Waveforms

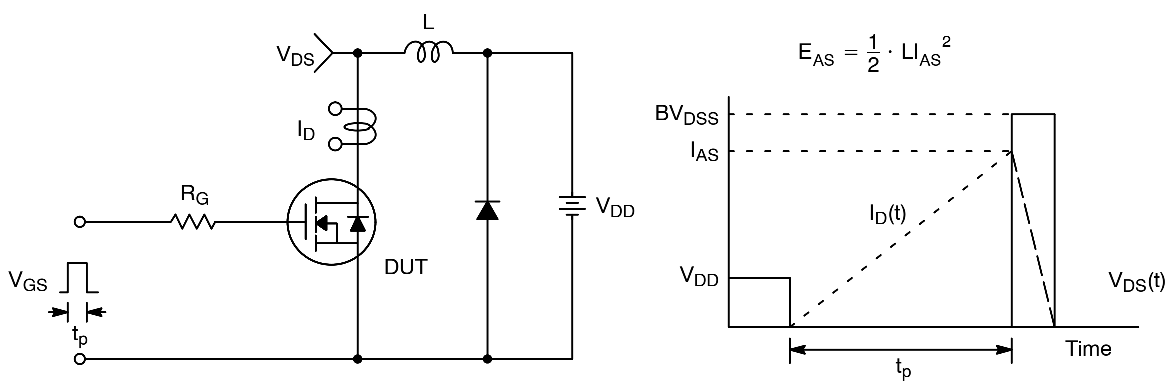


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

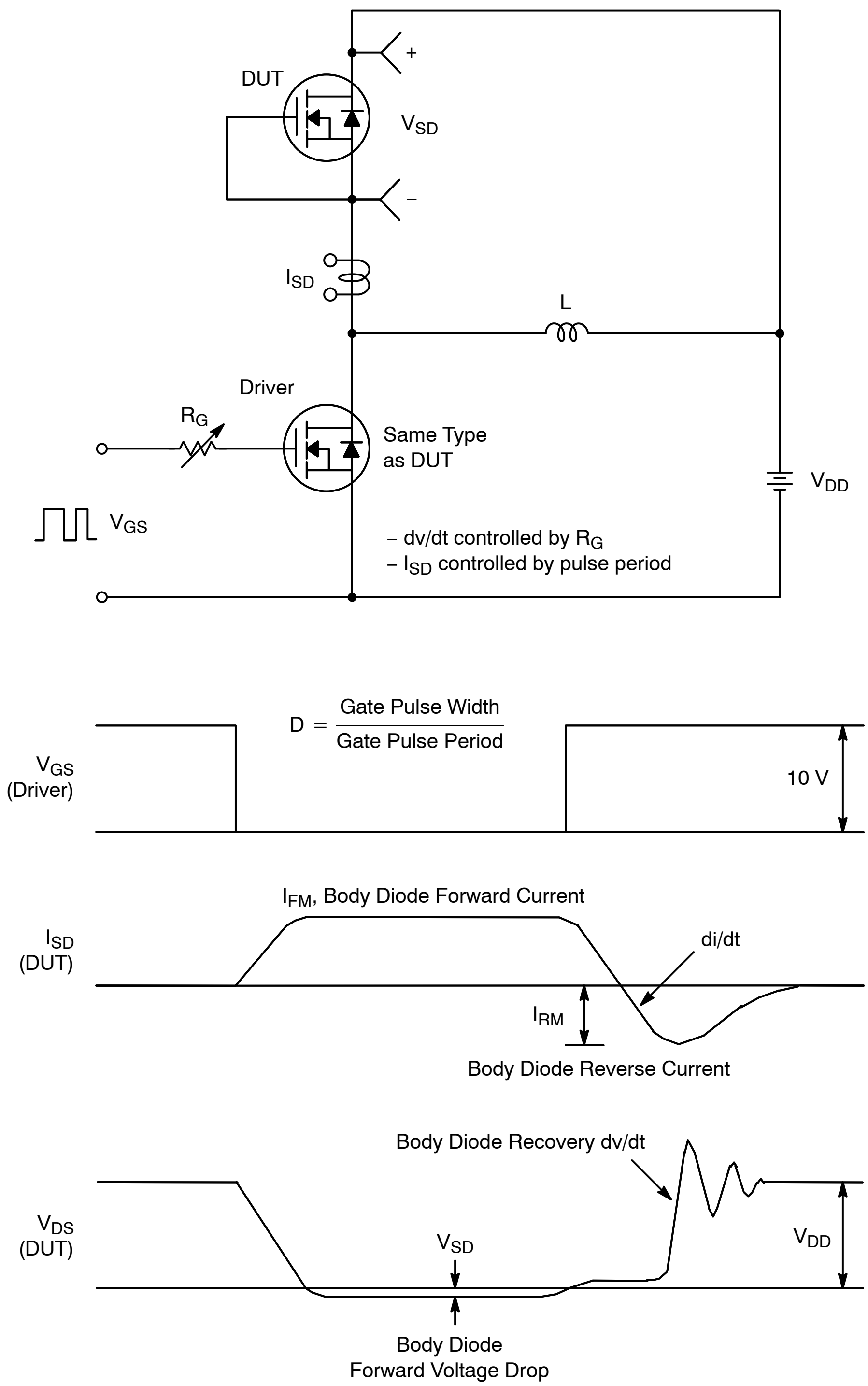


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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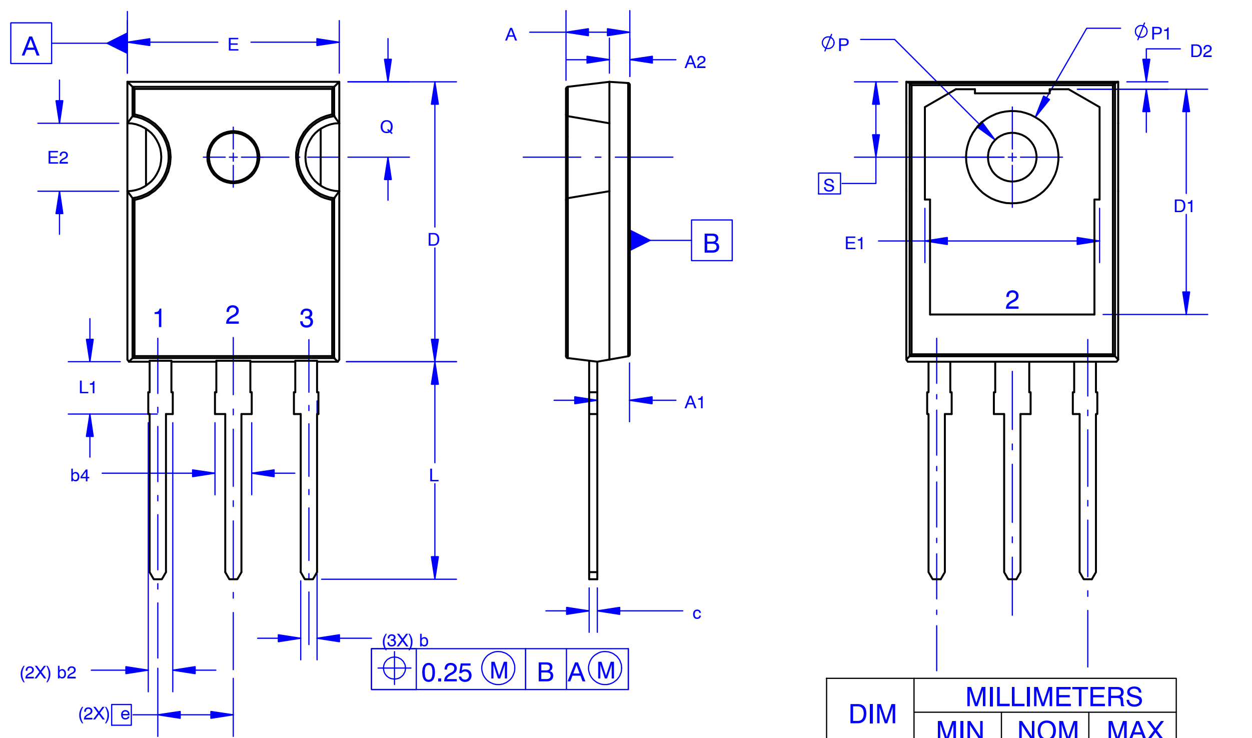
CASE 340CK
ISSUE A

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

GENERIC MARKING DIAGRAM*

AYWWZZ
XXXXXXX
XXXXXXX

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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