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FAN6292BMX/FAN6292MX

Compact Secondary-Side Synchronous Rectifier Control with USB Type-C Control

FAN6292BMX/FAN6292MX are highly integrated, secondary-side power adaptor controllers compatible with Type-C control. Internally adopted synchronous rectifier control helps for less BOM counts as well as easy design.

FAN6292BMX/FAN6292MX are also a source only USB Type-C controllers which are optimized for mobile chargers and power adapters. It supports standard 3 A VBUS current level. N-Channel MOSFET is compatible as a load switch, and helps to reduce BOM cost.

FAN6292BMX/FAN6292MX incorporate adaptive output under-voltage protection to improve system reliability.

Features

- Type-C Control for Standard 3 A VBUS Current
- N-Channel MOSFET Control as a Type-C Load Switch
- Internal Synchronous Rectifier Control Circuit
- Protections for Safe Operation; Output Under-Voltage-Protection

Typical Applications

- Battery Chargers for Smart Phones, Feature Phones, and Tablet PCs
- AC-DC Adapters for Portable Devices that Require CV/CC Control

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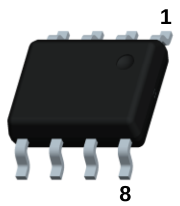
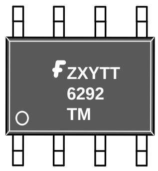


TSSOP-8

MARKING DIAGRAM

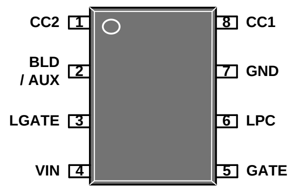


1st Line:
- F: Corporate Logo
- Z: Assembly Plant Code
- X: Year Code
- Y: Week Code
- TT: Die Run Code

2nd Line:
- 6292 : IC Part Name for FAN6292MX
- 6292B: IC Part Name for FAN6292BMX

3rd Line:
- T: Package Type (M=SOIC)
- M: Manufacture Flow Code

PIN CONNECTIONS



(TOP View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

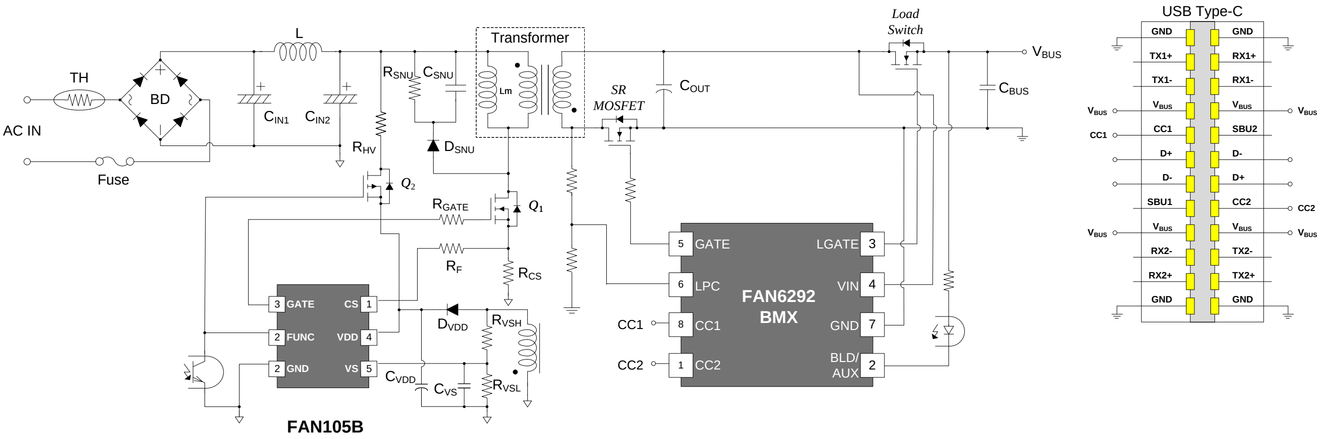


Figure 1 FAN6292BMX Typical Application Schematic

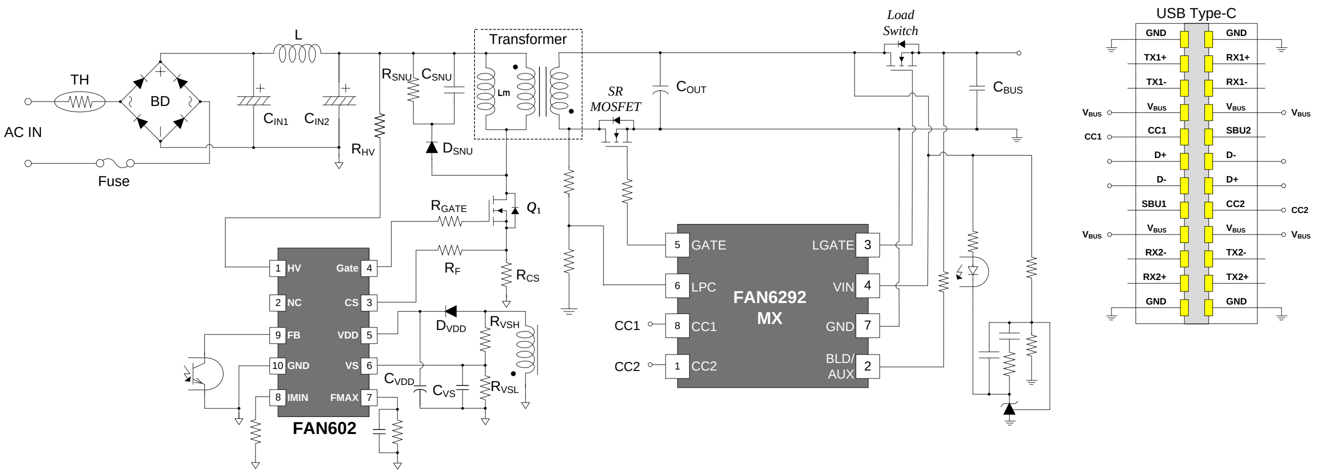


Figure 2 FAN6292MX Typical Application Schematic

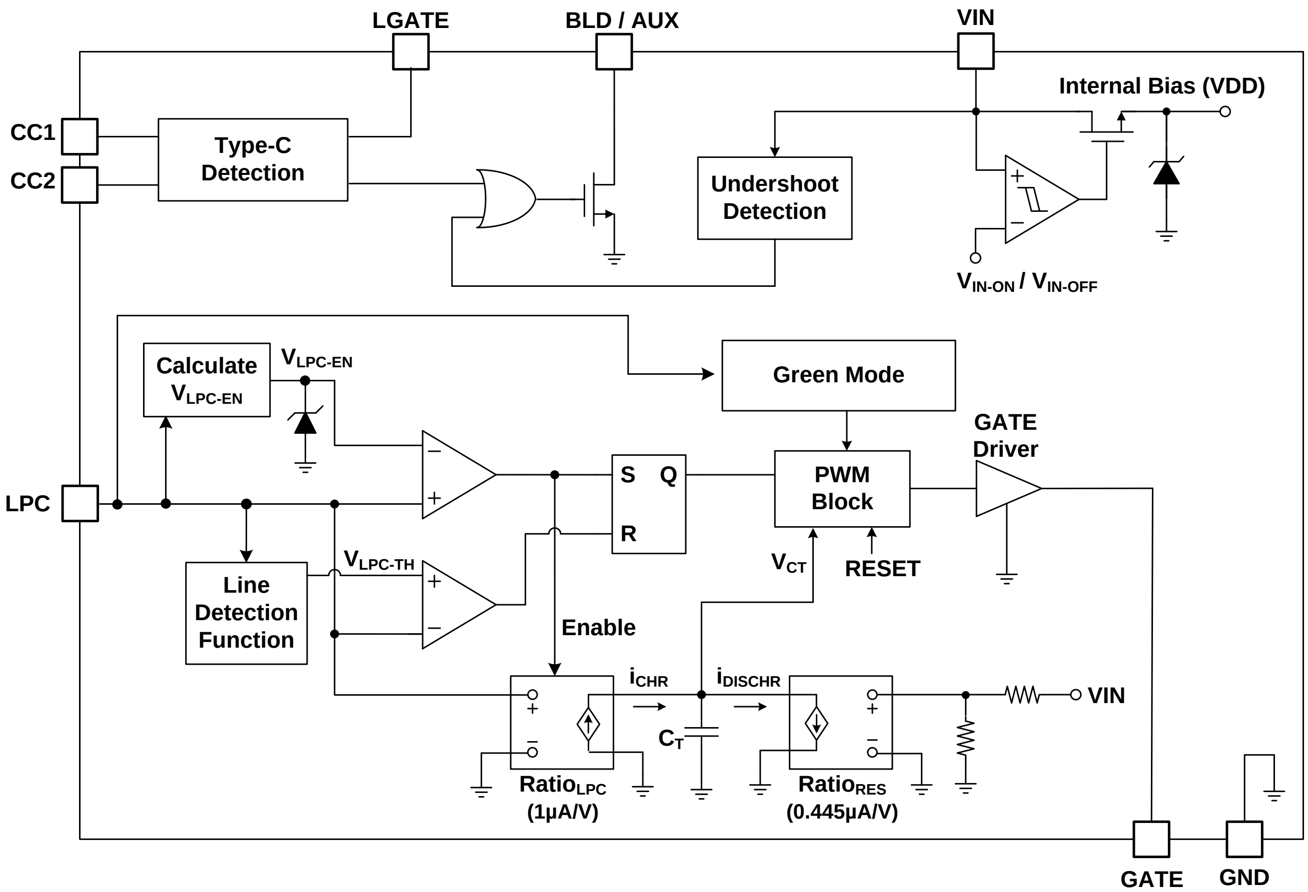


Figure 3 FAN6292BMX/FAN6292MX Function Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	CC2	**Configuration Channel 2.** This pin is used to detect connections of Type-C cables and connectors. It is tied to the USB Type-C CC2.
2	BLD / AUX	**Bleeder and AUX function.** Discharging path of output capacitor when UFP detachment is acknowledged. In addition, information is delivered to primary to enhance output performance.
3	LGATE	**Load Switch Gate.** This pin is tied to the gate of the load switch
4	VIN	**Input Voltage.** This pin is tied to the output of the adaptor to monitor its output voltage and supply internal bias. IC operating current, and MOSFET gate drive current are supplied through this pin.
5	GATE	**Gate Drive Output.** Totem-pole output to drive the external SR MOSFET.
6	LPC	**SR MOSFET Drain Voltage Detection.** This pin is used to detect the voltage on the secondary winding during the on time period of the primary MOSFET.
7	GND	**Ground.**
8	CC1	**Configuration Channel 1.** This pin is used to detect connections of Type-C cables and connectors. It is tied to the USB Type-C CC1.

MAXIMUM RATINGS (Note 1,2,3)

Rating	Symbol	Value	Unit
VIN Pin Input Voltage	V_{IN}	20	V
BLD/AUX Pin Input Voltage	$V_{BLD/AUX}$	20	V
LGATE Pin Input Voltage	V_{LGATE}	20	V
CC1 Pin Input Voltage	V_{CC1}	-0.3 to 6.0	V
CC2 Pin Input Voltage	V_{CC2}	-0.3 to 6.0	V
LPC pin input voltage	V_{LPC}	-0.3 to 6.5	V
GATE pin input voltage	V_{GATE}	-0.3 to 6.0	V
Power Dissipation (T_A=25°C)	P_D	850	mW
Operating Junction Temperature	T_J	-40 to 150	°C
Storage Temperature Range	T_{STG}	-40 to 150	°C
Lead Temperature, (Soldering,10 Seconds)	T_L	260	°C
Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 (Note 4)	ESD_{HBM}	4	kV
Charged Device Model, JESD22-C101 (Note 4)	ESD_{CDM}	1.75	kV

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. All voltage values, except differential voltages, are given with respect to the GND pin.
3. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
4. Meets JEDEC standards JS-001-2012 and JESD 22-C101.

THERMAL CHARACTERISTICS (Note 5)

Rating	Symbol	Value	Unit
Thermal Characteristics, Thermal Resistance, Junction-to-Air Thermal Reference, Junction-to-Top	 $R_{\theta JA}$ $R_{\psi JT}$	 153 22	°C/W

5. T_A=25°C unless otherwise specified.

RECOMMENDED OPERATING RANGES (Note 6)

Rating	Symbol	Min	Max	Unit
VIN Pin Input Voltage	V_{IN}	0	6	V
BLD/AUX Pin Input Voltage	$V_{BLD/AUX}$	0	6	V
LGATE Pin Input Voltage	V_{LGATE}	0	10	V
CC1 Pin Input Voltage	V_{CC1}	0	5.8	V
CC2 Pin Input Voltage	V_{CC2}	0	5.8	V
LPC pin input voltage	V_{LPC}	0	5	V
GATE pin input voltage	V_{GATE}	0	5.5	V

6. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{IN}=5 V, LPC=1.5 V, LPC width=2 µs at T_J= -40~125 °C, F_{LPC}=100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VIN Section						
Continuous Operating Voltage(7)		V_{IN-OP}			6	V
Operating Supply Current	V_{IN}=5 V	$I_{IN-OP-5V}$		8		mA
Green Mode Operating Supply Current	V_{IN}=5 V, with SR gate F = 400Hz CC1/CC2 open circuit	$I_{IN-OP-Green}$	0.5	0.9	1.3	mA
Internal Bias Section						
Turn-On Threshold Voltage	V_{IN} increases	V_{IN-ON}	3.0	3.2	3.4	V
Turn-Off Threshold Voltage	V_{IN} decreases	V_{IN-OFF}	2.75	2.85	2.95	V
Green Mode Section (FAN6292BMX)						
Green Mode Enable Debounce Time	Non-switching time, when LPC falling	$t_{Green-EN-Debounce}$	54	64	74	µs
Number of switching to enter green mode	When switching period > $T_{Green-EN-Debounce}$	$N_{Green-EN-Debounce}$		1		Cycle
Green Mode Disable Debounce Time	Enable after enter green mode, Non-switching time, when LPC falling	$t_{Green-DIS-Debounce}$	54	64	74	µs
Green Mode Section (FAN6292MX)						
Green Mode Enable Debounce Time	Non-switching time, when when LPC falling	$t_{Green-EN-Debounce}$	0.4	0.5	0.6	ms
Green Mode Disable Debounce Time	Enable after enter green mode, Non-switching time, when LPC falling	$t_{Green-DIS-Debounce}$	0.2	0.3	0.4	ms
Number of consecutive switching to leave green mode	Independently enable with $T_{Green-DIS-Debounce}$, when LPC falling	$N_{Green-DIS-Debounce}$		256		Cycles
Bleeder Section						
BLD Pin Sink Current through when bleeding (7)	V_{BLD}=5 V	$I_{BLD-Sink}$	90			mA
Maximum Discharging Time when bleeding		$t_{BLD-MAX}$	275	320	365	ms
AUX Section (FAN6292BMX)						
Output undershoot detection threshold voltage		V_{IN-AUX}	4.7	4.8	4.9	V
Internal debounce time to enable I_{AUX}(7)	RC filter type	$T_{AUX-Debounce}$			5	µs
BLD/AUX pin pull-down time		T_{AUX-ON}	44	64	84	µs
BLD/AUX pin pull down current with V_{AUX}=5V	V_{BLD}=5 V, R_{BLD}=0 Ω	I_{AUX}	3.3		15	mA

ELECTRICAL CHARACTERISTICS

V_{IN}=5 V, LPC=1.5 V, LPC width=2 µs at T_J= -40~125 °C, F_{LPC}=100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Type-C Section						
Source current on CC1 pin	V_{IN}=5 V, V_{CC2}=0 V	I_{P-CC1}	304	330	356	µA
Source current on CC2 pin	V_{IN}=5 V, V_{CC1}=0 V	I_{P-CC2}	304	330	356	µA
Input impedance on CC1 pin		$Z_{OPEN-CC1}$	126			kΩ
Input impedance on CC2 pin		$Z_{OPEN-CC2}$	126			kΩ
Ra impedance detection threshold on CC1 pin	V_{IN}=5 V, V_{CC2}=0 V, Decreasing V_{CC1}	V_{RA-CC1}	0.75	0.80	0.85	V
Ra impedance detection threshold on CC2 pin	V_{IN}=5 V, V_{CC1}=0 V, Decreasing V_{CC2}	V_{RA-CC2}	0.75	0.80	0.85	V
Rd impedance detection threshold on CC1 pin	V_{IN}=5 V, V_{CC2}=0 V, Increasing V_{CC1}	V_{RD-CC1}	2.45	2.60	2.75	V
Rd impedance detection threshold on CC2 pin	V_{IN}=5 V, V_{CC1}=0 V, Increasing V_{CC2}	V_{RD-CC2}	2.45	2.60	2.75	V
UFP attachment debounce time	V_{IN}=5 V, V_{CC2}=0 V, Increasing V_{CC1}	$t_{CC-Attach-debounce}$	100	150	200	ms
UFP detachment debounce time	V_{IN}=5 V, V_{CC2}=0 V, Decreasing V_{CC1}	$t_{CC-Detach-debounce}$	10	15	20	ms
After $t_{CC-attach-debounce}$ until V_{BUS}=5 V(7)	V_{IN}=5 V, V_{CC2}=0 V, Increasing V_{CC1}	$t_{VBUS-ON}$			275	ms
After detaching UFP until V_{BUS}=0 V(7)	V_{IN}=5 V, V_{CC2}=0 V, Decreasing V_{CC1}	$t_{VBUS-OFF}$			650	ms
Gate high voltage	V_{IN}=5 V	V_{NGATE}	8		10	V
Output Driver Section						
Output Voltage Low	V_{IN}=5 V, I_{GATE}=100 mA	V_{OL}		0.16	0.25	V
Output Voltage High	V_{IN}=5 V	V_{OH}	4.5			V
Rising Time(7)	V_{IN}=5 V, C_L=3300 pF, GATE=1 V ~ 4 V	t_R		20	35	ns
Falling Time(7)	V_{IN}=5 V, C_L=3300 pF, GATE=4 V~ 1 V	t_F		9		ns
Propagation Delay to OUT High (LPC trigger)	V_{IN}=5 V, GATE=1 V	$t_{PD-HIGH-LPC}$		44	80	ns
Propagation Delay to OUT Low (LPC trigger)(7)	V_{IN}=5 V, GATE=4 V	$t_{PD-LOW-LPC}$		30		ns
Gate inhibit Time(7)		$t_{INHIBIT}$		1.4		µs
Gate start-up disable time	For FAN602 (FAN6292MX)	$t_{SR-startup-dis}$		60		ms
Gate start-up disable time	For FAN105B (FAN6292BMX)	$t_{SR-startup-dis}$	1.5	2	2.5	ms

ELECTRICAL CHARACTERISTICS

V_{IN}=5 V, LPC=1.5 V, LPC width=2 µs at T_J= -40~125 °C, F_{LPC}=100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Internal RES section						
Internal RES ratio	V_{IN}=5 V, Turn-ratio=15~17	K_{RES}	0.196	0.200	0.204	V/V
VIN Dropping Protection Ratio with Two Cycle	LPC width=5 µs VIN=5 V to 3.5 V	$K_{VIN-DROP}$	70		90	%
Debounce time for disable SR when VIN dropping protection		t_{SR_OFF}	3.5	5.5	7.5	ms
Debounce time for noise immunity on VIN(7)		$t_{VIN-Debounce}$	1	2	3	µs
LPC Section						
Linear Operation Range of LPC Pin Voltage(7)	$V_{IN\ -OFF} < V_{IN} \leq 5V$	V_{LPC}	0.4		V_{IN} -1	V
LPC Sink Current	V_{LPC}=1V	$I_{LPC-SINK}$		100		nA
SR Enabled Threshold Voltage @High Line		$V_{LPC-HIGH-H}$	1.418	1.500	1.583	V
Threshold Voltage on LPC Rising Edge @High Line(7)	$V_{LPC-HIGH-H}$ *0.875 = $V_{LPC-TH-H}$	$V_{LPC-TH-H}$	1.205	1.313	1.424	V
SR Enabled Threshold Voltage @ Low Line	$V_{LPC-HIGH-L-5V}$ = $V_{LPC-TH-L-5V}$ / 0.875	$V_{LPC-HIGH-L-5V}$	0.703	0.743	0.783	V
Threshold Voltage on LPC Rising Edge @ Low Line(7)	Spec.=0.4+0.05*VIN VIN = 5V	$V_{LPC-TH-L-5V}$	0.63	0.650	0.67	V
Falling Edge Threshold Voltage to trigger SR (7)		$V_{LPC-TH-TRIG}$		70		mV
Low to High Line Threshold Voltage on LPC pin	VIN = 5V, Spec.=(0.8+0.03*VIN)*2	$V_{LINE-H-5V}$	1.81	1.90	1.99	V
High to Low Line Threshold Voltage on LPC pin	VIN = 5V, Spec.=(0.75+0.03*VIN)*2	$V_{LINE-L-5V}$	1.72	1.80	1.88	V
Line Change Threshold Hysteresis	$V_{LINE-HYS-5V}$ = $V_{LINE-H-5V}$ - $V_{LINE-L-5V}$	$V_{LINE-HYS-5V}$		0.1		V
Higher Clamp Voltage		$V_{LPC-CLAMP-H}$	5.4	6.2	7.0	V
LPC Threshold Voltage to Disable SR Gate Switching	V_{IN} = 5V LPC=3V↑	$V_{LPC-DIS}$	V_{IN} - 0.6			V
Enable VLPC-DIS	Increasing V_{IN}	$V_{EN-LPC-DIS}$	4.25	4.4	4.45	V
Disable VLPC-DIS	Decreasing V_{IN}	$V_{DIS-LPC-DIS}$	4.1	4.2	4.3	V
Line Change Debounce from Low Line to High Line(7)	Counts for LPC falling < $V_{LPC-TH-L-5V}$	$t_{LPC-LH-debounce}$		7		cycles
Line Change Debounce from High Line to Low Line(7)		$t_{LPC-HL-debounce}$		15		µs

ELECTRICAL CHARACTERISTICS

V_{IN}=5 V, LPC=1.5 V, LPC width=2 µs at T_J= -40~125 °C, F_{LPC}=100 kHz, unless otherwise specified

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Internal Timing Section						
LPC Transfer Ratio to I_{LPC} (7)		$Ratio_{LPC}$		1		µA/V
V_{RES} Transfer Ratio to I_{RES} (7)		$Ratio_{RES}$		0.445		µA/V
Ratio between V_{LPC} & V_{RES}	VIN=5V, F_{LPC}=50 kHz, K_{RES}=0.20	$Ratio_{LPC-RES}$	3.15	3.37	3.59	
Minimum LPC Time to Enable the SR Gate @ High Line	V_{LPC}=3V	$t_{LPC-EN-H}$	80	180	280	ns
Minimum LPC Time to Enable the SR Gate @ Low Line	V_{LPC}=1.5V	$t_{LPC-EN-L}$	500	600	700	ns
Minimum Gate Width	FAN6292BMX	t_{MIN}	1.9	2.2	2.5	µs
Max SR On Time (7)		t_{ON-MAX}	20			µs
$t_{on-SR}(n+1)$- $t_{on-SR}(n) < t_{gate-limit}$		$t_{gate-limit}$	350	500	650	ns
Maximum Gate Limit On-time) (7)		$t_{gate-limit-max}$		5		µs
Forced internal CT reset time (7)		$t_{CT-RESET}$		10		ns
Reverse Current Mode Section						
Reverse current mode entry debounce time	V_{IN}=5 V, V_{LPC}=0 V	$T_{reverse-debounce}$	350	500	650	ms
Operating current during reverse current mode	V_{IN}=5 V, V_{LPC}=0 V	$I_{OP.reverse}$			1.7	mA
Source current on CC1 pin during reverse current mode (7)	V_{IN}=5 V, V_{LPC}=0 V	$I_{P-CC1.reverse}$			10	µA
Source current on CC2 pin during reverse current mode (7)	V_{IN}=5 V, V_{LPC}=0 V	$I_{P-CC2.reverse}$			10	µA
AUX pin current during reverse current mode (7)	V_{IN}=5 V, V_{LPC}=0 V	$I_{BLD.reverse}$			10	uA

7. Guaranteed by Design.
8. Guaranteed at -5° ~ 85°C.

TYPICAL CHARACTERISTICS

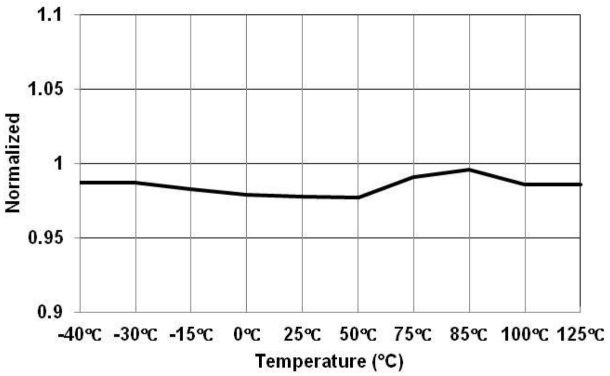


Figure 4 Turn-On Threshold Voltage (V_{IN-ON}) vs. Temperature

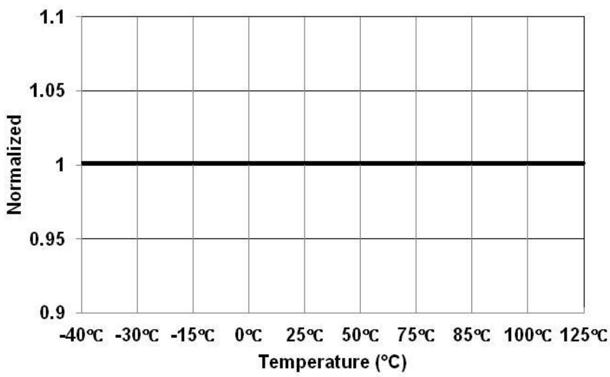


Figure 5 Turn-Off Threshold Voltage (V_{IN-OFF}) vs. Temperature

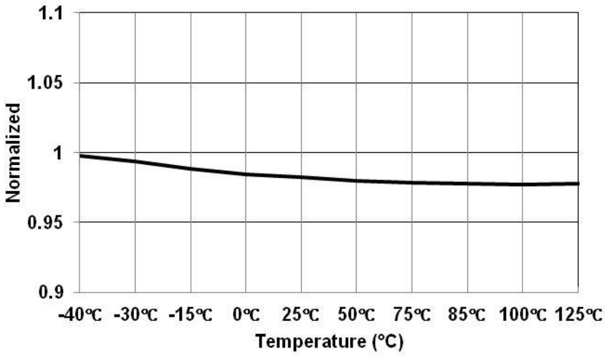


Figure 6 Minimum LPC Time to Enable the SR Gate @ Low-Line ($t_{LPC-EN-L}$) vs. Temperature

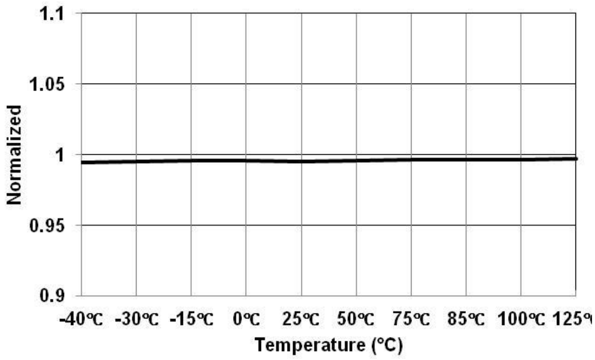


Figure 7 VIN Under-Voltage-Protection Enable (V_{IN-AUX}) vs. Temperature

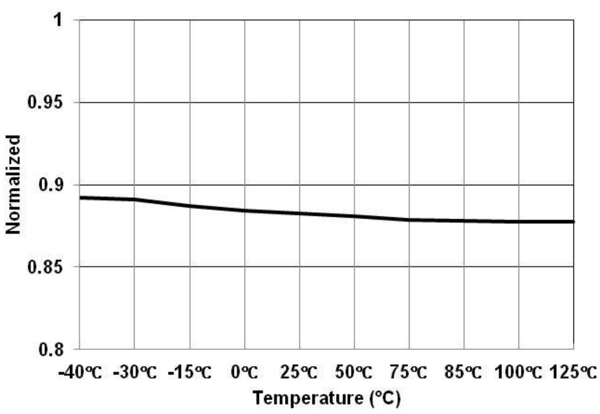


Figure 8 Minimum LPC Time to Enable the SR Gate @ High-Line ($t_{LPC-EN-H}$) vs. Temperature

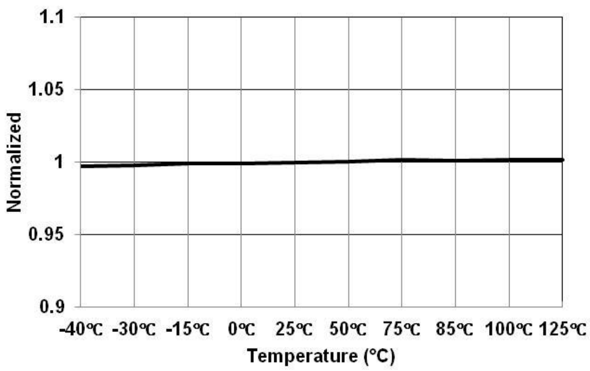


Figure 9 Ratio between V_{LPC} & V_{RES} ($Ratio_{LPC-RES}$) vs. Temperature

TYPICAL CHARACTERISTICS

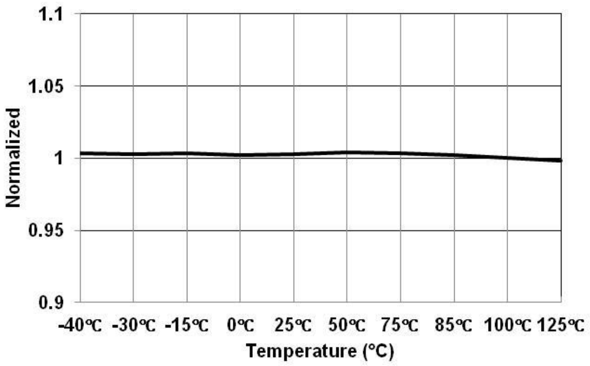


Figure 10 Source Current on CC1 Pin (I_{P-CC1}) vs. Temperature

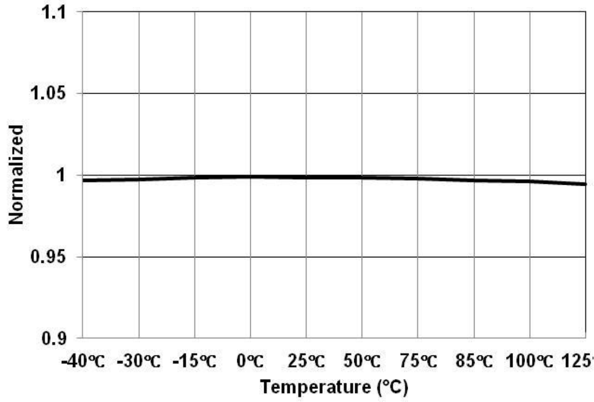


Figure 11 Source Current on CC2 Pin (I_{P-CC2}) vs. Temperature

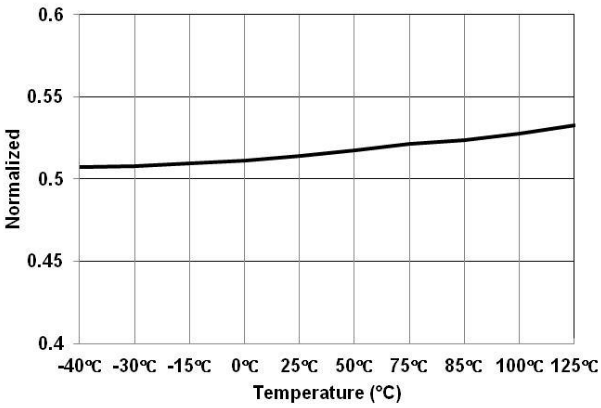


Figure 12 Operating Current during Reverse Current Mode($I_{OP.reverse}$) vs. Temperature

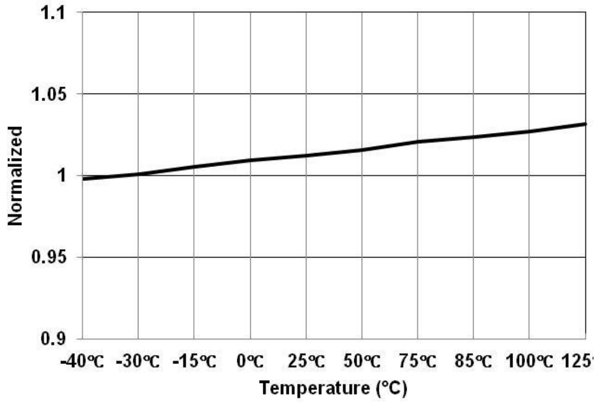


Figure 13 Gate High Voltage (V_{NGATE}) vs. Temperature

APPLICATIONS INFORMATION

N-channel MOSFET for Load Switch

FAN6292BMX/FAN6292MX implement Type-C block to enable or disable an external load switch. Internally adapted charge pump lets it control N-channel MOSFET as a load switch. It helps system be more cost competitive compared to P-channel MOSFET as a load switch. Since the minimum pumped voltage is V_{BUS}+3 V, it is recommended to use N-channel MOSFET supporting lower gate threshold levels.

Detail of Load Switch Control

FAN6292BMX/FAN6292MX support output current higher than 1.5 A. In order to meet Type-C specification, 330 µA is applied on CC1 pin and CC2 pin. When Rd (5.1 kΩ) is attached on either CC1 or CC2, load switch is turned-on after 150 ms debounce time. As soon as load switch is enabled, BC1.2 counter is enabled. To acknowledge detachment, it needs 15 ms (typ.) debounce time. When load switch is turned-off, bleeder is also enabled at the same time.

Green Mode Operation (for FAN6292BMX)

In order to reduce power consumption at light-load conditions with FAN105B system, FAN6292BMX in green mode will disable LPC internal detection block but SR contiously works at mini on time for FAN105B which is a pure primary side controller to normally regulate output voltage. When V_{LPC} is smaller than $V_{LPC-HIGH-L-5V}$ and maintains duration longer than $t_{Green-EN-Debounce}$, FAN6292MX enters green mode where current can be reduced to 0.9 mA (typ.). It leaves green mode when V_{LPC} is larger than $V_{LPC-HIGH-L-5V}$ and maintains duration shorter than $t_{Green-DIS-Debounce}$.

Green Mode Operation(for FAN6292MX)

In order to reduce power consumption at light-load conditions with FAN602 system, FAN6292MX enters the green mode where some internal blocks are disabled such as Synchronous Rectifier control block. Therefore, the operating current can be largely reduced. It enters Green Mode when V_{LPC} is smaller than $V_{LPC-HIGH-L-5V}$ and maintains duration longer than $t_{Green-EN-Debounce}$. It leaves green mode when V_{LPC} is larger than $V_{LPC-HIGH-L-5V}$ and maintains duration shorter than $t_{Green-DIS-Debounce}$.

Bleeder Function

When the portable device is detached, BUS voltage should be discharged to zero within a short time to meet TypeC specification. FAN6292BMX/ FAN6292MX support bleeding function by turning on S1 for $T_{BLD-max}$ as shown in Figure 14. The amount of bleeding current through BLD/AUX pin can be controlled by the external resistor R_{BLD} shown in (1).

$$I_{BLD-RType} = \frac{V_{O\_MAX}}{R_{BLD} + R_{Internal}} \quad (1)$$

VIN-UVP Protection(for FAN6292BMX)

Since pure primary side controller detects and regulates output voltage only when switching, it is not easy maintaining output voltage when load suddenly increases from light load where switching frequency is slow to heavy load.Therefore, as Figure 15, FAN6292BMX automatically detects output voltage. When output undershoot is acknowledged via VIN pin, BLD/AUX pin pull-down current via S2 switch to inform undershoot status to primary controller via a photo-coupler. Since the pull-down current is limited through S2, the current will not affect to the amount of output current.

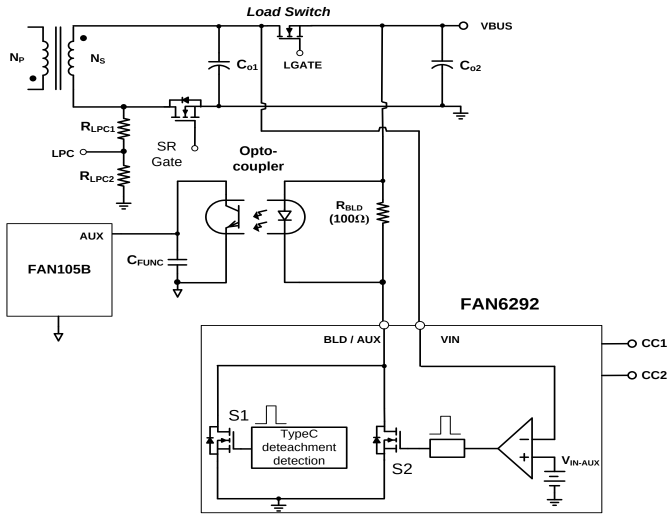


Figure 14 BLD/AUX Function Diagram

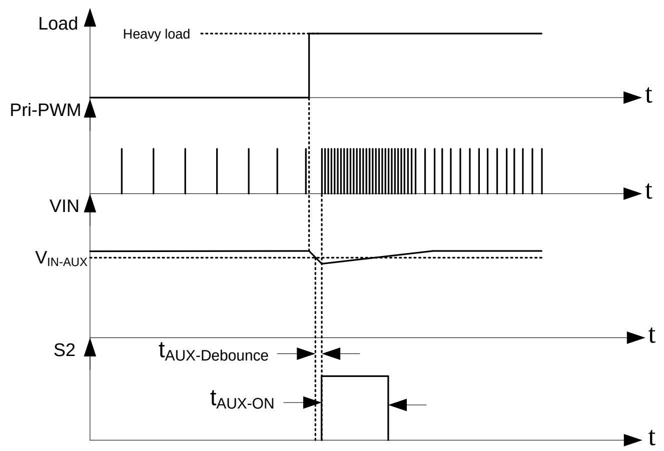
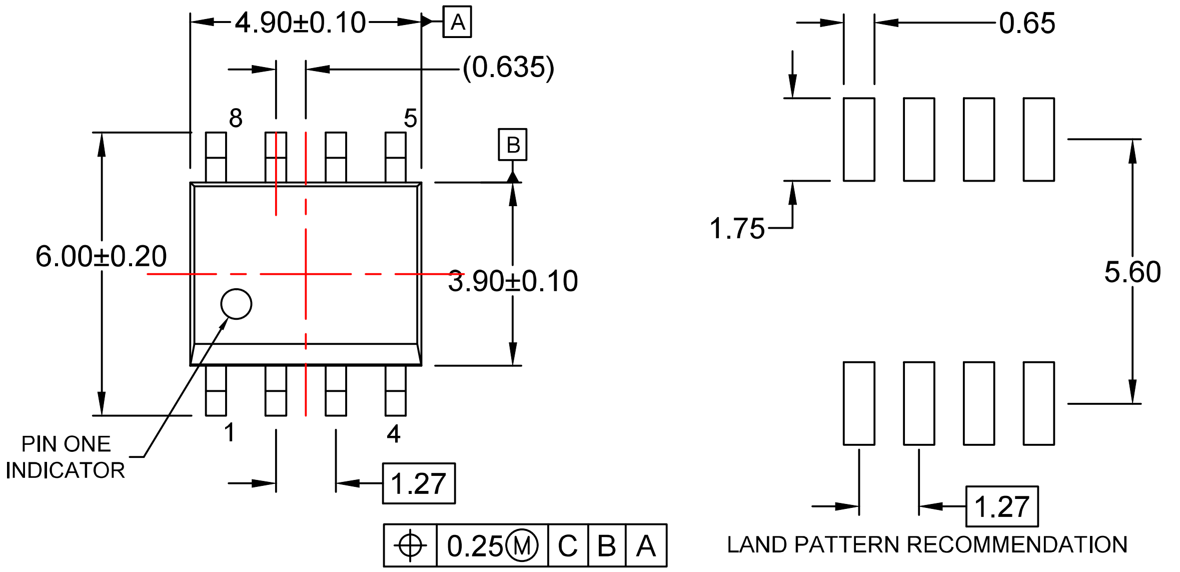


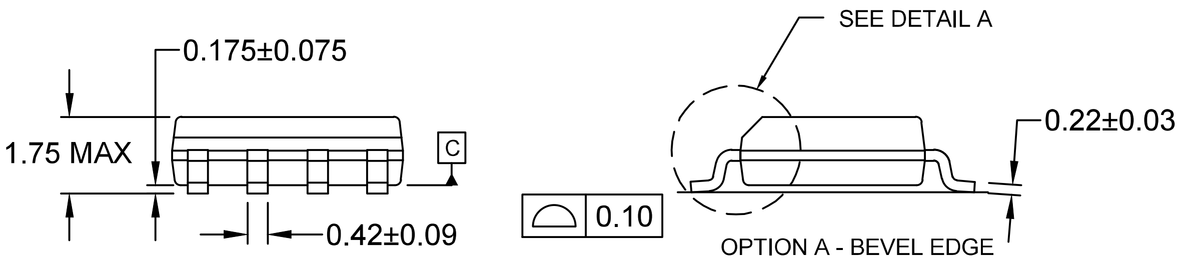
Figure 15 VIN-UVP Protection

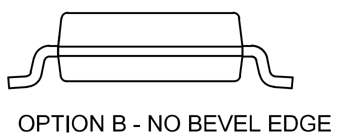
ORDERING INFORMATION

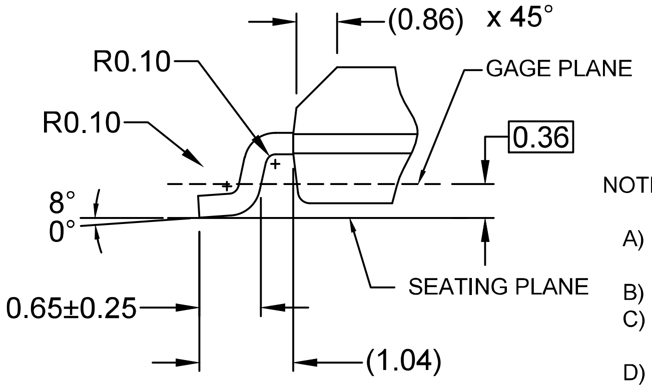
Part Number	Operating Temperature Range	Package	Packing Method
FAN6292BMX	-40°C to +125°C	8-Lead, Small Outline Package (SOIC), JEDEC MS-012, .150-Inch Narrow Body	Tape & Reel
FAN6292MX	-40°C to +125°C	8-Lead, Small Outline Package (SOIC), JEDEC MS-012, .150-Inch Narrow Body	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D









DETAIL A

SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

FAIRCHILD

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