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# FAN6208

## Secondary-Side Synchronous Rectifier Controller for LLC Topology

### Features

- Specialized SR Controller for LLC or LC Resonant Converters
- Secondary-Side Timing Detection with Timing Estimator
- Gate-Shrink Function to Prevent Shoot-Through During Load and Line Transient
- Green-Mode Function for Higher Efficiency at Light-Load Condition
- Programmable Dead Time between Primary-Side Gate Drive Signal and SR Drive Signal
- Advanced Output-Short / Overload Protection Based on the Feedback Information
- Internal Over-Temperature Protection (OTP)
- $V_{DD}$  Pin Over-Voltage Protection (OVP)

### Applications

- LCD TV
- PC Power
- Open-Frame SMPS

### Description

FAN6208 is a synchronous rectification (SR) controller for isolated LLC or LC resonant converters that can drive two individual SR MOSFETs emulating the behavior of rectifier diodes. FAN6208 measures the SR conduction time of each switching cycle by monitoring the drain-to-source voltage of each SR and determines the optimal timing of the SR gate drive. FAN6208 uses the change of opto-coupler diode current to adaptively shrink the duration of SR gate drive signals during load transients to prevent shoot-through. To improve light-load efficiency, Green-Mode operation is employed, which disables the SR drive signals, minimizing gate drive power consumption at light-load condition.

Optimal timing circuits and protection functions are integrated in an 8-pin SOP package, which allows high-efficiency power supply design with fewer components.

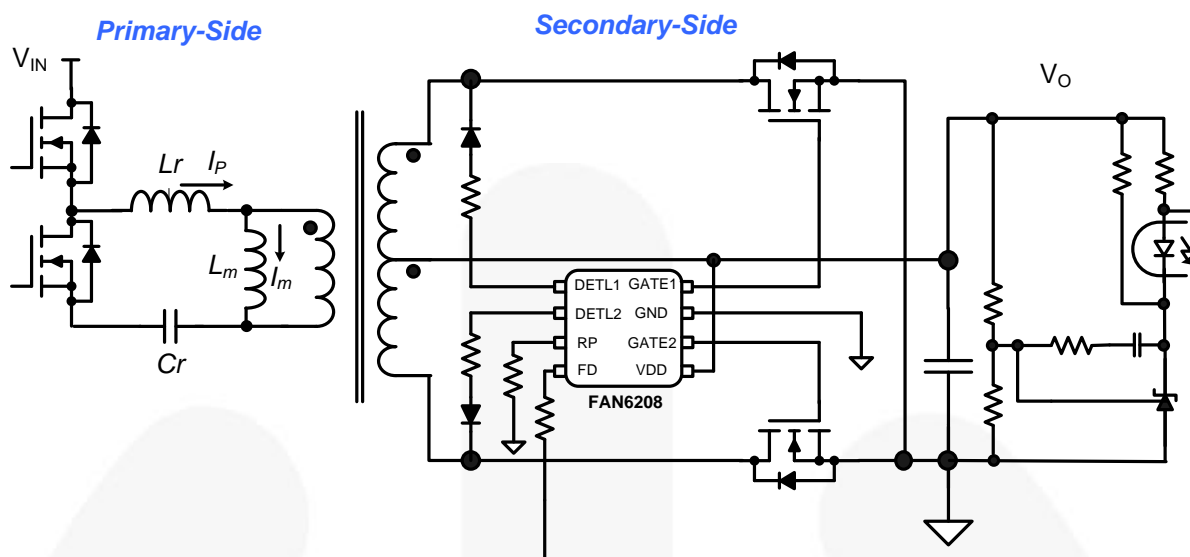
### Related Resources

- [FAN6208 Product Folder](#)

### Ordering Information

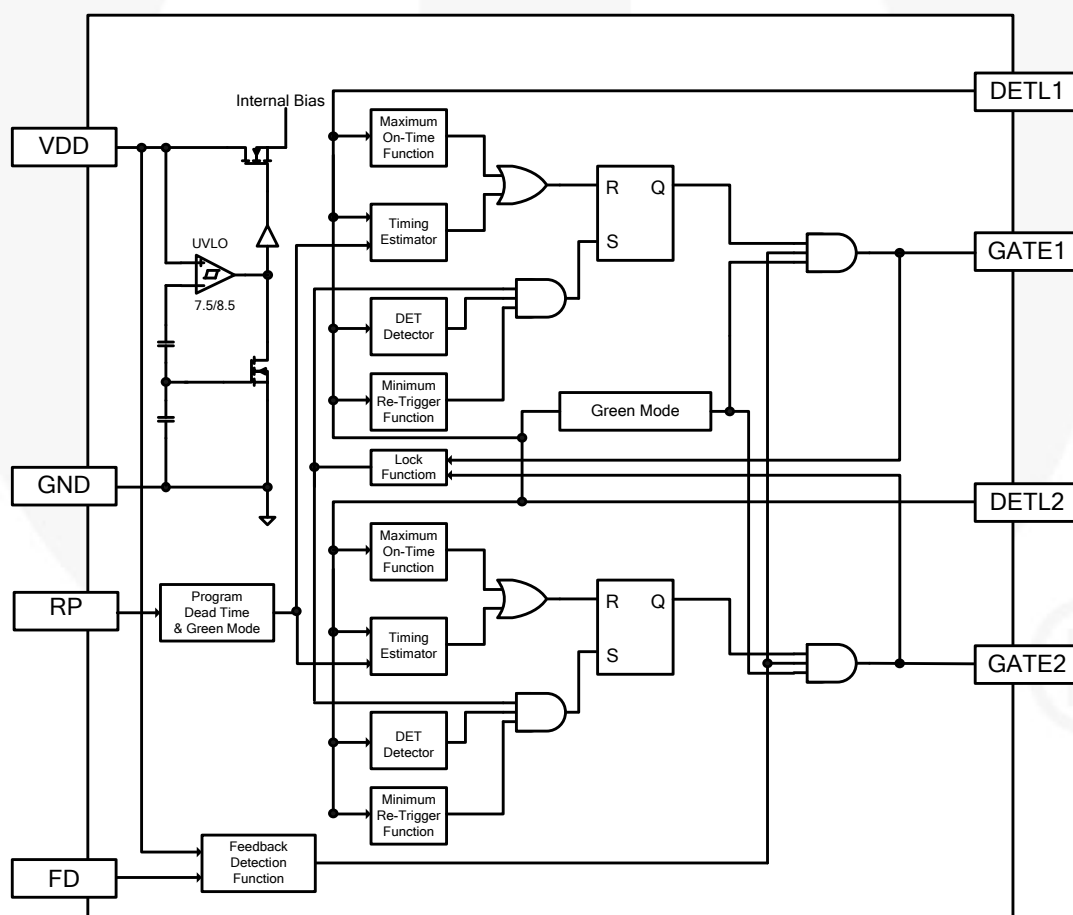
Part Number	Operating Temperature Range	Package	Packing Method
FAN6208MY	-40°C to +105°C	8-Pin Small Outline Package (SOP)	Tape & Reel

## Application Diagram



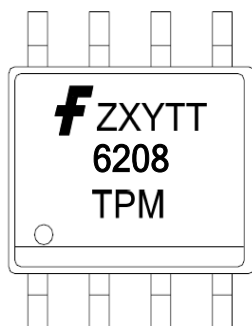
### Figure 1. Typical Application

## Block Diagram



### Figure 2. Block Diagram

## Marking Information



F- Fairchild Logo  
 Z- Plant Code  
 X- Year Code  
 Y- Week Code  
 TT: Die Run Code  
 T - Package Type (M = SOP)  
 P - Y: Green Package  
 M - Manufacture Flow Code

Figure 3. Top Mark

## Pin Configuration

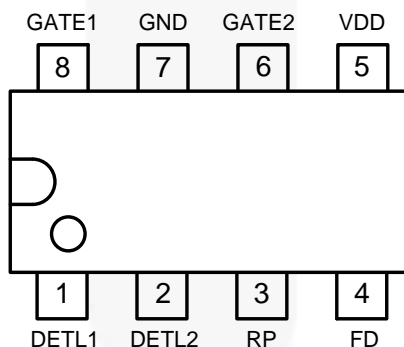


Figure 4. Pin Assignments

## Pin Definitions

Pin #	Name	Description
1	DETL1	<b>Low Detect</b> provides low-voltage detection of $V_{DS}$ of SR MOSFET1.
2	DETL2	<b>Low Detect</b> provides low-voltage detection of $V_{DS}$ of SR MOSFET2.
3	RP	<b>Dead Time Programming Resistor</b> programs H/L frequency version and dead time.
4	FD	<b>Feedback Detection</b> is used for short-circuit protection and gate shrink.
5	VDD	<b>Power Supply</b>
6	GATE2	<b>Driver Output.</b> The totem-pole output driver for driving the SR MOSFET2.
7	GND	<b>Ground</b>
8	GATE1	<b>Driver Output.</b> The totem-pole output driver for driving the SR MOSFET1.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{DD}$	Supply Voltage		30	V
$V_{FD}$	Voltage on FD Pin		30	V
$V_{LV}$	Voltage on DETL1, DETL2, RP Pins	-0.3	7.0	V
$P_D$	Power Dissipation	350 mW at $T_A=90^{\circ}\text{C}$	1000 mW at $T_A=25^{\circ}\text{C}$	
$\Theta_{JA}$	Junction-to-Ambient Thermal Resistance		130	$^{\circ}\text{C/W}$
$\Psi_{JT}$	Junction-to-Top Thermal Characteristics		45	$^{\circ}\text{C/W}$
$T_J$	Operating Junction Temperature	Internally Limited		$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature Range	-55	+150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (Wave Soldering or IR, 10 Seconds)		+260	$^{\circ}\text{C}$
ESD	Human Body Model, JESD22-A114		6	kV
	Charged Device Model, JESD22-C101		2	

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$T_A$	Operating Ambient Temperature	-40	+105	$^{\circ}\text{C}$

## Electrical Characteristics

$V_{DD}=20\text{ V}$ ,  $T_A=25^\circ\text{C}$ , unless otherwise specified. All voltages are with respect to GND unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>VDD Section</b>						
$V_{DD}$	DC Supply Voltage		$V_{TH-OFF}$		28	V
$I_{DD-OP1}$	Operating Current	$V_{DD}=12\text{ V}$ , DETL=50 KHz, $C_L=6\text{ nF}$ , $R_{RP}=24\text{ K}\Omega$	7.0	8.5	10.0	mA
$I_{DD-OP2}$	Operating Current	$V_{DD}=12\text{ V}$ , DETL=100 KHz	2.4	3.2	4.0	mA
$I_{DD-ST}$	Startup Current	$V_{DD}=8\text{ V}$	180	300	500	$\mu\text{A}$
$V_{TH-ON1}$ $V_{TH-ON2}$	On Threshold Voltage		9.3	9.7	10.1	V
$V_{TH-OFF1}$ $V_{TH-OFF2}$	Off Threshold Voltage		8.3	8.8	9.3	V
$V_{DD-OVP1}$ $V_{DD-OVP2}$	$V_{CC}$ Over-Voltage Protection		26	27	28	V
$V_{DD-OVP-HYS1}$ $V_{DD-OVP-HYS2}$	$V_{CC}$ Over-Voltage Protection Hysteresis		1.3	1.8	2.3	V
$t_{OVP1}, t_{OVP2}$	$V_{CC}$ Over-Voltage-Protection Debounce		30	60	100	$\mu\text{s}$
<b>DETL Section</b>						
$V_{DETL1}$ $V_{DETL2}$	Threshold Voltage for LOW Detection of DETL	$V_{DD}=12\text{ V}$ , DETL=50 KHz, $C_L=6\text{ nF}$ , $R_{RP}=24\text{ K}\Omega$	1.7	2.0	2.3	V
$t_{SR-ON-DETL1}$ $t_{SR-ON-DETL2}$	Delay from DETL LOW to SR Gate Turn-On	$t_{DB} + t_{PD} + t_R$	300	350	400	ns
$V_{DETL-FLOATING1}$ $V_{DETL-FLOATING2}$	DETL Floating Voltage	$V_{DD}=12\text{ V}$ , DETL Pin Floating	4.5			V
$I_{DETL-SOURCE1}$ $I_{DETL-SOURCE2}$	DETL Source Current	$V_{DETL1}=0\text{ V}$	40	50	60	$\mu\text{A}$
$t_{DETL\_Green\_LF1}$ $t_{DETL\_Green\_LF2}$	DETL LOW Time Threshold for Green Mode at Low-Frequency Operation	$V_{RP} < 1.5\text{ V}$	3.50	3.75	4.00	$\mu\text{s}$
$t_{DET(L)\_Green\_HF1}$ $t_{DET(L)\_Green\_HF2}$	DETL LOW Time Threshold for Green Mode at High-Frequency Operation	$V_{RP} > 1.5\text{ V}$	1.75	1.90	2.05	$\mu\text{s}$
<b>Thermal Shutdown</b>						
$T_{SHUTDOWN}$	Shutdown Temperature	Temperature Rising, $V_{DD}=15\text{ V}$		140		$^\circ\text{C}$
	Hysteresis			20		
$T_{STARTUP}$	Startup Temperature	Before Startup		120		

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## Electrical Characteristics

$V_{DD}=20\text{ V}$ ,  $T_A=25^\circ\text{C}$ , unless otherwise specified. All voltages are with respect to GND unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Gate Section</b>						
$V_{Z1}\ V_{Z2}$	Gate Output Voltage Maximum (Clamping)	$V_{DD}=20\text{ V}$	10	12	14	V
$V_{OL1}\ V_{OL2}$	Gate Output Voltage LOW	$V_{DD}=12\text{ V}$ ; $I_O=100\text{ mA}$			0.5	V
$V_{OH1}\ V_{OH2}$	Gate Output Voltage HIGH	$V_{DD}=12\text{ V}$ ; $I_O=100\text{ mA}$	9			V
$t_{R1}\ t_{R2}$	Rising Time	$V_{DD}=12\text{ V}$ ; $C_L=6\text{ nF}$ ; $V_{GATE}=2\text{ V to }9\text{ V}$	30	70	120	ns
$t_{F1}\ t_{F2}$	Falling Time	$V_{DD}=12\text{ V}$ ; $C_L=6\text{ nF}$ ; $V_{GATE}=9\text{ V to }2\text{ V}$	30	50	70	ns
$t_{PD\_HIGH\_DETL1}$ $t_{PD\_HIGH\_DETL2}$	Propagation Delay to Gate Output HIGH (DETL Trigger)	$t_R: 0\text{ V}\sim 2\text{ V}$ , $V_{DD}=12\text{ V}$ (DET Floating)		120		ns
$t_{PD\_LOW\_DETL1}$ $t_{PD\_LOW\_DETL2}$	Propagation Delay to Gate Output LOW (DETL Trigger)	$t_F: 100\%\sim 90\%$ , $V_{DD}=12\text{ V}$ (DET Floating)		120		ns
$t_{ON\_MAX1}$ $t_{ON\_MAX2}$	Maximum On-Time	Trim Maximum On-Time	9.0	10.5	12.0	$\mu\text{s}$
$t_{INHIBIT\_LF1}$ $t_{INHIBIT\_LF2}$	Gate Inhibit Time (from Turn-Off to Next Turn-On)	$V_{RP} < 1.5\text{ V}$	1.8	2.1	2.5	$\mu\text{s}$
$t_{INHIBIT\_HF1}$ $t_{INHIBIT\_HF2}$	Gate Inhibit Time (from Turn-Off to Next Turn-On)	$V_{RP} > 1.5\text{ V}$	1.25	1.45	1.70	$\mu\text{s}$
$t_{BLANKING1}$ $t_{BLANKING2}$	Blanking Time for SR Turn-Off Triggered by DETL High (Minimum On-Time)			300		ns
$K_R$	Gate ON-Time Increase Rate Between Two Consecutive Cycles	$t_{ON}(n) / t_{ON}(n-1) \%$		140		%
<b>Timing Estimator Section</b>						
$t_{DW}$	Detection Window for Insufficient Dead Time (from Gate Turn-Off to DETL HIGH)		80	125	150	ns
$t_{SHRINK-DT}$	Gate Shrink Time by Insufficient Dead Time	$R_{RP}=20\text{ K}\Omega$ , $t_{DETL}=5\text{ }\mu\text{s}$	1.00	1.25	1.50	$\mu\text{s}$
$t_{DEAD}$	Dead Time by Timing Estimator (70 kHz ~ 140 kHz, $V_{RP} < 1.5\text{ V}$ )	$t_{DETL}=4\text{ }\mu\text{s}$ , $R_{RP}=20\text{ K}\Omega$	210	300	390	ns
		$t_{DETL}=6\text{ }\mu\text{s}$ , $R_{RP}=20\text{ K}\Omega$	570	720	870	
	Dead Time by Timing Estimator (160kHz ~ 240 kHz, $V_{RP} > 1.5\text{ V}$ )	$t_{DETL}=2.5\text{ }\mu\text{s}$ , $R_{RP}=43\text{ K}\Omega$	220	320	420	
		$t_{DETL}=3.8\text{ }\mu\text{s}$ , $R_{RP}=43\text{ K}\Omega$	560	670	780	
$t_{DB}$	DETL HIGH-to-LOW Debounce Time for Gate Turn-on Trigger			150		ns
$t_{SHRINK-RNG}$	Gate Shrink by DETL Ringing around Zero			1.2		$\mu\text{s}$
$t_{Green\_DH}$	DETL Pull-HIGH Time Threshold for Green Mode		18	24	30	$\mu\text{s}$

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## Electrical Characteristics

$V_{DD}=20\text{ V}$ ,  $T_A=25^\circ\text{C}$ , unless otherwise specified. All voltages are with respect to GND unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Feedback Detection (FD) Section</b>						
$\Delta V1\% \Delta V2\%$	Feedback Increase Threshold for Gate Shrink	$[(V_{DD}-V_{FD})_{n+1}/(V_{DD}-V_{FD})_n]$		120		%
$t_{SHRINK-FD}$	Gate Shrink by Feedback Detection			1.4		$\mu\text{s}$
$t_{D-SHRINK-FD}$	Gate-Shrink Duration by Feedback Detection		60	90	120	$\mu\text{s}$
$V_{DD}-V_{FD,SCP}$	Short-Circuit Protection (SCP) Threshold by Feedback Detection		200	270	340	mV
$t_{DB-SCP}$	Debounce Time for Short-Circuit Protection (SCP)		12	16	20	$\mu\text{s}$
<b>RP Section</b>						
$I_{RP}$	RP Source Current		38.5	41.5	44.5	$\mu\text{A}$
$V_{RPO}$	RP Open Protect		3.40	3.65	3.90	V
$V_{RPS}$	RP Short Protect		0.25	0.30	0.35	V
$t_{RPOS}$	RP Open/Short Debounce		1.6	2.0	2.4	$\mu\text{s}$
$V_{RPHL}$	H/L Frequency Threshold		1.40	1.46	1.52	V

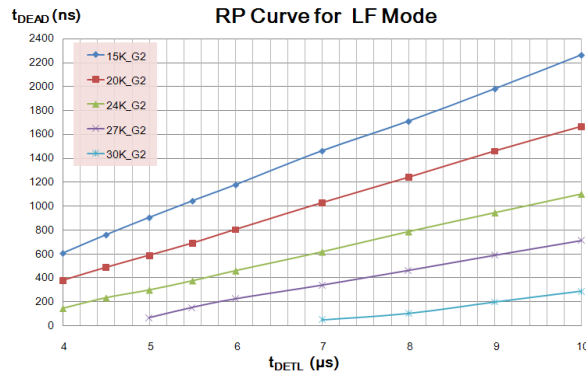


Figure 5.  $t_{DEAD}$  vs.  $t_{DETL}$  RP Curve for LF Mode

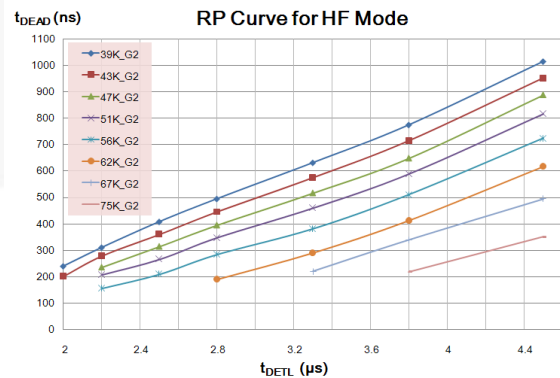


Figure 6.  $t_{DEAD}$  vs.  $t_{DETL}$  RP Curve for HF Mode



## Function Description

### Operation Principle

FAN6208 is a secondary-side synchronous rectifier controller for LLC or LC resonant converters that drive two synchronous rectifier MOSFETs. Figure 7 is the simplified circuit diagram of an LLC converter. The FAN6208 determines SR MOSFET turn-on/off timing by detecting the drain-to-source voltage of each SR MOSFET. The key waveforms for LLC resonant converter for below resonance and above resonance are shown in Figure 8 and Figure 9, respectively.

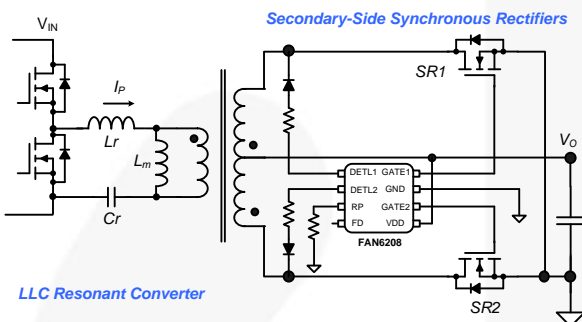


Figure 7. Simplified Schematic of LLC Converter

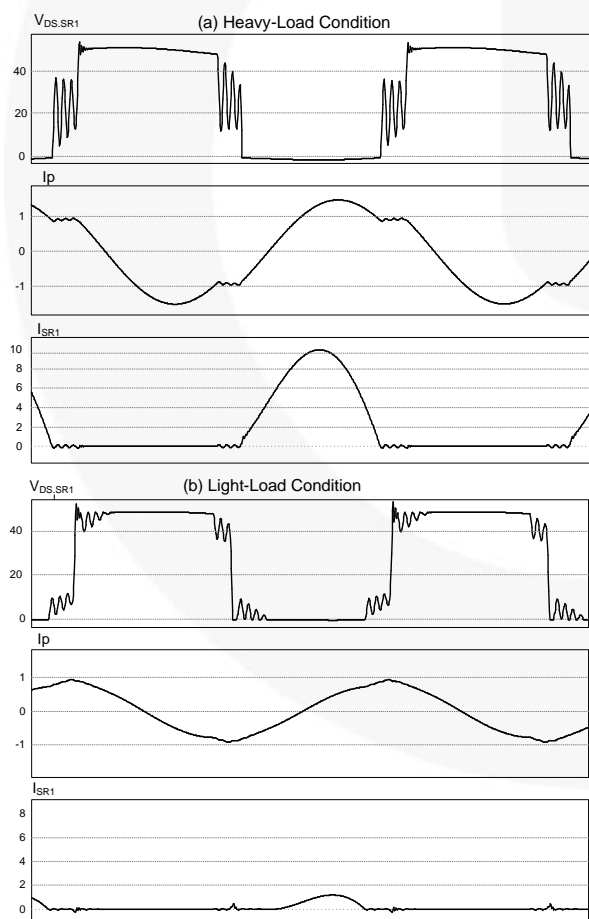


Figure 8. Key Waveforms of LLC Resonant Converter for Below Resonance Operation

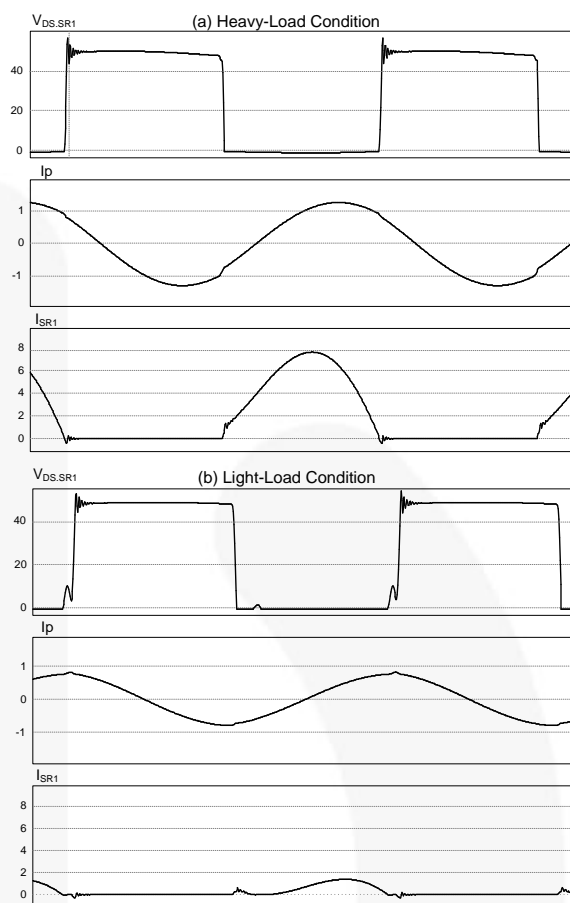


Figure 9. Key Waveforms of LLC Resonant Converter for Above Resonance Operation

### Timing Estimator

Figure 10 shows the timing diagram for FAN6208. Once the body diode of SR begins conducting, the drain-to-source voltage drops to zero, which causes DETL pin voltage to drop to zero. FAN6208 turns on the MOSFET after  $t_{ON-ON-DETL}$  (about 350 ns), when voltage on DETL drops below 2 V. As depicted in Figure 11, the turn-on delay (after  $t_{SR-ON-DETL}$ ) is the sum of debounce time (150 ns) and propagation delay (200 ns).

FAN6208 measures the SR conduction duration ( $t_{DETL}$ ), during which DETL stays lower than 2 V, and uses this information to determine the turn-off instant of SR gates of the next switching cycle. The turn-off timing is obtained by subtracting a dead time ( $t_{DEAD}$ ) from the measured SR conduction duration of the previous switching cycle. The dead time can be programmed using a resistor on the RP pin and the relationship between the dead time and SR conduction duration ( $t_{DETL}$ ) for different resistor values on RP pin is given in Figure 5.

The figure displays four timing diagrams for DETL1 and GATE1 signals. Each diagram shows the relationship between the gate signal (GATE1) and the detector output (DETL1).

- Top Diagram:** Shows a single pulse on GATE1 with a duration of 150ns (t<sub>DB</sub>) followed by a delay of 200ns (t<sub>PD</sub>). The DETL1 signal shows a single sharp peak. The time from the start of the gate pulse to the peak is labeled t<sub>SR-ON-DETL</sub>. The peak voltage is 2V, and the baseline is V<sub>DETL1</sub>. The pulse width is 350ns.
- Second Diagram:** Shows a single pulse on GATE1 with a duration of 150ns (t<sub>DB</sub>) followed by a delay of 200ns (t<sub>PD</sub>). The DETL1 signal shows a single sharp peak. The time from the start of the gate pulse to the peak is labeled t<sub>SR-ON-DETL</sub>. The peak voltage is 2V, and the baseline is V<sub>DETL1</sub>. The pulse width is 350ns.
- Third Diagram:** Shows a single pulse on GATE1 with a duration of 150ns (t<sub>DB</sub>) followed by a delay of 200ns (t<sub>PD</sub>). The DETL1 signal shows a single sharp peak. The time from the start of the gate pulse to the peak is labeled t<sub>SR-ON-DETL</sub>. The peak voltage is 2V, and the baseline is V<sub>DETL1</sub>. The pulse width is 350ns.
- Bottom Diagram:** Shows a single pulse on GATE1 with a duration of 150ns (t<sub>DB</sub>) followed by a delay of 200ns (t<sub>PD</sub>). The DETL1 signal shows a single sharp peak. The time from the start of the gate pulse to the peak is labeled t<sub>SR-ON-DETL</sub>. The peak voltage is 2V, and the baseline is V<sub>DETL1</sub>. The pulse width is 350ns.

The diagram shows two waveforms:  $V_{DET}$  (top) and  $V_{GATE}$  (bottom). The  $V_{DET}$  signal has a series of pulses, with the first one labeled  $2V$ . The  $V_{GATE}$  signal has corresponding rectangular pulses. A horizontal dashed line represents a threshold level. A shaded region between the two signals is labeled "125ns Detection window". The duration of the first  $V_{GATE}$  pulse is labeled  $t_{DET\_LOW}(n-1) - t_{DEAD}$ . The duration of the second  $V_{GATE}$  pulse is labeled  $t_{DET\_LOW}(n) - t_{DEAD} - t_{SHRINK}$ . The duration of the third  $V_{GATE}$  pulse is labeled  $t_{DET\_LOW}(n+1)$ . An arrow labeled "Shrink" points to the right, indicating the reduction in the detection window over time.

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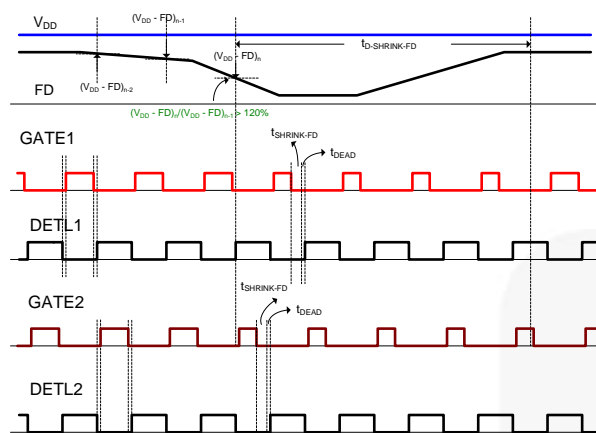


Figure 14. Gate Shrink by Feedback Detection

- (c) When the DETL voltage has ringing around zero. As depicted in Figure 8, the drain voltage of SR has ringing around zero at light-load condition after the switching transition of the primary-side switches. When DETL voltage rises above 2 V within 350 ns after DETL voltage drops to zero and stays above 2 V longer than 150 ns, the gate is shrunk by 1.2  $\mu$ s ( $t_{SHRINK-RNG}$ ), as shown in Figure 15.

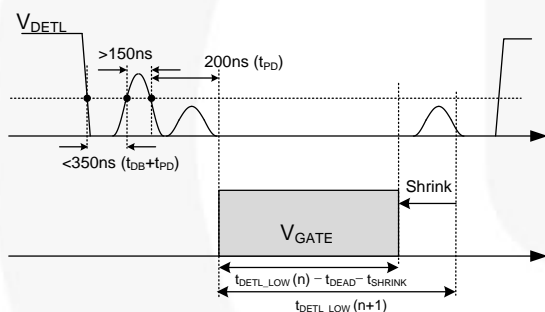


Figure 15. Gate Shrink by DETL Voltage Ringing Around Zero

## RP Pin Function

The RP pin programs the level of green mode and  $t_{DEAD}$ . Figure 16 shows how the mode is selected by the voltage on the RP pin (open protection, short protection, and HF/LF mode). When  $R_{RP}$  is less than 36 K $\Omega$ , FAN6208 operates in low-frequency mode. Green mode is enabled when  $t_{DETL}$  is smaller than 3.75  $\mu$ s. When  $R_{RP}$  is larger than 36 K $\Omega$ , high-frequency mode is selected and green mode is enabled for  $t_{DETL} < 1.90 \mu$ s.  $t_{DEAD}$  can be also adjusted by a resistor on the RP pin. Figure 5 shows the relationship between  $t_{DEAD}$  and  $t_{DETL}$  for different RP resistors.

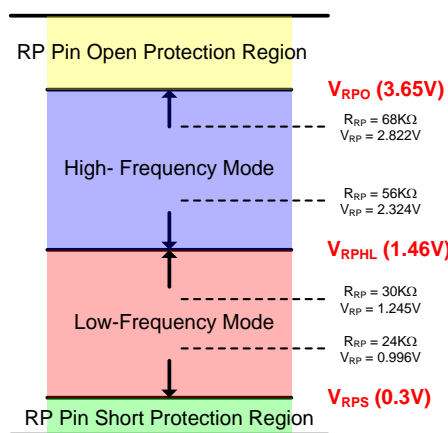


Figure 16. RP Pin Operation

To handle abnormal conditions for IC pins, the RP pin also provides open/short protection. When  $V_{RP}$  is less than  $V_{RPS}$  (0.3 V) or  $V_{RP}$  is higher than  $V_{RPO}$  (3.65 V), the protection is triggered. Figure 17 shows the RP pin short protection timing sequence. If  $V_{RP} < V_{RPS}$  (0.3 V) for longer than  $t_{RPOS}$  (2  $\mu$ s), FAN6208 is disabled. Figure 18 shows the RP pin open protection timing sequence. If  $V_{RP} > V_{RPO}$  (3.65 V) for longer than  $t_{RPOS}$  (2  $\mu$ s), FAN6208 is disabled.

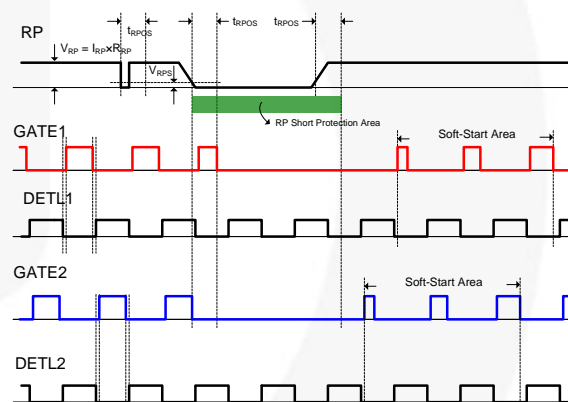


Figure 17. RP Pin Short Protection

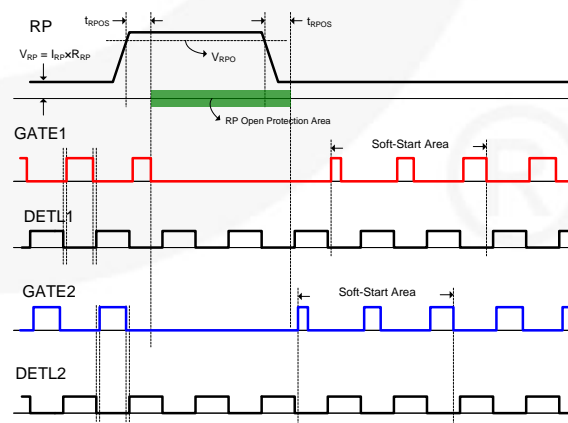


Figure 18. RP Pin Open Protection

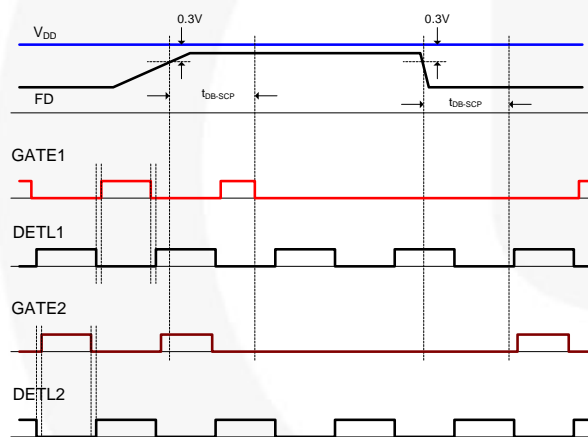
## Green Mode

Switching frequency increases in LLC topology at light-load condition, which increases the power consumption for the SR gate drive. Green mode reduces power loss at light load. FAN6208 has two ways to enable green mode. Green mode is triggered when DETL voltage is pulled LOW for less than 3.75  $\mu\text{s}$  (LF mode) or 1.90  $\mu\text{s}$  (HF mode) for seven switching cycles. FAN6208 resumes normal SR gate driving when DETL voltage is pulled LOW for longer than 3.75  $\mu\text{s}$  (LF mode) or 1.90  $\mu\text{s}$  (HF mode) for seven switching cycles.

When DETL voltage is pulled HIGH for longer than 24  $\mu\text{s}$ . This occurs when the LLC resonant converter operates in burst mode (skipping mode).

## Short-Circuit Protection

As depicted in Figure 13, FAN6208 monitors the current through the opto-coupler diode by measuring the voltage across the resistor in series with the opto-coupler diode. When the output of the power supply is short circuited, the output voltage drops and the cathode of the shunt regulator (KA431) is saturated to HIGH. No current flows through the opto coupler diode. The output short protection is triggered when the voltage between  $V_{DD}$  and FD is smaller than 0.3 V, as shown in Figure 19.



**Figure 19. Output Short Protection by Feedback Detection**

## $V_{DD}$ Pin Over-Voltage Protection

Over-voltage conditions are usually caused by an open feedback loop.  $V_{DD}$  over-voltage protection prevents damage of SR MOSFET. When the voltage on the  $V_{DD}$  pin exceeds 27 V, FAN6208 disables gate output.

## Internal Over-Temperature Protection

Internal over-temperature protection prevents the SR gate from fault triggering in high temperatures. If the temperature is over 140°C, the SR gate is disabled until the temperature drops below 120°C.

## Typical Performance Characteristics

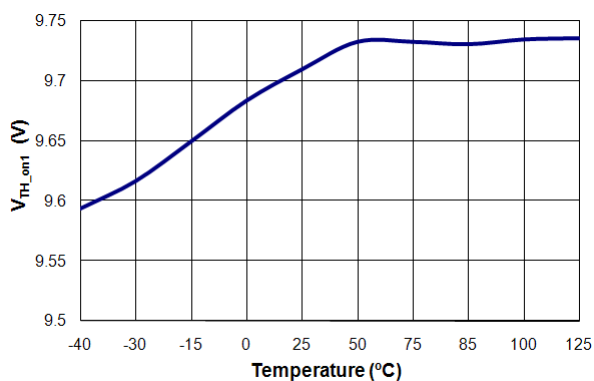


Figure 20.  $V_{TH\_ON1}$  vs.  $T_A$

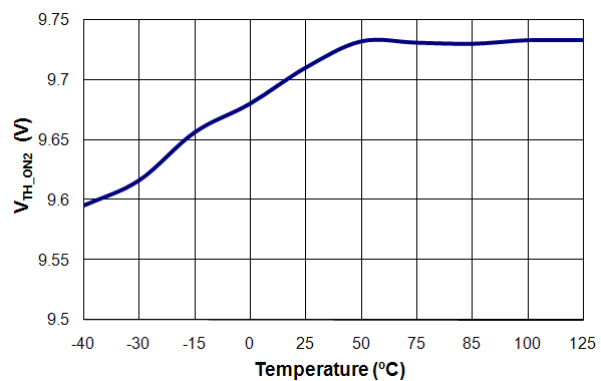


Figure 21.  $V_{TH\_ON2}$  vs.  $T_A$

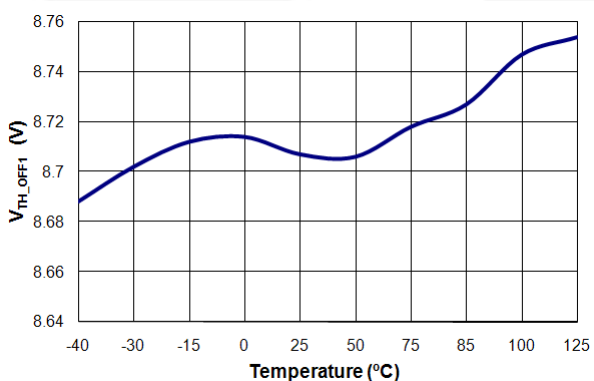


Figure 22.  $V_{TH\_OFF1}$  vs.  $T_A$

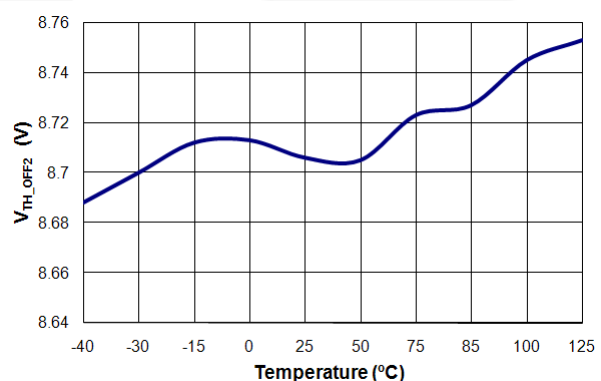


Figure 23.  $V_{TH\_OFF2}$  vs.  $T_A$

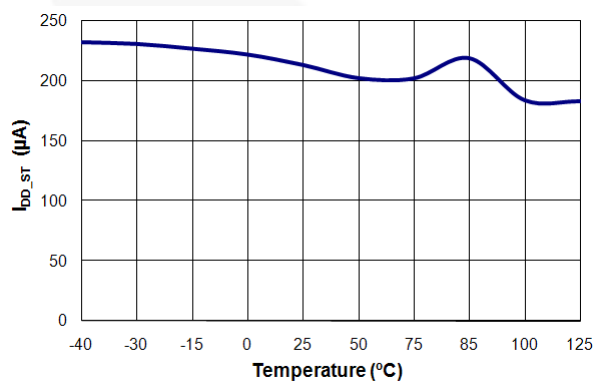


Figure 24.  $I_{DD\_ST}$  vs.  $T_A$

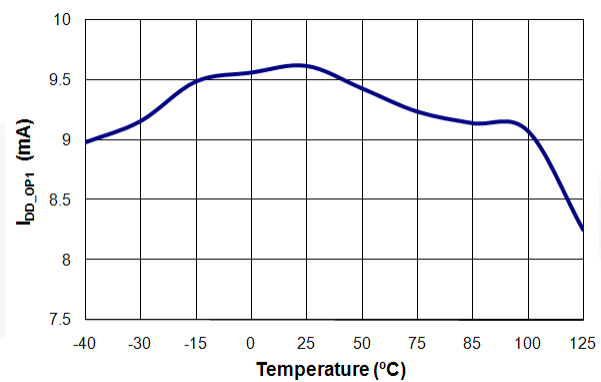


Figure 25.  $I_{DD\_OP1}$  vs.  $T_A$

## Typical Performance Characteristics (Continued)

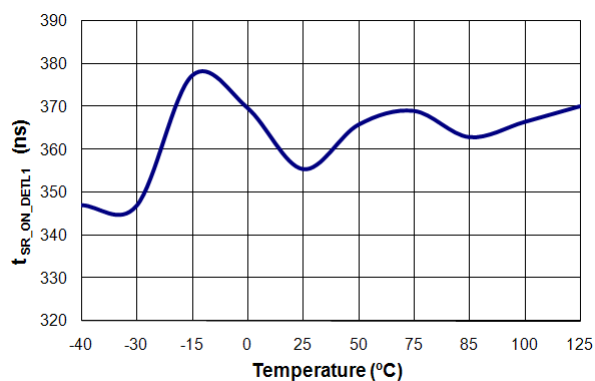


Figure 26.  $t_{SR\_ON\_DET1}$  vs.  $T_A$

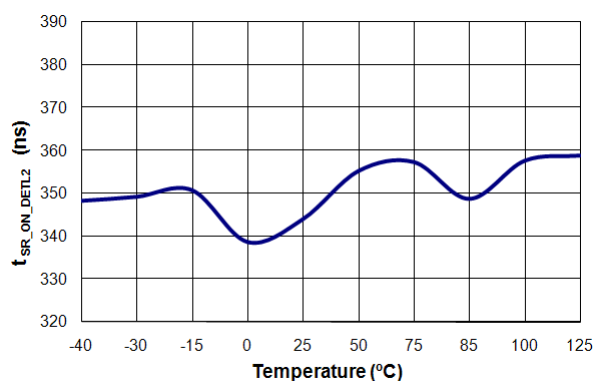


Figure 27.  $t_{SR\_ON\_DET2}$  vs.  $T_A$

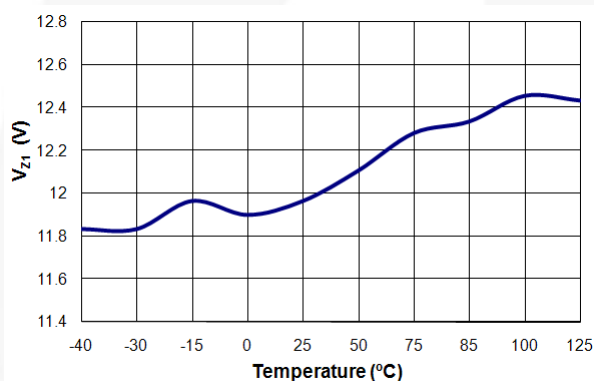


Figure 28.  $V_{Z1}$  vs.  $T_A$

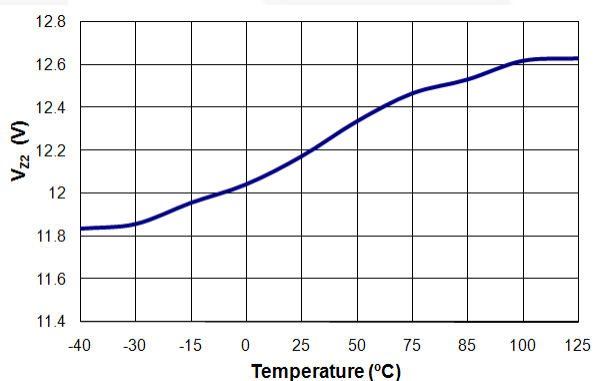


Figure 29.  $V_{Z2}$  vs.  $T_A$

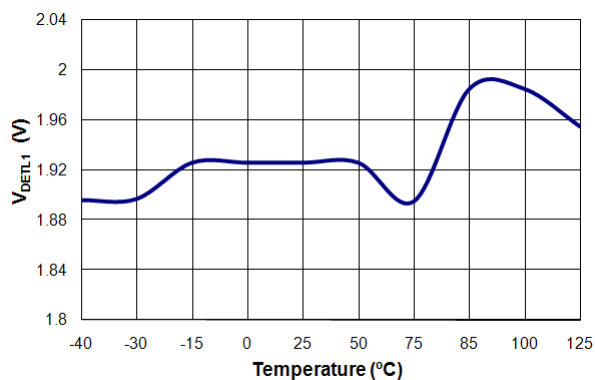


Figure 30.  $V_{DET1}$  vs.  $T_A$

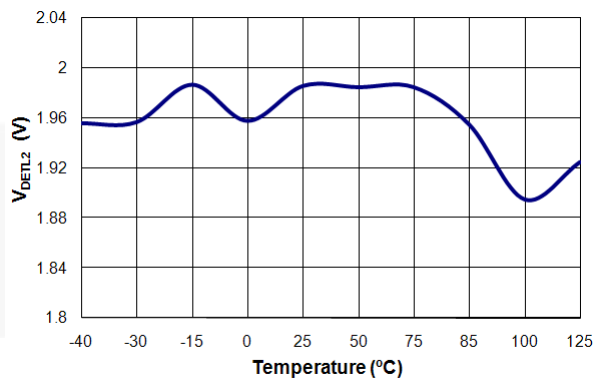


Figure 31.  $V_{DET2}$  vs.  $T_A$

## Typical Performance Characteristics (Continued)

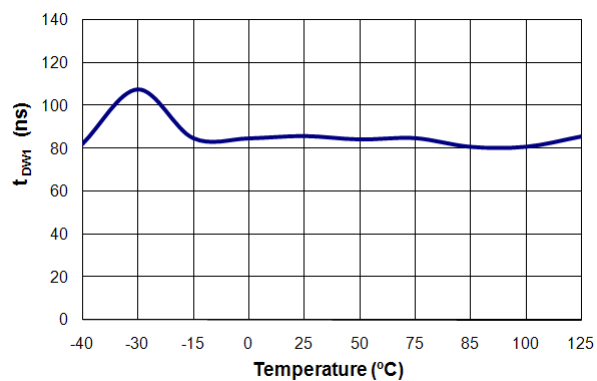


Figure 32.  $t_{DW1}$  vs.  $T_A$

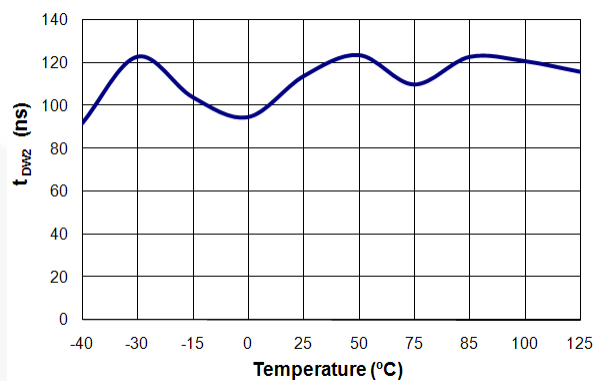


Figure 33.  $t_{DW2}$  vs.  $T_A$

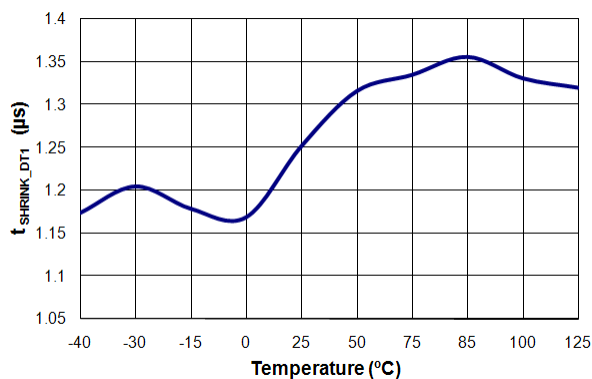


Figure 34.  $V_{SHRINK\_DT1}$  vs.  $T_A$

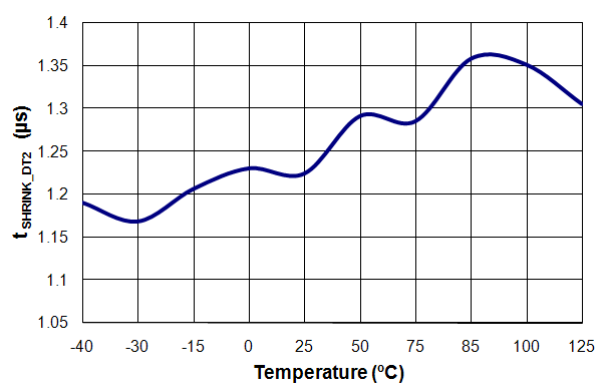


Figure 35.  $V_{SHRINK\_DT2}$  vs.  $T_A$

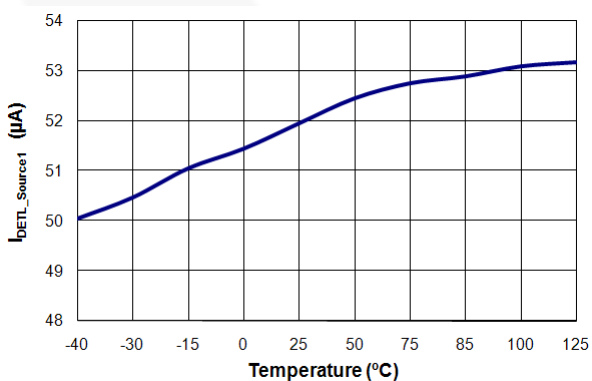


Figure 36.  $I_{DET\_Source1}$  vs.  $T_A$

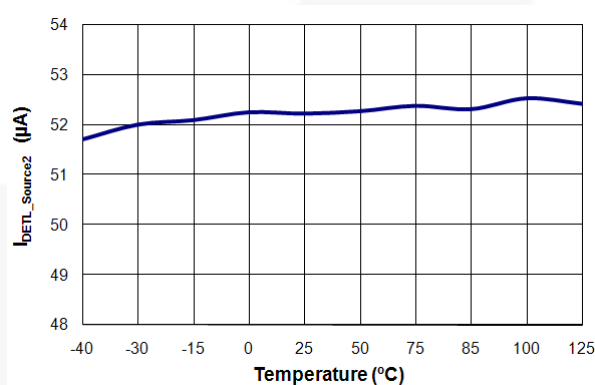


Figure 37.  $I_{DET\_Source2}$  vs.  $T_A$

## Typical Performance Characteristics (Continued)

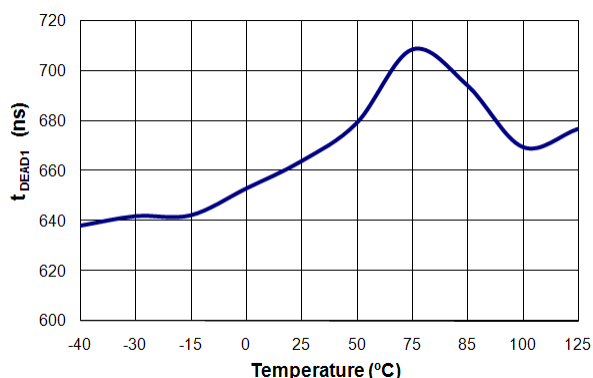


Figure 38.  $t_{\text{DEAD1}}$  ( $R_{\text{RP}}=20 \text{ k}$ ,  $6 \mu\text{s}$ ) vs.  $T_A$

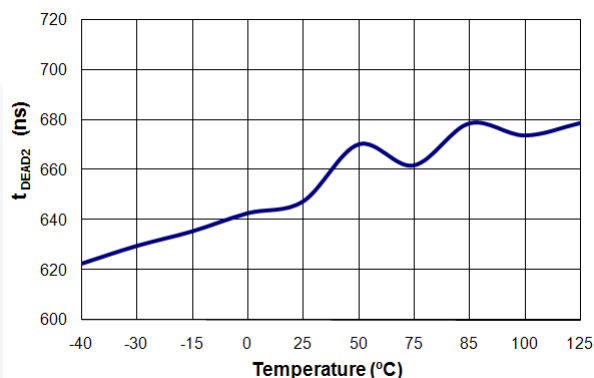


Figure 39.  $t_{\text{DEAD2}}$  ( $R_{\text{RP}}=20 \text{ k}$ ,  $6 \mu\text{s}$ ) vs.  $T_A$

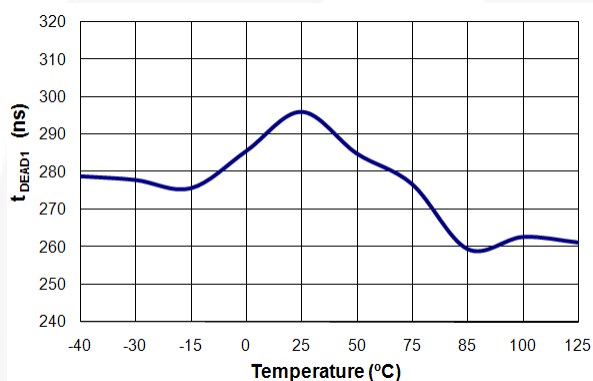


Figure 40.  $t_{\text{DEAD1}}$  ( $R_{\text{RP}}=43 \text{ k}$ ,  $2.5 \mu\text{s}$ ) vs.  $T_A$

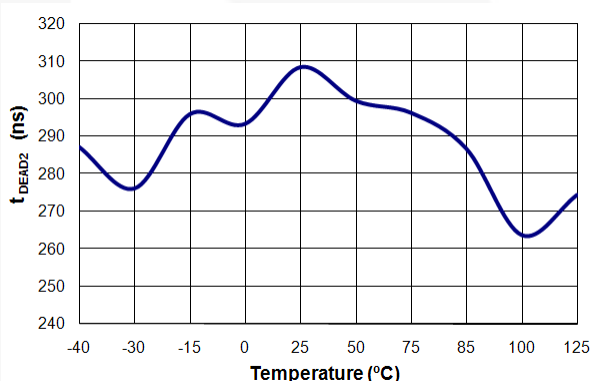


Figure 41.  $t_{\text{DEAD2}}$  ( $R_{\text{RP}}=43 \text{ k}$ ,  $2.5 \mu\text{s}$ ) vs.  $T_A$

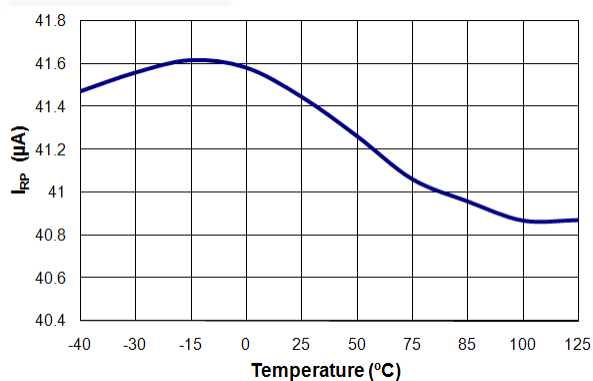


Figure 42.  $I_{\text{RP}}$  vs.  $T_A$

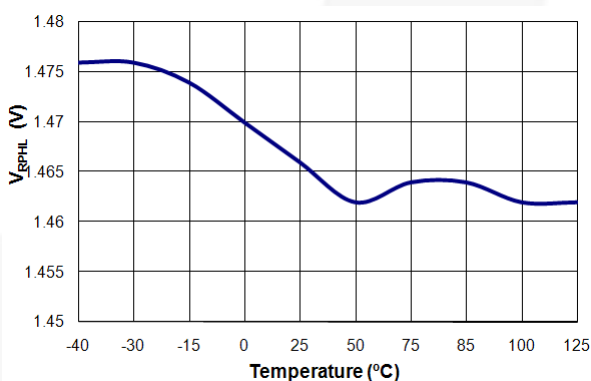


Figure 43.  $V_{\text{RPHL}}$  vs.  $T_A$



# Typical Application Circuit (LLC Converter with SR)

Application	Fairchild Devices	Input Voltage Range	Output
TV Power	FAN7621 FAN6208	350~400 V <sub>DC</sub>	24 V / 8 A

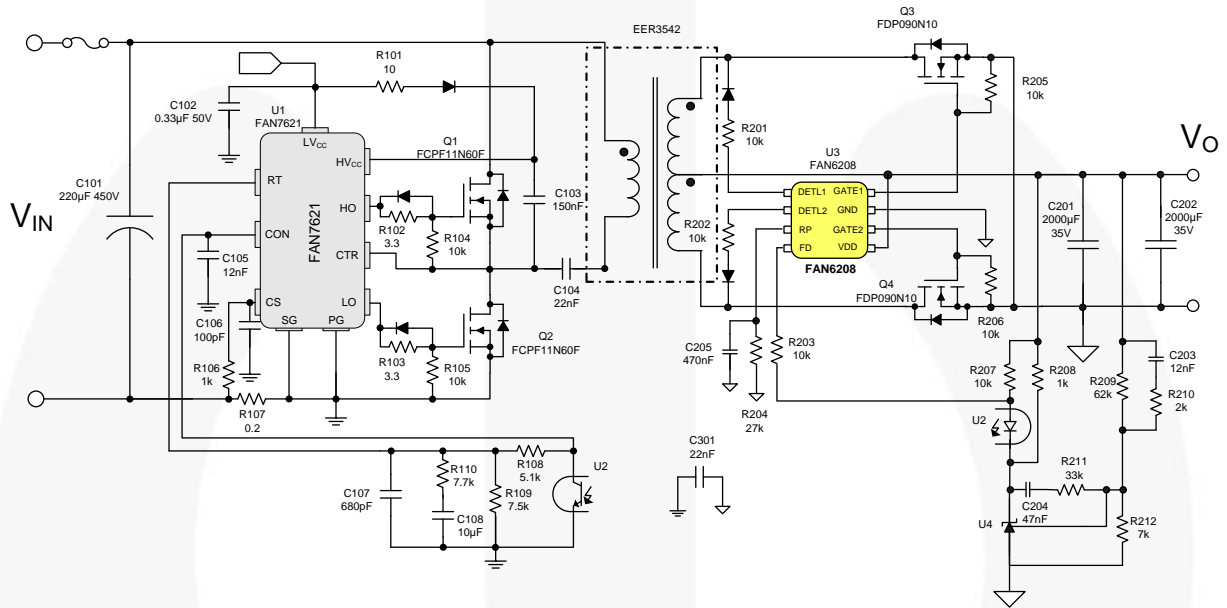
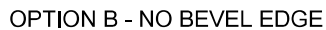
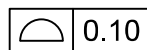
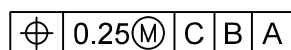


Figure 44. Application Circuit



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16

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