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June 2016

FAN602L
Offline Quasi-Resonant PWM Controller

Features

- High Efficiency Across Wide Input and Output Conditions in a Small Form Factor
- Quasi-Resonant Switching Operation with Programmable Maximum Blanking Frequency Range (60 kHz~ 140 kHz)
- User Configurable Burst Mode Entry and Exit to Maximize Light Load Efficiency and Minimize Audible Noise
- Adaptive Burst Mode Entry Level for Adaptive Charger Application
- mWSaver® Technology for Ultra Low Standby Power Consumption (<20 mW)
- Forced and Inherent Frequency Modulation of Valley Switching for Low EMI Emissions and Common Mode Noise
- Built-In and User Configurable Over-Voltage Protection (OVP), Under-Voltage Protection (UVP) and Over-Temperature Protection (OTP)
- Fully Programmable Brown-In and Brownout Protection
- Precise Constant Output Current Regulation with Programmable Line Compensation
- Built-In High-Voltage Startup to Reduce External Components
- 10 Lead SOIC JEDEC

Applications

- Battery Charges for Smart Phones, Feature Phones, and Tablet PCs
- AC-DC Adapters for Portable Devices or Battery Chargers that Require CV/CC Control

Description

The FAN602L is an advanced PWM controller aimed at achieving power density of ≥10W/in³ in universal input range AC/DC flyback isolated power supplies. It incorporates Quasi-Resonant (QR) control with proprietary Valley Switching with a limited frequency variation. QR switching provides high efficiency by reducing switching losses while Valley Switching with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

FAN602L features mWSaver® burst mode operation with extremely low operating current (300 µA) and significantly reduces standby power consumption to meet the most stringent efficiency regulations such as Energy Star's 5-Star Level and CoC Tier II specifications.

FAN602L includes several user configurable features aimed at optimizing efficiency, EMI and protections. FAN602L has a programmable blanking frequency range that provides flexibility in choosing noise rejection in targeted frequency zones. It incorporates user-configurable minimum peak current, which allows controlling the burst mode entry/exit power level, thereby enhancing light load efficiency and eliminating audible noise. It also includes several rich programmable protection features such as over-voltage protection (OVP), precise constant output current regulation (CC).

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN602LMX	-40°C to +125°C	10-Lead, Small Outline Package (SOIC), JEDEC MS-012, .150-Inch Narrow Body	Tape & Reel

Typical Application

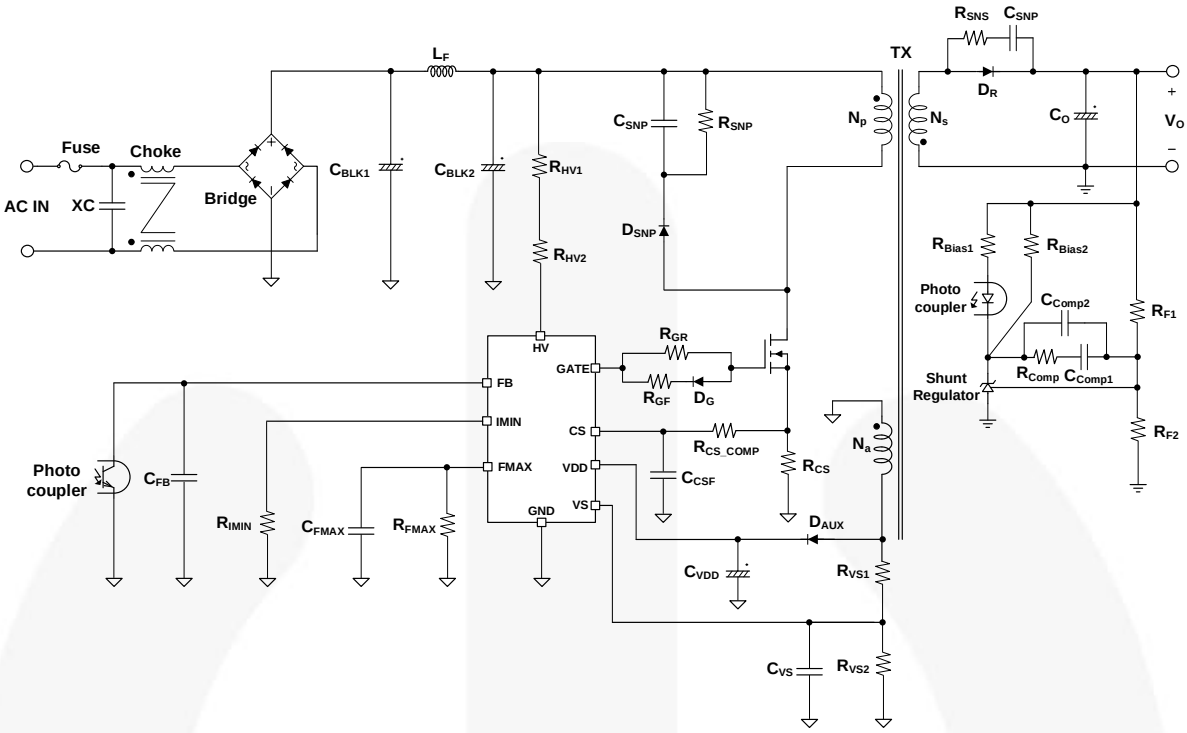


Figure 1. FAN602L Typical Application Circuit

Block Diagram

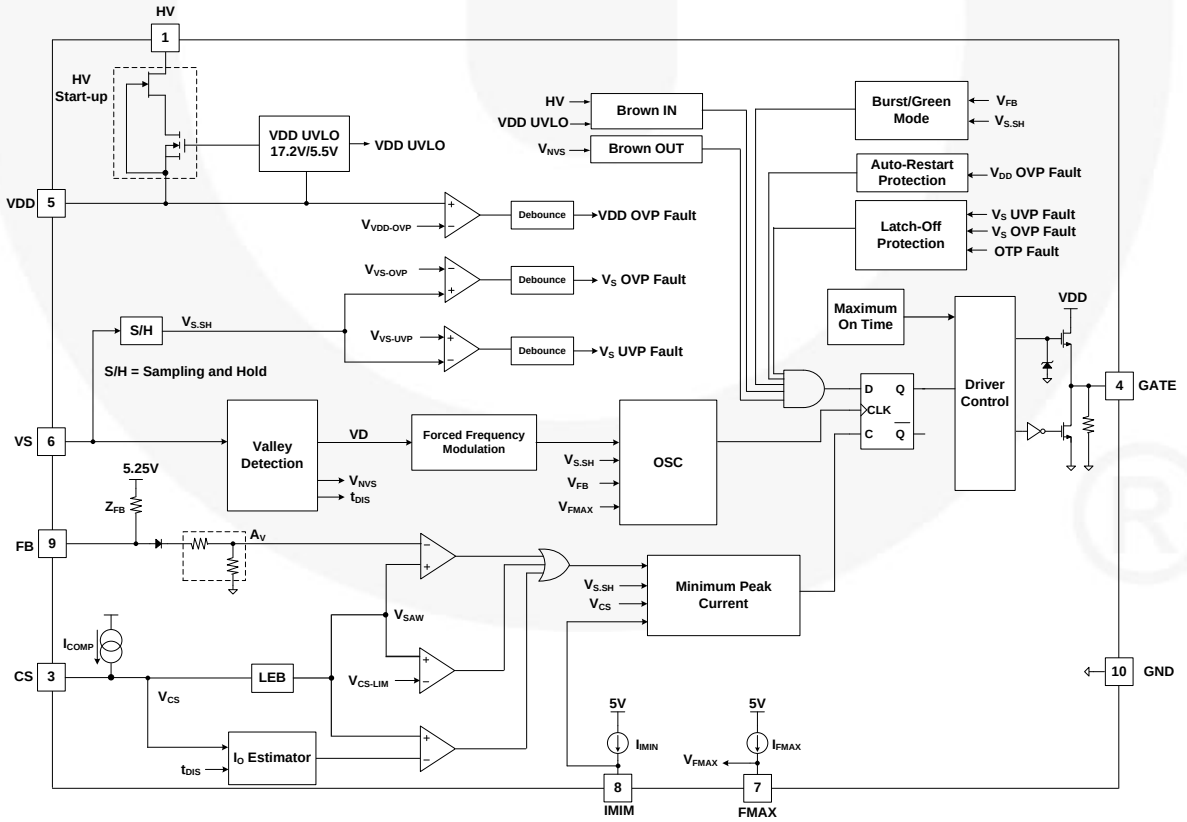
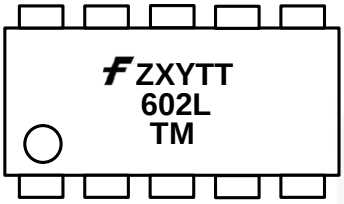


Figure 2. FAN602L Block Diagram

Marking Information



***F*- Fairchild Logo**
Z: Assembly Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
P: T: Package Type (M=SOIC)
M: Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

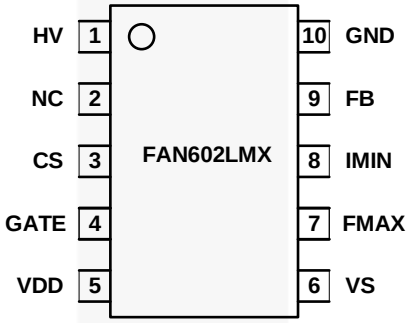


Figure 4. Pin Assignment

Pin Definitions

Pin #	Name	Description
1	HV	**High Voltage**. This pin connects to DC bus for high-voltage startup.
2	NC	**No Connect**.
3	CS	**Current Sense**. This pin connects to a current-sense resistor to sense the MOSFET current for Peak-Current-Mode control for output regulation. The current sense information is also used to estimate the output current for CC regulation.
4	GATE	**PWM Signal Output**. This pin has an internal totem-pole output driver to drive the power MOSFET. The gate driving voltage is internally clamped at 7.5 V.
5	VDD	**Power Supply**. IC operating current and MOSFET driving current are supplied through this pin. This pin is typically connected to an external V_{DD} capacitor.
6	VS	**Voltage Sense**. The VS voltage is used to detect resonant valleys for quasi-resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage. It also senses input voltage for Brownout protection.
7	FMAX	**Maximum Blanking Frequency**. This pin connects to external resistor to program maximum blanking frequency.
8	IMIN	**Minimum V_{cs}**.This pin connects to external resistor to program minimum VCS Threshold level for burst mode operating optimization.
9	FB	**Feedback**. Typically Opto-Coupler is connected to this pin to provide feedback information to the internal PWM comparator. This feedback is used to control the duty cycle in CV regulation.
10	GND	**Ground**.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{HV}	HV Pin Input Voltage			500	V
V_{VDD}	DC Supply Voltage			30	V
V_{VS}	VS Pin Input Voltage		-0.3	6.0	V
V_{CS}	CS Pin Input Voltage		-0.3	6.0	V
V_{FB}	FB Pin Input Voltage		-0.3	6.0	V
V_{FMAX}	FMAX Pin Input Voltage		-0.3	6.0	V
V_{IMIN}	IMIN Pin Input Voltage		-0.3	6.0	V
P_D	Power Dissipation (T_A=25°C)			850	mW
θ_{JA}	Thermal Resistance (Junction-to-Ambient)			140	°C/W
Ψ_{JT}	Thermal Resistance (Junction-to-Top)			13	°C/W
T_J	Operating Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-40	+150	°C
T_L	Lead Temperature, (Wave soldering or IR, 10 Seconds)			+260	°C
ESD[3]	Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22_A114 (Except HV Pin)		3.0	kV
		Charged Device Model, JEDEC:JESD22_C101 (Except HV Pin)		2.0	

Notes:

1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. ESD ratings including HV pin: HBM=2.0 kV, CDM=2.0 kV.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{HV}	HV Pin Supply Voltage	50		400	V
V_{VDD}	VDD Pin Supply Voltage	6	15	25	V
V_{VS}	VS Pin Supply Voltage	0.65		2.90	V
V_{CS}	CS Pin Supply Voltage	0		0.9	V
V_{FB}	FB Pin Supply Voltage	0		5.25	V
V_{FMAX}	FMAX Pin Supply Voltage	0		1	V
V_{IMIN}	IMIN Pin Supply Voltage	0		2.5	V
T_A	Operating Temperature	-40		+85	°C

Electrical Characteristics

V_{DD}=15 V and T_J=-40~125 °C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
HV Section						
I_{HV}	Supply Current Drawn from HV Pin	V_{HV}=120 V, V_{DD}=0 V	1.2	2.0	10	mA
I_{HV-LC}	Leakage Current Drawn from HV Pin	V_{HV}=500 V, V_{DD}=V_{DD-OFF}+1 V	0	0.8	10	µA
$V_{Brown-IN}$	Brown-In Threshold Voltage.	R_{HV}=150 kΩ, V_{IN}=80 V_{rms}	100	110	120	V
V_{DD} Section						
V_{DD-ON}	Turn-On Threshold Voltage	V_{DD} Rising	15.3	17.2	18.7	V
V_{DD-OFF}	Turn-Off Threshold Voltage	V_{DD} Falling	5.0	5.5	5.7	V
$V_{DD-HV-ON}$	Threshold Voltage for HV Startup	T_J=25°C	4.1	4.7	5.4	V
V_{DD-DLH}	Threshold Voltage for Latch Release		2	2.5	3	V
I_{DD-ST}	Startup Current	V_{DD}=V_{DD-ON}-0.16 V, T_J=25°C		300	400	µA
I_{DD-OP}	Operating Supply Current	V_{CS}=5.0 V, V_S=3 V, V_{FB}=3 V, V_{DD}=15 V, C_{GATE}=1 nF		2	3	mA
$I_{DD-Burst}$	Burst-Mode Operating Supply Current	V_{CS}=0.3 V, V_S=0 V, V_{FB}=0 V; V_{DD}=V_{DD-ON}→V_{DD-OVP}→10 V, C_{GATE}=1 nF		300	600	µA
$V_{VDD-OVP}$	V_{DD} Over-Voltage-Protection Level	T_J=25°C	27.5	29.0	29.5	V
$t_{D-VDDOVP}$	VDD Over-Voltage-Protection Debounce Time			70	105	µs
Oscillator Section						
I_{FMAX}	FMAX Pin Current		18	20	22	µA
$f_{BNK-MAX}$	Maximum Blanking Frequency	R_{FMAX}= 0	130	140	150	kHz
$f_{BNK-MIN}$	Minimum Blanking Frequency	R_{FMAX}= 48.3 kΩ	50	60	65	kHz
$f_{OSC-MIN-DCM}$	Minimum Frequency for DCM	V_{VS}=0 V	40	50	60	kHz
$f_{OSC-MIN-CrM}$	Minimum Frequency for CrM	V_{VS}=1 V, T_J=25°C	11	20	29	kHz
$\Delta t_{FM-Range}$	Forced Frequency Modulation Range(4)	V_{FB} > $V_{FB-Burst-H}$	225	265	305	ns
$\Delta t_{FM-Period}$	Forced Frequency Modulation Period(4)		2.1	2.5	2.9	ms
Feedback Input Section						
Z_{FB}	FB Pin Input Impedance		39	42	45	kΩ
A_V	Internal Voltage Attenuator of FB Pin(4)	V_{HV}= 120 V_{DC}, V_{DD}=0 V	1/3	1/3.5	1/4	V/V
$V_{FB-Open}$	FB Pin Pull-Up Voltage	FB Pin Open	4.75	5.25	5.90	V
$V_{FB-Burst-H}$	FB Threshold to Enable/Disable Gate Drive in Burst Mode	V_{FB} Rising	1.15	1.25	1.35	V
$V_{FB-Burst-L}$		V_{FB} Falling	1.1	1.2	1.3	V
$V_{FB-BNK-H}$	Frequency Fold-back Starting/Stopping V_{FB}		1.75	2.05	2.35	V
$V_{FB-BNK-L}$			1.2	1.5	1.8	V

Continued on the following page…

Electrical Characteristics

V_{DD}=15 V and T_J=-40~125 °C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Voltage-Sense Section						
I_{VS-MAX}	Maximum V_S Source Current Capability				3	mA
$t_{VS-BNK1}$	V_S Sampling Blanking Time 1 after GATE Pin Pull-Low	V_{FB} < 2.0 V	0.90	1.10	1.37	µs
$t_{VS-BNK2}$	V_S Sampling Blanking Time 2 after GATE Pin Pull-Low	V_{FB} > 2.2 V, T_J=25°C	1.6	1.8	2.1	µs
$t_{ZCD-to\ PWM}$	Delay from VS Voltage Zero Crossing to PWM ON(4)	V_{VS}=0 V, C_{GATE}=1 nF		175		ns
$I_{VS-Brownout}$	V_S Source Current Threshold to Enable Brownout	Set I_{VS}=2.4 mA at 264 V_{rms}, Brownout =55 V_{rms}	370	450	520	µA
$t_{D-Brownout}$	Brownout Debounce Time		12.5	16.5	21.0	ms
V_{VS-OVP}	Output Over-Voltage-Protection with Vs Sampling Voltage		2.8	2.9	3.0	V
N_{VS-OVP}	Output Over-Voltage-Protection Debounce Cycle Counts			2		Cycle
$V_{VS-UVP-H}$	Output Under-Voltage-Protection with Vs Sampling Voltage	T_J=25°C	0.76	0.80	0.84	V
$V_{VS-UVP-L}$	Output Under-Voltage-Protection with Vs Sampling Voltage	T_J=25°C	0.625	0.650	0.675	V
N_{VS-UVP}	Output Over-Voltage-Protection Debounce Cycle Counts			2		Cycle
$t_{VS-UVP-BLANK}$	Output Under-Voltage Protection Blanking Time at startup		25	40	55	ms
Over-Temperature Protection Section						
T_{OTP}	Threshold Temperature for Over-Temperature-Protection(4)			140		°C
Current-Sense Section						
V_{CS-LIM}	Current Limit Threshold Voltage	FB Pin Open	0.85	0.90	0.95	V
I_{IMIN}	IMIN Pin Current		9	10	11	µA
$V_{CS-IMIN-MIN}$	Minimum Current Sense Voltage	V_{S_SH}=2.5 V,R_{IMIN}=250 kΩ	0.14	0.18	0.23	V
$V_{CS-IMIN-MAX}$	Maximum Current Sense Voltage	V_{S_SH}=2.5 V,R_{IMIN}=0 Ω	0.40	0.44	0.50	V
t_{PD}	GATE Output Turn-Off Delay			100	200	ns
t_{LEB}	Leading-Edge Blanking Time			150	200	ns

Continued on the following page…

Electrical Characteristics

V_{DD}=15 V and T_J=-40~125 °C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Constant Current Correction Section						
I_{COMP-H}	High Line Compensation Current	V_{IN}=264 V_{rms}	90	100	110	µA
I_{COMP-L}	Low Line Compensation Current	V_{IN}=90 V_{rms}	32	36	40	µA
Constant Current Estimator						
V_{REF_CC}	Constant Current Control Reference Voltage(4)			1.2		V
A_{PK}	Peak Value Amplifying Gain(4)			3.6		V/V
$V_{FB-CC-Open}$	FB CC Pull-Up Voltage(4)			4.0		V
A_{V-CC}	Internal Voltage Attenuator of FB CC(4)			0.444		V/V
GATE Section						
V_{GATE-L}	Gate Output Voltage Low		0		1.5	V
$V_{DD-PMOS-ON}$	Internal Gate PMOS Driver ON		7.0	7.5	8.0	V
$V_{DD-PMOS-OFF}$	Internal Gate PMOS Driver OFF		9.0	9.5	10.0	V
t_r	Rising Time	V_{CS}=0 V, V_S=0 V, C_{GATE}=1 nF	100	135	180	ns
t_f	Falling Time	V_{CS}=0 V, V_S=0 V, C_{GATE}=1 nF	30	50	70	ns
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=25 V	6.8	7.5	8.2	V
t_{ON-MAX}	Maximum On Time	V_{FB}=3 V, V_{CS}=0.3 V	18	20	23	µs

Note:

4. Guaranteed by design.

Typical Performance Characteristics

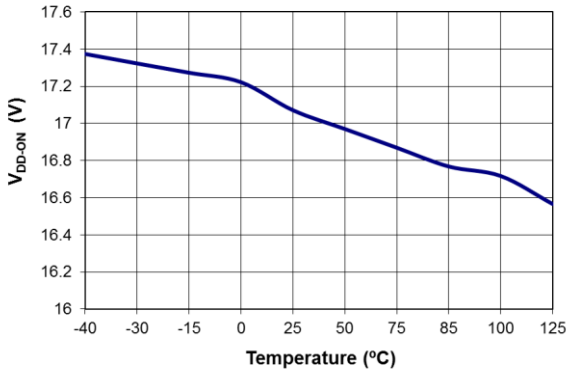


Figure 5. Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

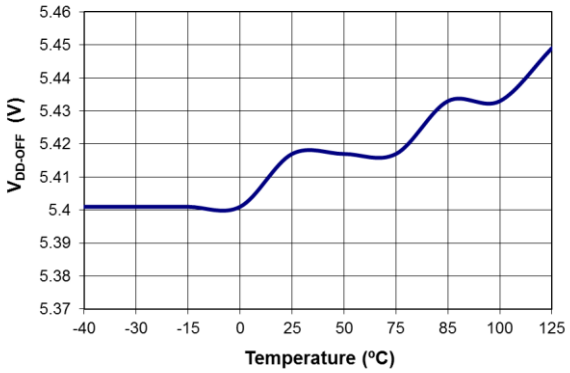


Figure 6. Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

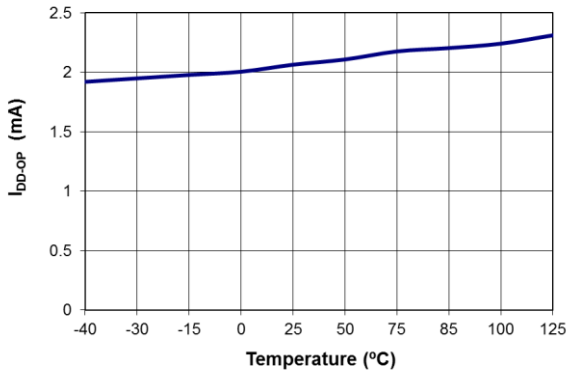


Figure 7. Operating Supply Current (I_{DD-OP}) vs. Temperature

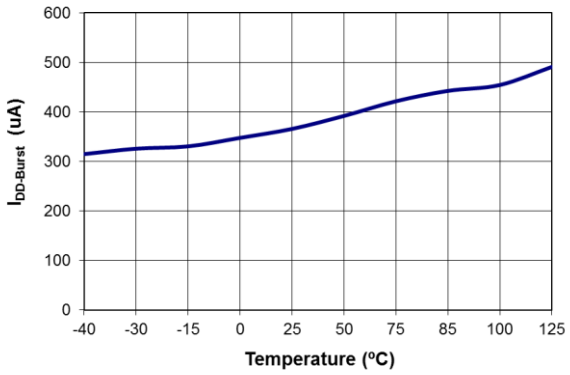


Figure 8. Burst-Mode Operating Supply Current ($I_{DD-Burst}$) vs. Temperature

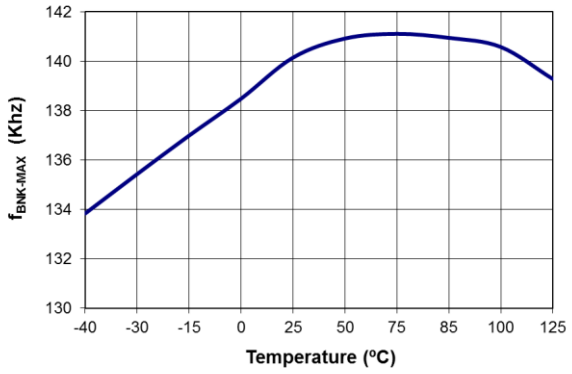


Figure 9. Maximum Blanking Frequency ($f_{BNK-MAX}$) vs. Temperature

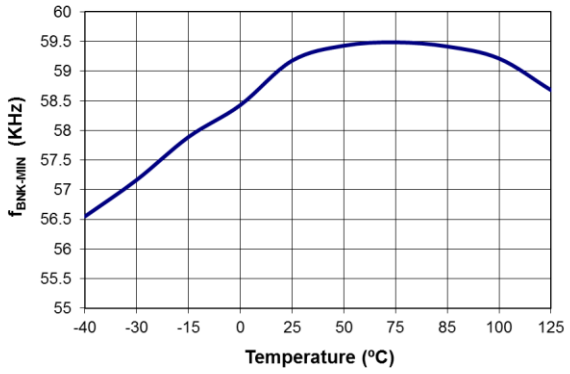


Figure 10. Minimum Blanking Frequency ($f_{BNK-MIN}$) vs. Temperature

Typical Performance Characteristics (Continued)

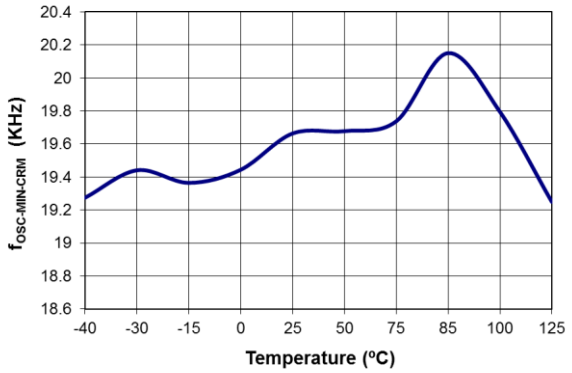


Figure 11. Minimum Frequency for CrM ($f_{OSC-MIN-CrM}$) vs. Temperature

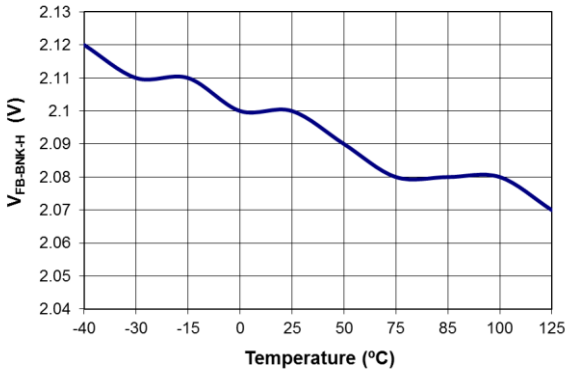


Figure 12. Frequency Fold-back Starting ($V_{FB-BNK-H}$) vs. Temperature

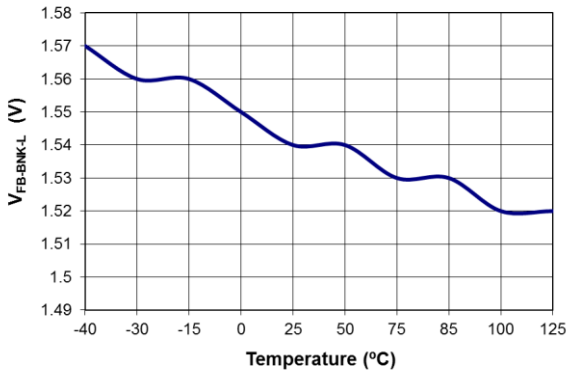


Figure 13. Frequency Fold-back Stopping ($V_{FB-BNK-L}$) vs. Temperature

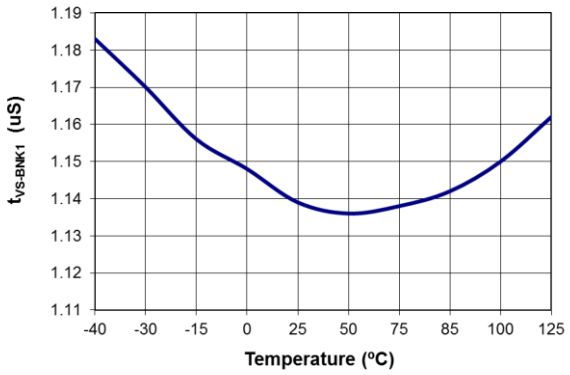


Figure 14. V_S Sampling Blanking Time 1 ($t_{VS-BNK1}$) vs. Temperature

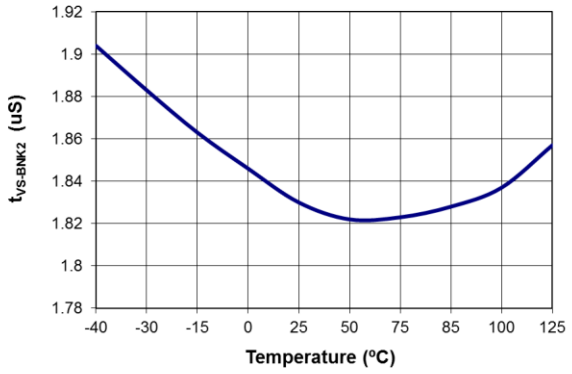


Figure 15. V_S Sampling Blanking Time 2 ($t_{VS-BNK2}$) vs. Temperature

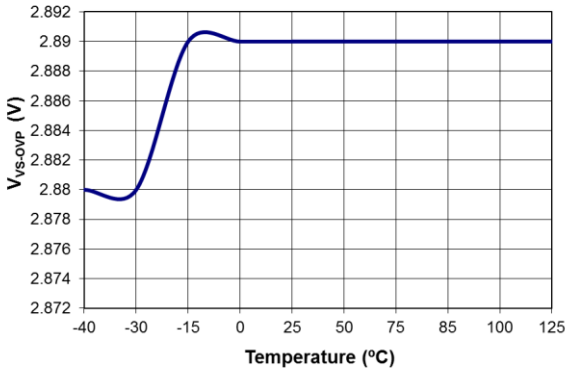


Figure 16. Output Over-Voltage-Protection (V_{VS-OVP}) vs. Temperature

Typical Performance Characteristics (Continued)

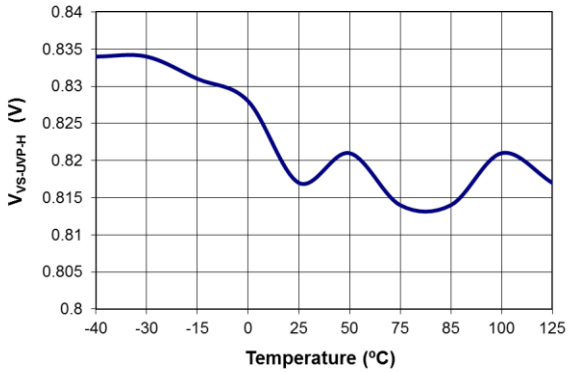


Figure 17. Output Under-Voltage Protection ($V_{VS-UVP-H}$) vs. Temperature

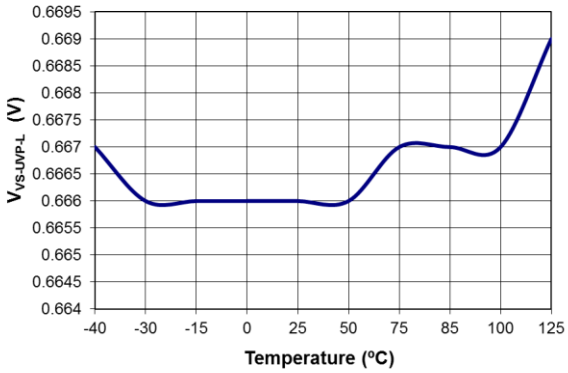


Figure 18. Output Under-Voltage Protection ($V_{VS-UVP-L}$) vs. Temperature

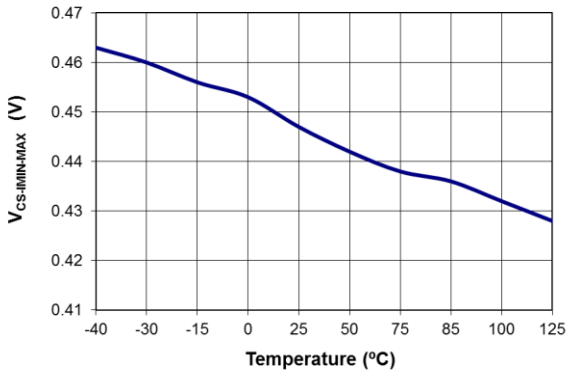


Figure 19. Maximum Current Sense Voltage ($V_{CS-IMIN-MAX}$) vs. Temperature

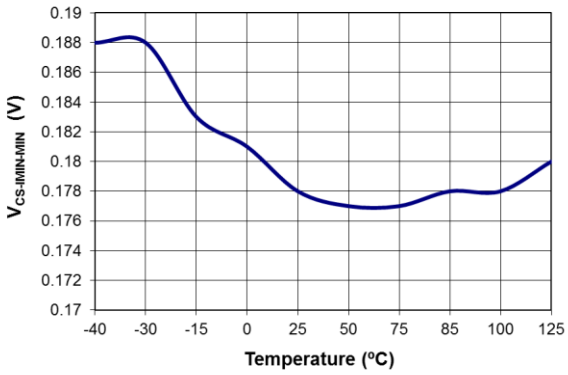


Figure 20. Minimum Current Sense Voltage ($V_{CS-IMIN-MIN}$) vs. Temperature

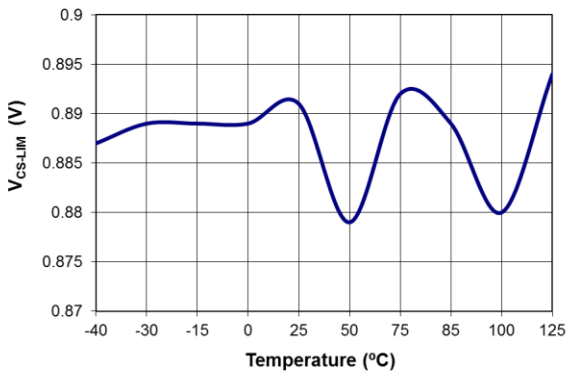


Figure 21. Current Limit Threshold Voltage (V_{CS-LIM}) vs. Temperature

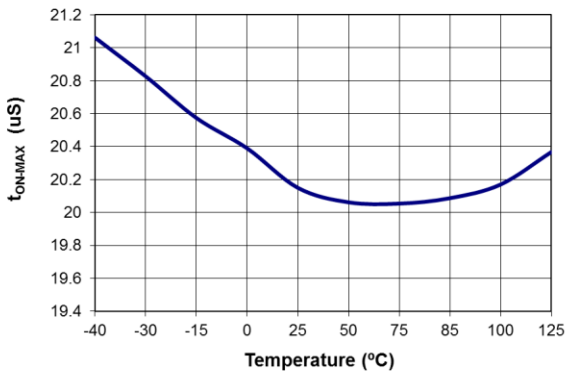


Figure 22. Maximum On Time (t_{ON-MAX}) vs. Temperature

Functional Description

FAN602L is an offline PWM controller which operates in a quasi-resonant (QR) mode and significantly enhances system efficiency and power density. Its control method is based on the load condition (valley switching with fixed blanking time at heavy load and valley switching with variable blanking time at medium load) to maximize the efficiency. FMAX pin allows programming the maximum blanking frequency. It offers constant output voltage (CV) regulation through opto-coupler feedback circuitry.

Line voltage compensation gain can be programmed by using an external resistor to minimize the effect of line voltage variation on output current regulation due to turn-off delay of the gate drive circuit. FAN602L incorporates HV startup and accurate brown-In through HV pin. The brown-in voltage is programmed by using an external HV pin resistor. The minimum peak current ($V_{CS-IMIN}$), which controls the burst mode entry/exit and improves light load efficiency, is programmable via an external resistor connected to the IMIN pin.

Basic Operation Principle

Quasi-resonant switching is a method to reduce primary MOSFET switching losses especially in high line. In order to perform QR turn-on of the primary MOSFET, the valley of the resonance occurring between transformer magnetizing inductance (L_m) and MOSFET effective output capacitance ($C_{oss-eff}$) must be detected.

$$C_{OSS-eff} = C_{OSS-MOSFET} + C_{trans} + C_{parasitic} \quad (1)$$

$$t_{resonance} = 2\pi \cdot \sqrt{L_m \cdot C_{OSS-eff}} \quad (2)$$

For heavy load condition (50%~100% of full load), the blanking time for the valley detection is fixed such that the switching time is between t_{BNK} and $t_{BNK}+t_{resonance}$. The upper limit of the blanking frequency is programmed by FMAX pin. For the medium load condition (25%~50% of full load), the blanking time is modulated as a function of load current such that the upper limit of the blanking frequency varies from $f_{BNK-MAX}$ as load decreases where the blanking frequency reduction stop point is $f_{BNK-MIN}$.

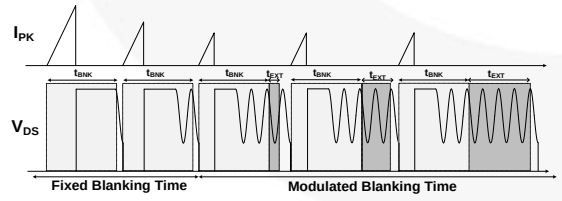


Figure 23. Frequency Fold-back Function

The Maximum Blanking Frequency Selection

The FAN602L allows adjusting the maximum blanking frequency ($f_{BNK-MAX}$) of operation through an external resistor on the FMAX pin. As shown in Figure 24, an internal current source of 20 µA creates a voltage V_{FMAX} across the resistance, R_{FMAX}. This voltage sets the oscillator reference voltage which determines $t_{BNK-MIN}$ (time period for $f_{BNK-MAX}$). The relationship between $f_{BNK-MAX}$ and R_{FMAX} is shown in Figure 25.

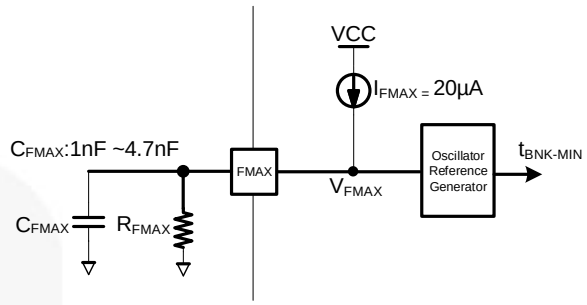


Figure 24. FMAX Function Circuit

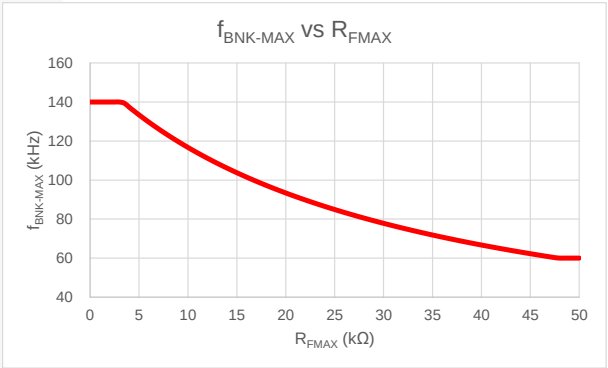


Figure 25. $f_{BNK-MAX}$ vs. R_{FMAX}

Valley Detection

There will be a logic propagation delay from VS Zero-Crossing Detection (V_{S-ZCD}) to IC GATE turn on and a MOSFET gate drives propagation delay from GATE pin to MOSFET turn on. We can assume the sum of these propagation delays to be $t_{ZCD-to-PWM}$, as shown in Figure 27. However, if 1/2 t_F is larger than $t_{ZCD-to-PWM}$, the switching occurs away from the valley causing higher losses. The time period of resonant ringing is dependent on L_m and $C_{oss-eff.}$ Typically, the time period of resonance ringing is around 1~1.5 µs depending on the system parameters. Hence, the switching may occur at a point different from the valley depending on the system. When PCB layout is poor, it may cause noise on the VS pin. The VS pin needs to be in parallel with the capacitor (C_{VS}) less than 10 pF to filter the noise.

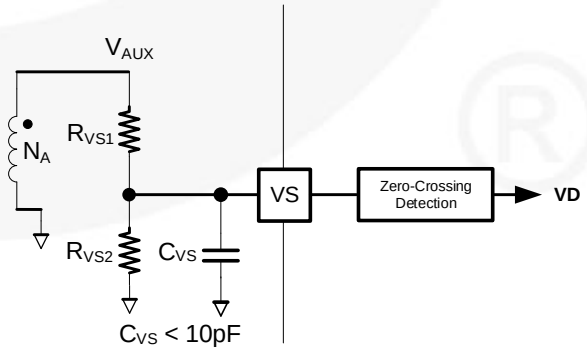


Figure 26. The Valley Detection Circuit

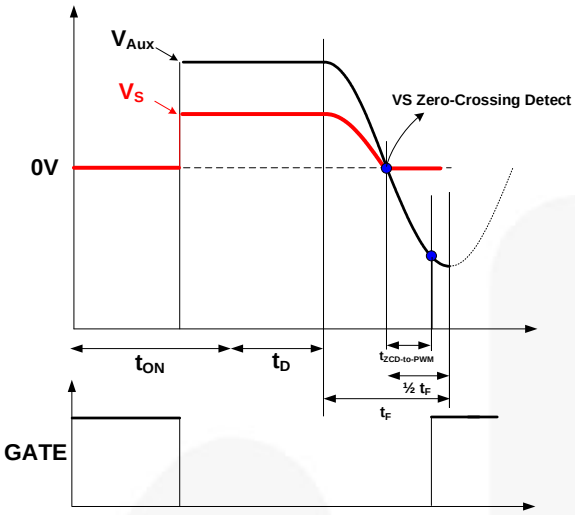


Figure 27. Valley Detection Behavior

Inherent and Forced Frequency Modulation

Typically, the bulk capacitor of flyback converter has a longer charging time in low line than in high line. Thus, the voltage ripple (ΔV_{DC}) in low line is higher as shown in Figure 28. This large ripple results in 4~6% variation of the switching frequency in low line for a valley switched converter. Hence, the EMI performance in low line is satisfied. However, in high line, the ripple is very small and consequent. The EMI performance for high line may suffer. In order to maintain good EMI performance for high line, forced frequency modulation is provided. FAN602L varies the valley switching point from 0 to $\Delta t_{FM\text{-}Range}$ (265 ns) in every $\Delta t_{FM\text{-}Period}$ (2.5 ms) as shown in Figure 29. Since the drain voltage at which the switching occurs does not change much with this variation, there is minimum impact on the efficiency.

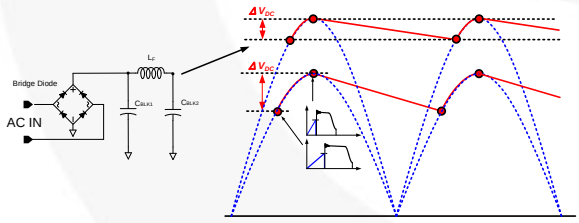


Figure 28. Inherent Frequency Modulation

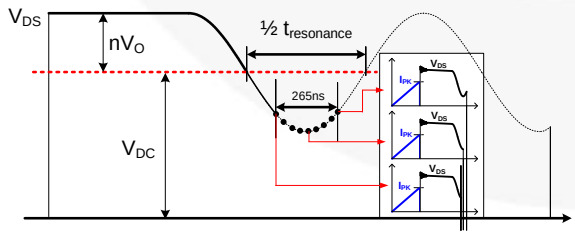


Figure 29. Forced Frequency Modulation

Output Voltage Detection

Figure 30 shows the VS voltage is sampled ($V_{S\text{-}SH}$) after $t_{VS\text{-}BNK}$ of GATE turn-off so that the ringing does not introduce any error in the sampling. FAN602L dynamically varies $t_{VS\text{-}BNK}$ with load. At heavy load, $t_{VS\text{-}BNK}$=$t_{VS\text{-}BNK1}$ (1.8 µs) when V_{FB} > 2.2 V. At light load, $t_{VS\text{-}BNK}$=$t_{VS\text{-}BNK2}$ (1.1 µs) when V_{FB} < 2 V. This dynamic variation ensures that VS sampling occurs after ringing due to leakage inductance has stopped and before secondary current goes to zero.

$$V_{S-SH} = V_O \cdot \frac{N_A}{N_S} \cdot \frac{R_{VS2}}{(R_{VS1} + R_{VS2})} \quad (3)$$

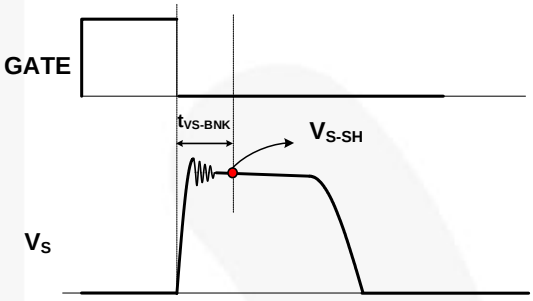


Figure 30. Output Voltage Detection

Burst Mode Operation

FAN602L features burst mode operation with a programmable burst mode entry load condition by using minimum peak current ($V_{CS\text{-}IMIN}$) control which enables light-load efficiency to be optimized for a given application. The IMIN pin can be programmed with external resistor R_{IMIN} to select the minimum V_{CS} threshold level for burst mode entry. Figure 31 shows the implementation of IMIN in FAN602L.

Figure 32 shows when V_{FB} drops below $V_{FB\text{-}Burst\text{-}L}$, the PWM output shuts off and the output voltage drops at a rate which is depended on the load current level. This causes the feedback voltage to rise. Once V_{FB} exceeds $V_{FB\text{-}Burst\text{-}H}$, FAN602L resumes switching. As shown in Figure 33, when the FB voltage drops below the corresponding $V_{CS\text{-}IMIN}$, the peak currents in switching cycles are fixed to $V_{CS\text{-}IMIN}$ regardless of FB voltage. Thus, more power is delivered to the load than required and once FB voltage is pulled low below $V_{FB\text{-}Burst\text{-}L}$, switching stops again. In this manner, the burst mode operation alternately enables and disables switching of the MOSFET to reduce the switching losses.

For adaptive output application, the minimum peak current is modulated in accordance with the $V_{S\text{-}SH}$ such that the minimum peak current is proportional to the square root of output voltage. For easy circuit implementation, curve fitting is used as shown in Figure 34.

$$V_{CS-IMIN} = \frac{(V_{S-SH} - I_{MIN} \times R_{IMIN})}{10} + 0.2 \quad (4)$$

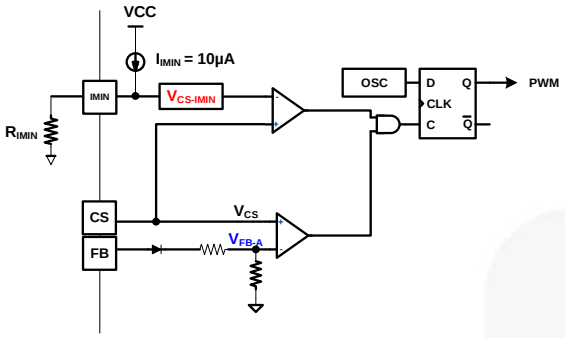


Figure 31. IMIN Function Circuit

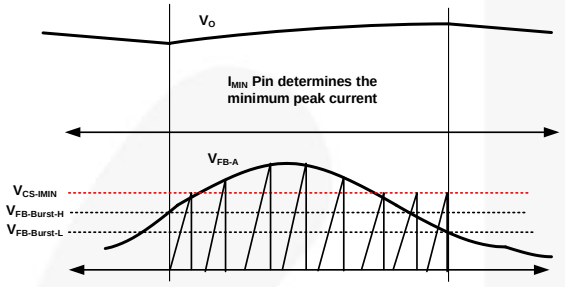


Figure 32. Burst-Mode Operation with IMIN

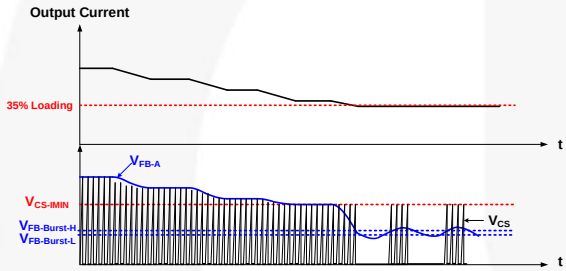


Figure 33. System enter Burst-mode Behavior

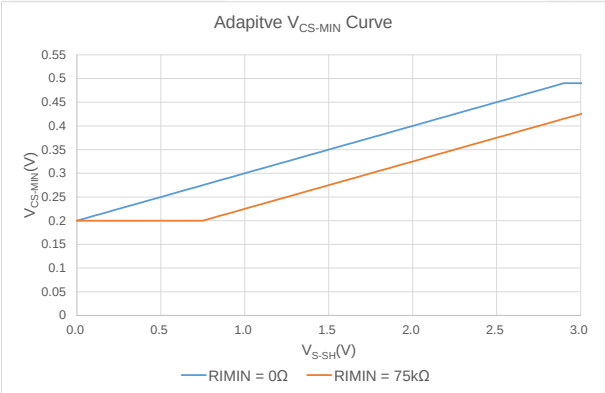


Figure 34. $V_{CS-IMIN}$ as a Function of R_{IMIN} with Variation of V_{S-SH}

Deep Burst Mode

FAN602L enters deep burst mode if FB voltage stays lower than $V_{FB-Burst-L}$ for more than $t_{Deep-Burst-Entry}$ (640 μs). Once FAN602L enters deep burst mode, the operating current is reduced to $I_{DD-Burst}$ (300 μA) to minimize power consumption. Once feedback voltage is more than $V_{FB-Burst-H}$, power-on-reset occurs within a time period of $t_{Deep-Burst-Exit}$ (25 μs) and IC resumes switching with normal operating current, I_{DD-OP}.

Line Voltage Detection

The FAN602L indirectly senses the line voltage through the VS pin while the MOSFET is turned on, as illustrated in Figure 35 and Figure 36. During MOSFET turn-on period, the auxiliary winding voltage, V_{AUX}, is proportional to the input bulk capacitor voltage, V_{BLK}, due to the transformer coupling between the primary and auxiliary windings. During the MOSFET conduction time, the line voltage detector clamps the VS pin voltage to $V_{S-Clamp}$ (0 V), and then the current I_{VS} flowing out of VS pin is expressed as:

$$I_{VS} = \frac{V_{BLK}}{R_{VS1}} \cdot \frac{N_A}{N_S} \quad (5)$$

The I_{VS} current, reflecting the line voltage information, is used for brownout protection and CC control correction weighting.

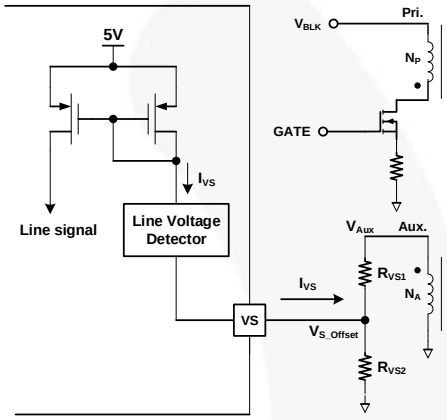


Figure 35. Line Voltage Detection Circuit

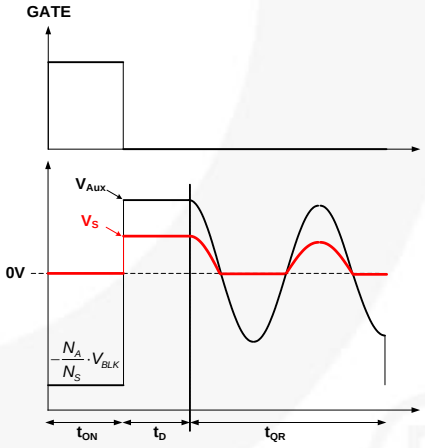


Figure 36. Waveforms for Line Voltage Detection

CV / CC PWM Operation Principle

Figure 37 shows a simplified CV / CC PWM control circuit of the FAN602L. The Constant Voltage (CV) regulation is implemented in the same manner as the conventional isolated power supply, where the output voltage is sensed using a voltage divider and compared with the internal reference of the shunt regulator to generate a compensation signal. The compensation signal is transferred to the primary side through an opto-coupler and scaled down by attenuator A_V to generate a COMV signal. This COMV signal is applied to the PWM comparator to determine the duty cycle.

The Constant Current (CC) regulation is implemented internally with primary-side control. The output current estimator calculates the output current using the transformer primary-side current and diode current discharge time. By comparing the estimated output current with internal reference signal, a COMI signal is generated to determine the duty cycle.

These two control signals, COMV and COMI, are compared with an internal saw-tooth waveform (V_{SAW}) by two PWM comparators to determine the duty cycle. Figure 38 illustrates the outputs of two comparators, combined with an OR gate, to determine the MOSFET turn-off instant. Either of COMV or COMI, the lower signal determines the duty cycle. As shown in Figure 38, during CV regulation, COMV determines the duty cycle while COMI is saturated to HIGH level. During CC regulation, COMI determines the duty cycle while COMV is saturated to HIGH level.

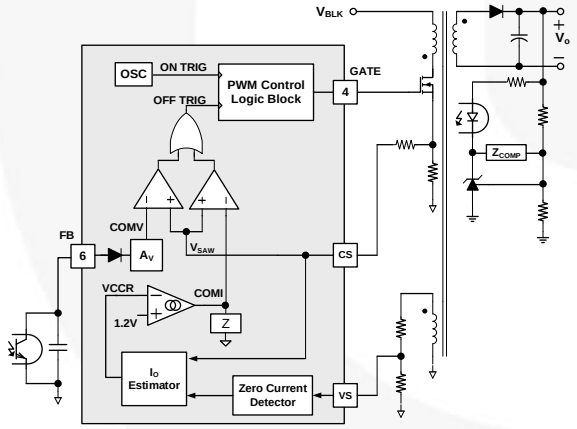


Figure 37. Simplified PWM Control Circuit

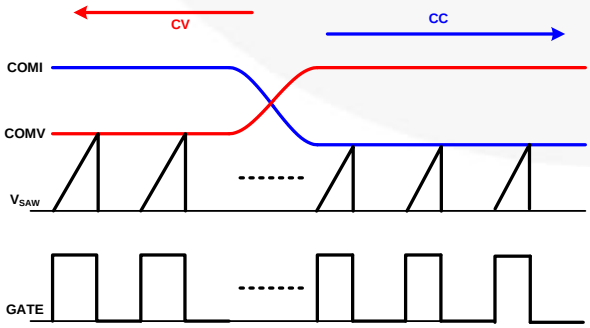


Figure 38. PWM Operation for CV/CC Regulation

Primary-Side Constant Current Operation

Figure 39 shows the key waveforms of a flyback converter operating in DCM. The output current is estimated by calculating the average of output diode current in the one switching cycle:

$$I_O = \frac{1}{2}\frac{1}{R_{CS}}\frac{V_{CS-PK}\cdot T_{dis}}{T_S}\frac{N_P}{N_S}\eta = \frac{1}{2}\frac{1}{R_{CS}}\frac{V_{REF\_CC}}{A_{PK}}\frac{N_P}{N_S}\eta \qquad (6)$$

When the diode current reaches zero, the transformer winding voltage begins to drop sharply and VS pin voltage drops as well. When VS pin voltage drops below the V_{S-SH} by more than 500 mV, Zero Current Detection (ZCD) of diode current is obtained.

The output current can be programmed by setting the current sensing resistor as:

$$R_{CS} = \frac{1}{2}\cdot\frac{1}{I_O}\cdot\frac{V_{REF\_CC}}{A_{PK}}\cdot\frac{N_P}{N_S}\cdot\eta \qquad (7)$$

Where V_{REF_CC} is the internal voltage for CC control and A_{PK} is the IC design parameter, 3.6 for FAN602L.

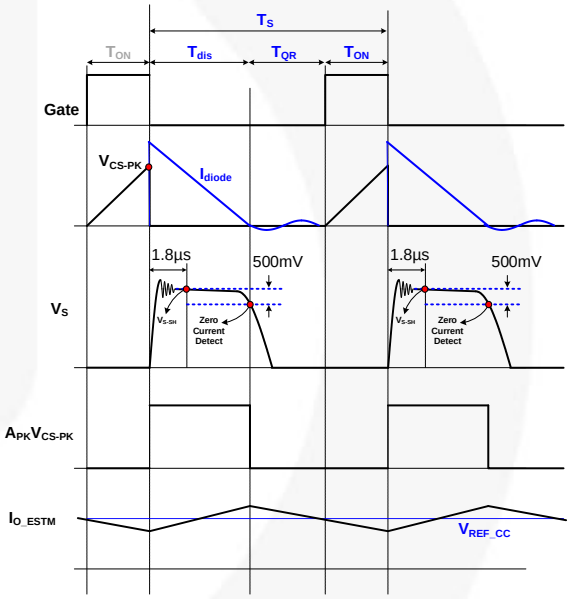


Figure 39. Waveforms for Estimate Output Current

Line Voltage Compensation

The output current estimation is also affected by the turn-off delay of the MOSFET as illustrated in Figure 40. The actual MOSFET's turn-off time is delayed due to the MOSFET gate charge and gate driver's capability, resulting in peak current detection error as:

$$\Delta I_{DS}{}^{PK} = \frac{V_{BLK}}{L_m}\cdot t_{OFF.DLY} \qquad (8)$$

Where L_m is the transformer's primary side magnetizing inductance. Since the output current error is proportional to the line voltage, the FAN602L incorporates line voltage compensation to improve output current estimation accuracy. Line information is obtained through the line voltage detector as shown in Figure 35. I_{COMP} is an internal current source, which is proportional to line voltage. The line compensation gain is programmed by using CS pin series resistor, R_{CS_COMP}, depending on the MOSFET turn-off delay, $t_{OFF.DLY}$. I_{COMP} creates a voltage drop, V_{OFFSET}, across R_{CS_COMP}. This line compensation offset is proportional to the DC link capacitor voltage, V_{BLK}, and turn-off delay, $t_{OFF.DLY}$. Figure 41 demonstrates the effect of the line compensation. When PCB layout is poor, it may cause noise on the CS pin. The CS pin needs to be in parallel with the capacitor (C_{CSF}) less than 20 pF to filter the noise.

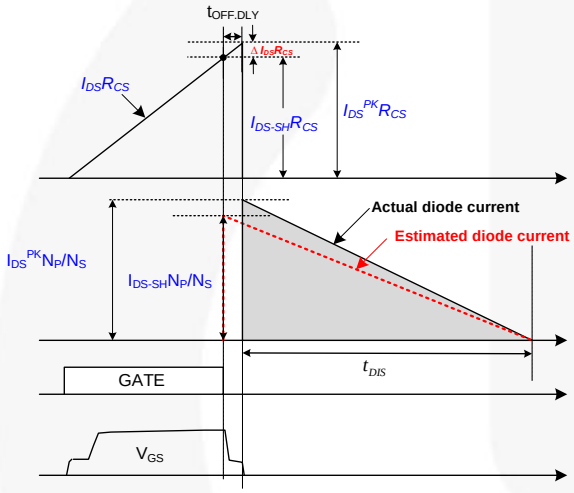


Figure 40. Effect of MOSFET Turn-off Delay

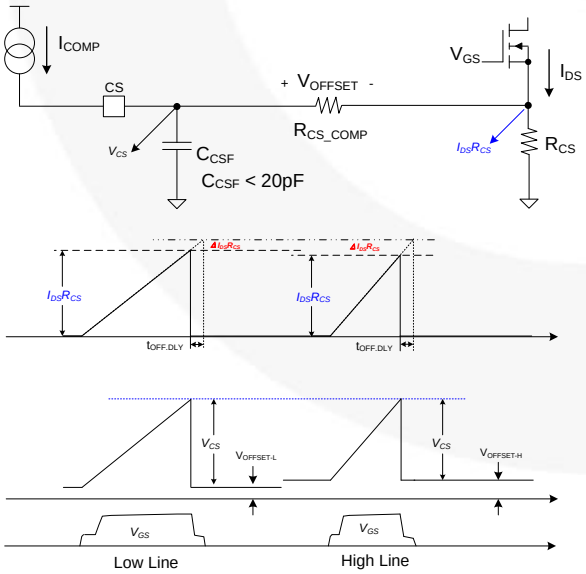


Figure 41. Line Voltage Compensation

CCM Prevention

When input or output voltage drops, the secondary side current does not reduce to zero within $t_{OSC\text{-}MIN\text{-}DCM}$ (time period for $f_{OSC\text{-}MIN\text{-}DCM}$). FAN602L does not initiate turn-on. FAN602L turns on the primary MOSFET after VS-ZCD and ensures boundary conduction mode switching. Thus FAN602L does not allow the converter to enter CCM. During CCM prevention, FAN602L can reduce the frequency down to $f_{OSC\text{-}MIN\text{-}CrM}$ (20 kHz). This phenomenon is explained in Figure 42.

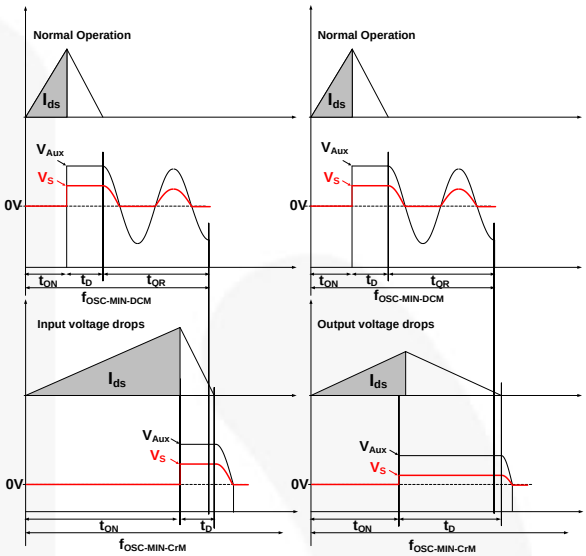


Figure 42. CCM Prevention Behavior

HV Startup and Brown-In

Figure 43 shows the high-voltage (HV) startup circuit. An Internal JFET provides a high voltage current source, whose characteristics are shown in Figure 44. To improve reliability and surge immunity, it is typical to use a R_{HV} resistor between the HV pin and the bulk capacitor voltage. The actual current flowing into the HV pin at a given bulk capacitor voltage and startup resistor value is determined by the intersection point of characteristics I-V line and the load line as shown in Figure 44.

During startup, the internal startup circuit is enabled and the bulk capacitor voltage supplies the current, I_{HV}, to charge the hold-up capacitor, C_{VDD}, through R_{HV}. When the V_{DD} voltage reaches $V_{DD\text{-}ON}$, the sampling circuit shown in Figure 43 is turned on for $t_{HV\text{-}det}$ (100 µs) to sample the bulk capacitor voltage. Voltage across R_{LS} is compared with reference which generates a signal to start switching. If brown-in condition is not detected within this time, switching does not start. Equation (9) can be used to program the brown-In of the system. If line voltage is lower than the programmed brown-In voltage, FAN602L goes in auto-restart mode.

$$V_{IN} = \frac{R_{LS} + R_{JEFT} + R_{HV}}{R_{LS}} \times V_{REF} \qquad (9)$$

Once switching starts, the internal HV startup circuit is disabled. During normal switching, the line voltage information is obtained from the IVS signal. Once the HV startup circuit is disabled, the energy stored in CVDD supplies the IC operating current until the transformer auxiliary winding voltage reaches the nominal value. Therefore, CVDD should be properly designed to prevent VDD from dropping below VDD-

OFF threshold (typically 5.5 V) before the auxiliary winding builds up enough voltage to supply VDD. During startup, the IC current is limited to IDD-ST (300 μA).

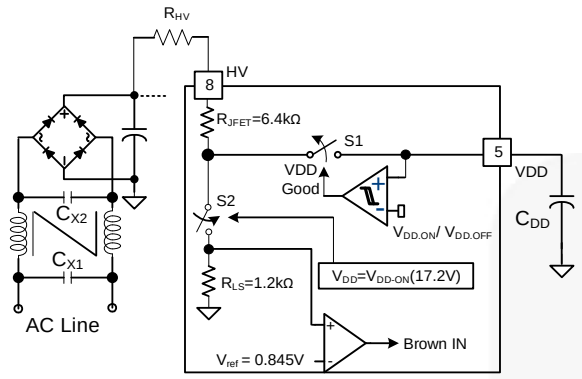


Figure 43. HV Startup Circuit

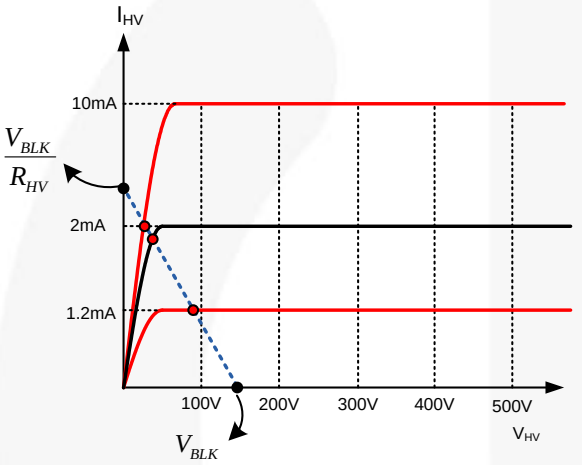


Figure 44. Characteristics of HV pin

Protections

The FAN602L protection functions include VDD Over-Voltage Protection (VDD-OVP), brownout protection, VS Over-Voltage Protection (VS-OVP), VS Under-Voltage Protection (VS-UVP), and IC internal Over-Temperature Protection (OTP). The VDD-OVP, brownout protection are implemented with Auto-Restart mode. The VS-UVP, VS-OVP and OTP are implemented with Latch-Off mode.

When the Auto-Restart Mode protection is triggered, switching is terminated and the MOSFET remains off, causing VDD to drop because of IC operating current I_{DD-OP} (2 mA). When VDD drops to the VDD turn-off voltage of V_{DD-OFF} (5.5 V), operation current reduces to $I_{DD-Deep-Burst}$ (300 μA). When the VDD voltage drops further to $V_{DD-HV-ON}$, the protection is reset and the supply current drawn from HV pin begins to charge the VDD hold-up capacitor. When VDD reaches the turn-on voltage of V_{DD-ON} (17.2 V), FAN602L resumes normal operation. In this manner, the Auto-Restart mode alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated as shown in Figure 45.

When the Latch-Off mode protection is triggered, PWM switching is terminated and the MOSFET remains off, causing VDD to drop. When VDD voltage drops to VDD turn-off voltage (V_{DD-OFF}), the IC supply current drops to $I_{DD-Burst}$. Then, when VDD drops to $V_{DD-HV-ON}$, internal startup circuit is enabled without resetting the protection, and the supply current drawn from HV pin charges the hold-up capacitor. Since the protection is not reset, the IC does not resume PWM switching even when VDD reaches the turn-on voltage of 17.2 V. Then, VDD drops again down to V_{DD-OFF}. In this manner, the Latch-Off mode protection alternately charges and discharges VDD until there is no more energy in DC link capacitor. The protection is reset when VDD drops to V_{DD-DLH} (2.5 V), which can only happen after the power supply is unplugged from the AC line as shown in Figure 46.

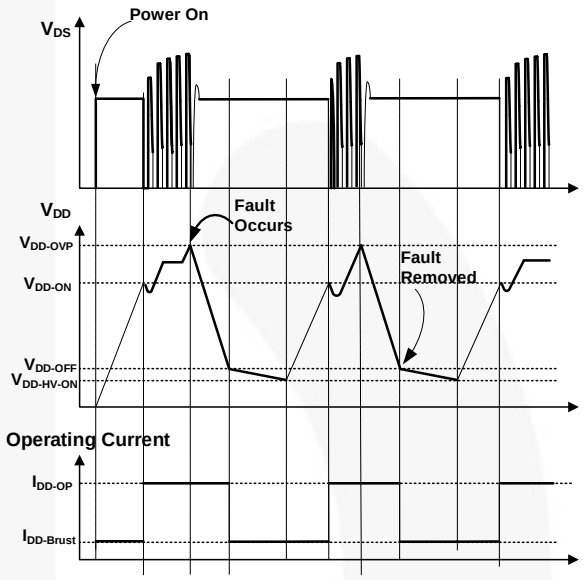


Figure 45. Auto-Restart Mode Operation

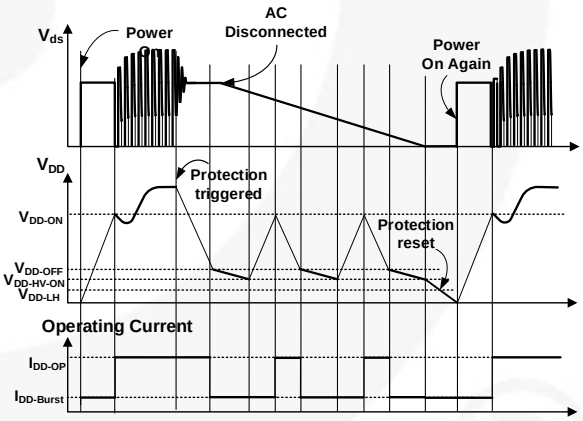


Figure 46. Latch-Off Mode Operation

VDD Over-Voltage-Protection (V_{DD-OVP})

VDD over-voltage protection prevents IC damage from over-voltage stress. It is operated in Auto-Restart mode. When the VDD voltage exceeds V_{DD-OVP} (29.0 V) for the de-bounce time, $t_{D-VDDOVP}$ (70 μs), due to abnormal condition, the protection is triggered. This protection is typically caused by an open circuit of secondary side feedback network.

Brownout Protection

Line voltage information is also used for brownout protection. When the I_{VS} current out of the VS pin during the MOSFET conduction time is less than 450 µA for longer than 16.5 ms, the brownout protection is triggered. The input bulk capacitor voltage to trigger brownout protection is given as:

$$V_{BLK.BO} = 450\mu \cdot \frac{R_{VS1}}{N_A/N_P} \quad (10)$$

IC Internal Over-Temperature-Protection (OTP)

The internal temperature-sensing circuit disables the PWM output if the junction temperature exceeds 140°C (T_{OTP}) and the FAN602L enters Latch-Off mode protection.

VS Over-Voltage-Protection (VS-OVP)

VS over-voltage protection prevents damage caused by output over-voltage condition. It is operated in Latch-Off mode. Figure 47 shows the internal circuit of VS-OVP protection. When abnormal system conditions occur, which cause VS sampling voltage to exceed $V_{VS\text{-}OVP}$ (2.9 V) for more than 2 consecutive switching cycles ($N_{VS\text{-}OVP}$), PWM pulses are disabled and FAN602L enters Latch-Off protection. VS over-voltage conditions are usually caused by open circuit of the secondary side feedback network or a fault condition in the VS pin voltage divider resistors. For VS pin voltage divider design, R_{VS1} is obtained from Equation (10), and R_{VS2} is determined by the desired VS-OVP protection function as:

$$R_{VS2} = R_{VS1} \cdot \frac{1}{\frac{V_{O-OVP}}{V_{VS-OVP}} \cdot \frac{N_A}{N_S} - 1} \quad (11)$$

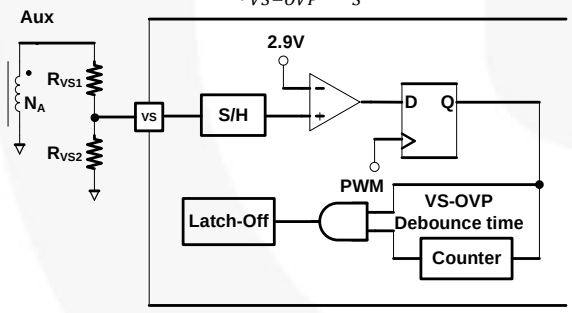


Figure 47. VS-OVP Protection Circuit

VS Under-Voltage-Protection ($V_{S\text{-}UVP}$)

In the event of an output short, output voltage will drop and the primary peak current will increase. To prevent operation for a long time in this condition, FAN602L incorporates under-voltage protection through VS pin. Figure 48 shows the internal circuit for $V_{S\text{-}UVP}$. By sampling the auxiliary winding voltage on the VS pin at the end of diode conduction time, the output voltage is indirectly sensed. When V_S sampling voltage is less than $V_{VS\text{-}UVP}$ (0.65 V) and longer than de-bounce cycles $N_{VS\text{-}UVP}$, VS-UVP is triggered and the FAN602L enters Latch-Off Mode.

To avoid VS-UVP triggering during the startup sequence, a startup blanking time, $t_{VS\text{-}UVP\text{-}BLANK}$ (45 ms), is included for system power on. For VS pin voltage divider design, R_{VS1} is obtained from Equation (10) and R_{VS2} is determined by Equation (11). $V_{O\text{-}UVP}$ can be determined by Equation (12).

$$V_{O-UVP} = \frac{N_S}{N_A} \cdot \left(1 + \frac{R_{VS1}}{R_{VS2}}\right) \cdot V_{VS-UVP} \quad (12)$$

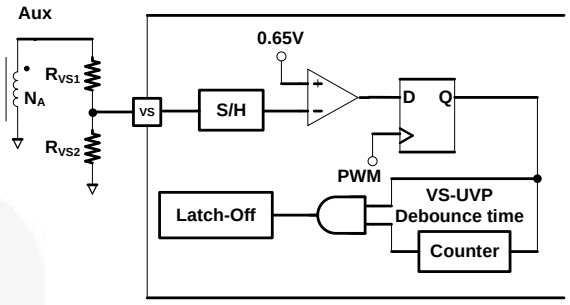


Figure 48. VS-UVP Protection Circuit

Pulse-by-Pulse Current Limit

During startup or overload condition, the feedback loop is saturated to high and is unable to control the primary peak current. To limit the current during such conditions, FAN602L has pulse-by-pulse current limit protection which forces the GATE to turn off when the CS pin voltage reaches the current limit threshold, $V_{CS\text{-}LIM}$ (0.9 V).

Secondary-Side Diode Shot Protection

When the secondary-side diode is damaged, the slope of the primary-side peak current will be sharp within leading-edge blanking time. To limit the current during such conditions, FAN602L has secondary-side diode short protection which forces the GATE to turn off when the CS pin voltage reaches 1.6V. After one switching cycle, it will operate in Auto-Restart mode as shown in Figure 49.

Current Sense Short Protection

Current sense short protection prevents damage caused by CS pin open or short to ground. After two switching cycle, it will operate in Auto-Restart mode. Figure 49 shows the internal circuit of current sense short protection. When abnormal system conditions occur, which cause CS pin voltage lower than 0.2 V after debounce time ($t_{CS\text{-}short}$) for more than 2 consecutive switching cycles, PWM pulses are disabled and FAN602L enters Auto-Restart protection. The $I_{CS\text{-}Short}$ is an internal current source, which is proportional to line voltage. The debounce time ($t_{CS\text{-}short}$) is created by $I_{CS\text{-}short}$, capacitor (2 pF) and threshold voltage (2.4 V). This debounce time ($t_{CS\text{-}short}$) is inversely proportional to the DC link capacitor voltage, V_{BLK}.

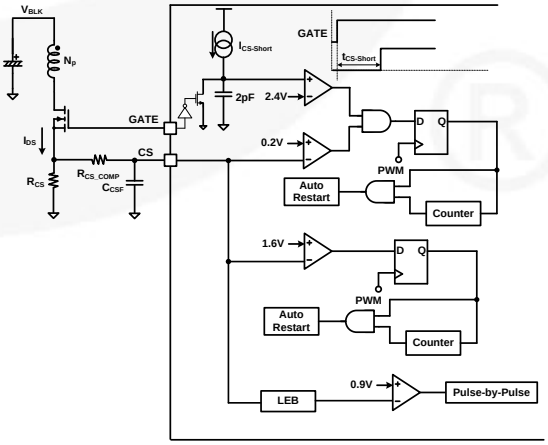
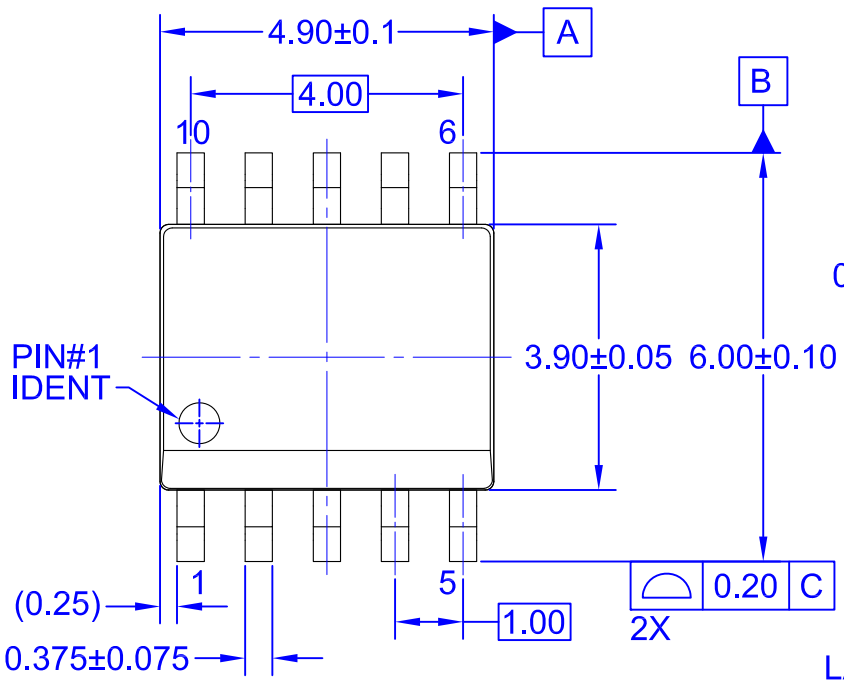
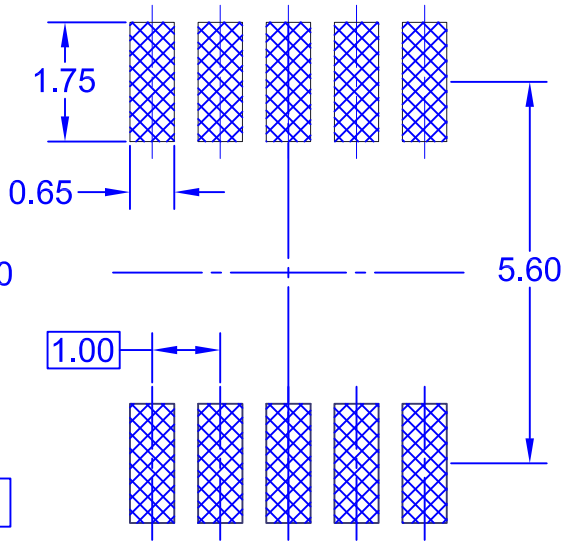


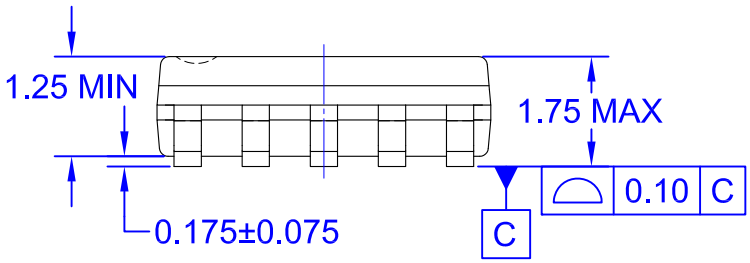
Figure 49. Current Sense Protection Circuit



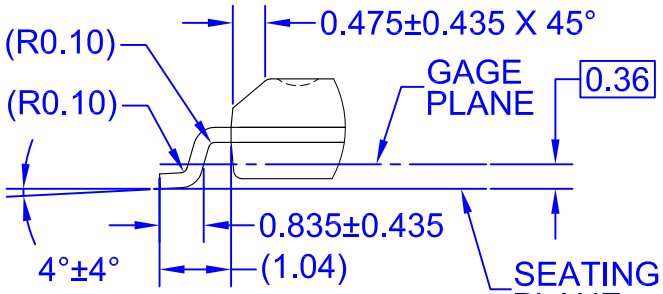
TOP VIEW



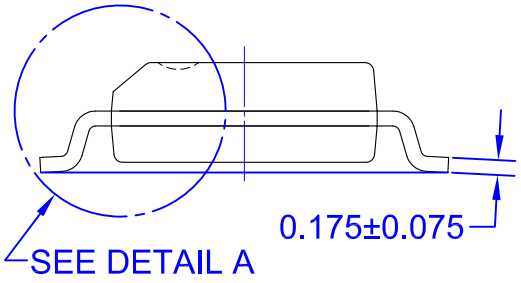
LAND PATTERN RECOMMENDATION



SIDE VIEW



DETAIL A



FRONT VIEW

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