EVBUM2253/D

KAF-4320 Imager Board User's Manual

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EVAL BOARD USER'S MANUAL

Description

The KAF-4320 Imager Evaluation Board, referred to in this document as the Imager Board, is designed to be part of a two−board set, used in conjunction with a Timing Generator Board. ON Semiconductor offers an Imager Board / Timing Generator Board package that has been designed and configured to operate with the KAF-4320 Image Sensor.

The Timing Generator Board generates the timing signals necessary to operate the CCD, and provides the power required by the Imager Board. The timing signals, in LVDS format, and the power, are provided to the Imager Board via the interface connector (J2). In addition, the Timing Generator Board performs the processing and digitization of the analog video output of the Imager Board.

The KAF-4320 Imager Board has been designed to operate the KAF-4320 with the specified performance at 3 MHz pixel clocking rate and nominal operating conditions. (See the KAF-4320 Device Specification for details).

For testing and characterization purposes, the KAF-4320 Imager Board provides the ability to adjust many of the CCD bias voltages and CCD clock level voltages by adjusting potentiometers on the board. The Imager Board provides the means to modify other device operating parameters (CCD reset clock pulse width, VSS bias voltage) by populating components differently on the board.

Certain features of the Imager Board circuitry are provided for Truesense Imaging use only, and are not supported for customer use. These circuits may not be populated on the Imager Board.

IMAGER BOARD INPUT REQUIREMENTS

Table 1. POWER REQUIREMENTS

Power Supplies	Minimum	Typical	Maximum	Units
+5 V_MTR Supply	4.9	5	5.1	V
		150		mA
−5 V_MTR Supply	−5.1	−5	−4.9	V
		0		mA
VPLUS Supply	18	20	25	V
		275		mA
VMINUS Supply	−21	−20	−18	V
		150		mA

Table 2. SIGNAL LEVEL REQUIREMENTS

Input Signals (LVDS)	V_{min}	$V_{threshold}$	V_{max}	Units	Comments
TIMING_OUT0 (±)	0	±0.1	2.4	V	Not Used
TIMING_OUT1 (±)	0	±0.1	2.4	V	H1L clock
TIMING_OUT2 (±)	0	±0.1	2.4	V	H2 clock
TIMING_OUT3 (±)	0	±0.1	2.4	V	H2 clock
TIMING_OUT4 (±)	0	±0.1	2.4	V	Not Used
TIMING_OUT5 (±)	0	±0.1	2.4	V	Reset clock
TIMING_OUT6 (±)	0	±0.1	2.4	V	V1 clock

Table 2. SIGNAL LEVEL REQUIREMENTS

Input Signals (LVDS)	V_{min}	$V_{threshold}$	V_{max}	Units	Comments
TIMING_OUT7 (±)	0	±0.1	2.4	V	V2 clock
TIMING_OUT8 (±)	0	±0.1	2.4	V	MUX SEL0
TIMING_OUT9 (±)	0	±0.1	2.4	V	MUX SEL1
TIMING_OUT10 (±)	0	±0.1	2.4	V	Not Used
TIMING_OUT11 (±)	0	±0.1	2.4	V	ALT_VDD ckt.

ARCHITECTURE OVERVIEW

The following sections describe the functional blocks of the KAF−4320 Imager Board (refer to Figure 1).

Power Filtering and Regulation

Power is supplied to the Imager Board via the J2 board interface connector. The power supplies are de-coupled and filtered with ferrite beads and capacitors to suppress noise. Voltage regulators are used to create the +15 V, −15 V and CCD VDD supplies from the VPLUS and VMINUS power supplies input to the Imager Board.

LVDS Receivers / TTL Buffers

LVDS timing signals are input to the Imager Board via the J2 interface connector. These signals are translated to TTL levels before being sent to the CCD clock drivers.

CCD Pixel−Rate Clock Drivers (H1, H1L, H2 & Reset Clocks)

The pixel rate CCD clock drivers utilize two fast switching transistors that are designed to translate TTL−level input clock signals to the voltage levels required by the CCD. The high level and low level of the CCD clocks are set by potentiometers.

Reset Clock One−Shot

The pulse width of the RESET_CCD clock can be set by a programmable One−Shot. The One−Shot can be configured to provide a RESET_CCD clock signal with a pulse width from 5 ns to 15 ns.

Alternatively, the One−Shot can be left unpopulated and bypassed by a shorting resistor. In this configuration the pulse width of the RESET_CCD clock is set by the programmable logic on the Timing Generator Board. This is the default configuration.

CCD VCLK Drivers

The vertical clock (VCLK) drivers consist of MOSFET driver IC's. These drivers are designed to translate the TTL−level clock signals to the voltage levels required by the CCD. The high and low voltage rails of the vertical clocks are set by potentiometers.

CCD Bias Voltages

The bias voltages are set by potentiometers. The bias voltages are de−coupled at the CCD pin.

Alternate VDD Circuit

The CCD's output amplifier can be turned off during the integration time by lowering the CCD's VDD bias voltage. This is accomplished using an amplifier enabled control line sent from the Timing Generator Board.

CCD Image Sensor

This evaluation board supports the KAF−4320 Image Sensor.

Emitter−Follower

The VOUT_CCD signal is buffered using a bipolar junction transistor in the emitter-follower configuration. This circuit also provides the necessary 5 mA current sink for the CCD output circuit.

Line Drivers

The buffered VOUT_CCD signals are AC−coupled and driven from the Imager Board by operational amplifiers in a non−inverting configuration. The operational amplifiers are configured to have a gain of 1.25.

Multiplexed VOUT Option

Each of the four CCD output signals is driven from the Imager Board independently. The four CCD output signals can also be input to a 4−to−1 multiplexer circuit. The output of this circuit is driven off the Imager Board as well. In order to utilize the multiplexer circuit, four shorting resistors (R7, R8, R18 and R25) must be installed on the Imager Board. Two mux control lines sent from the Timing Generator Board select which of the four CCD outputs will be driven from the Imager Board via the output of the multiplexer circuit.

OPERATIONAL SETTINGS

The Imager board is configured to operate the KAF−4320 under the following operating conditions:

Bias Voltages

The following voltages are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 3 were correct at the time of this document's publication, but may be subject to change; refer to the KAF−4320 device specification.

Table 3. BIAS VOLTAGES

Description	Symbol	Min	Nom	Max	Units	Potentiometer	Notes
Output Amplifier Supply	VDD	15	21	21	V	R104	1
Reset Drain	VRD	10	18	20	V	R130	4
Output Amplifier Return	VSS	0.7	2.1	2.8	V	–	2
Substrate	SUB		0		V	fixed	3
Output Gate	VOG	0.4	1	7.7	V	R88	4
Lateral Drain Guard Ring	VLOD	7.25	10	14.5	V	R69	4
Last Gate	VLG	0.4	3	7.7	V	R103	4

1. VDD may be switched to an alternate supply during integration; see Table 4.
2. VSS is set from 1 to 4 diode drops above AGND by populating 1-3 bypass resistors accordingly. Each resistor populated bypasses a diode. Default is 1 bypass resistor populated; therefore VSS is three diode drops above AGND.
3. VSUB is connected directly to AGND.
4. The Min and Max values shown refer to the adjustment range of the potentiometers on the Imager Board and may not be appropriate for proper device operation. For proper device operation the Nominal values should be used for all bias voltages.

Clock Voltages

The following clock voltage levels are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 4 were correct at the time of this document's publication, but may be subject to change; refer to the KAF−4320 device specification.

Table 4. CLOCK VOLTAGES

Description	Symbol	Level	Min	Nom	Max	Units	Potentiometer	Notes
Horizontal CCD Clock – Phase 1	H1_CCD	Low	−7.8	0	−0.7	V	R168	8
		High	0	10	10	V	R184	8
HCCD Last Gate Clock – Phase 1	H1L_CCD	Low		−4		V	R205	8
		High		6		V	R204	8
Horizontal CCD Clock – Phase 2	H2_CCD	Low	−7.8	−4	−0.7	V	R120	8
		High	0	6	10	V	R107	8
Vertical CCD Clock – Phase 1	V1_CCD	Low	−14	−8	−5	V	R57	5, 8
		High	0.2	0	4.2	V	R80	6, 8
Vertical CCD Clock – Phase 2	V2_CCD	Low	−14	−8	−5	V	R57	5, 8
		High	0.2	0	4.2	V	R80	6, 8
Reset Clock	RESET_CCD	Low	0.7	2	7.8	V	R194	8
		High	7.25	14	14.5	V	R174	8
VDD	ALT_VDD	Low	5	7	10	V	R158	7, 8
	VDD	High	15	21	21	V	R104	8

5. V1_CCD and V2_CCD low levels are controlled by the same potentiometer (R57).
6. V1_CCD and V2_CCD high levels are controlled by the same potentiometer (R80).
7. Controlled by AMP_ENABLE control line.
8. The Min and Max values shown refer to the adjustment range of the potentiometers on the Imager Board and may not be appropriate for proper device operation. For proper device operation the Nominal values should be used for all clock voltages.

Reset Clock Pulse Width

The pulsewidth of the RESET_CCD clock can be set by configuring the inputs to the programmable one−shot, P[2..0]. P[2..0] can be tied either high or low to achieve the desired pulse width by populating the resistors R192, R193, R200, and R201 accordingly.

Alternatively, the One−Shot can be left unpopulated and bypassed by a shorting resistor. In this configuration the pulse width of the RESET_CCD clock is set by the programmable logic on the Timing Generator Board. This is the default configuration.

Table 5. RESET CLOCK PULSE WIDTH

Pulse Width	P2	P1	P0	R192	R193	R200	R201	Notes
15 ns	0	0	0	IN	OUT	IN	OUT	
5 ns	0	0	1	OUT	IN	IN	OUT	
7.5 ns	0	1	0	IN	OUT	OUT	IN	
10 ns	0	1	1	OUT	IN	OUT	IN	
Set by Timing Generator Board								Default Configuration

Multiplexed VOUT Channel Select

If it is desired to utilize the 4:1 multiplexer circuit on the Imager Board, shorting resistors R7, R8, R18 and R25 must first be installed to connect the CCD video outputs to the multiplexer inputs. The multiplexer circuit presents a capacitive load to the video driver amplifiers of approximately 200 pF. This capacitive load will limit the bandwidth and slow down the transitioning of the CCD video output leaving the Imager Board. The overall system performance may be affected when the CCD video outputs are connected to the multiplexer circuit.

Any one of the four CCD VOUT signals can be selected and driven off the Imager Board via the multiplexed output SMB connector. The VOUT channel selection is controlled by the MUX[1..0] control line inputs from the Timing Generator Board.

Table 6. MULTIPLEXED VOUT CHANNEL SELECTION

MUX0	MUX1	VOUT MUX	Notes
0	0	VOUT3	Default Setting
1	0	VOUT2	
0	1	VOUT4	
1	1	VOUT1	

BLOCK DIAGRAM AND PERFORMANCE DATA

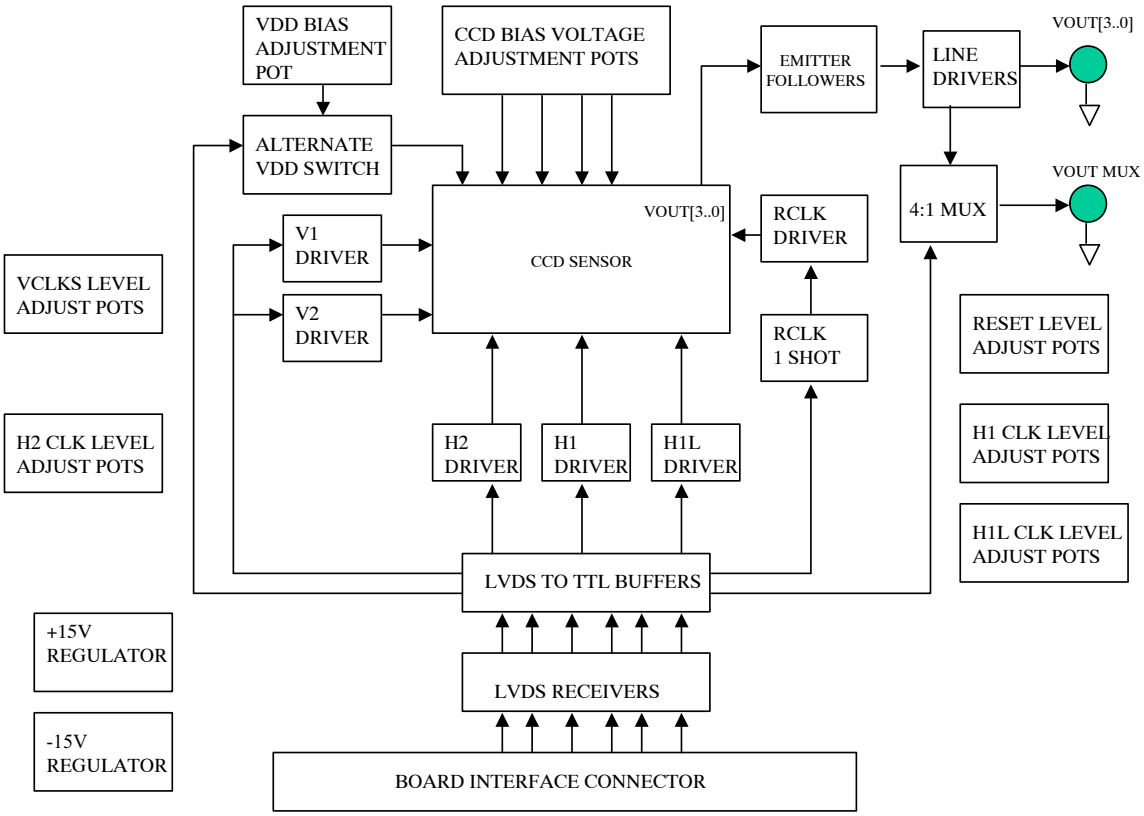

Figure 1. KAF−4320 Imager Board Block Diagram

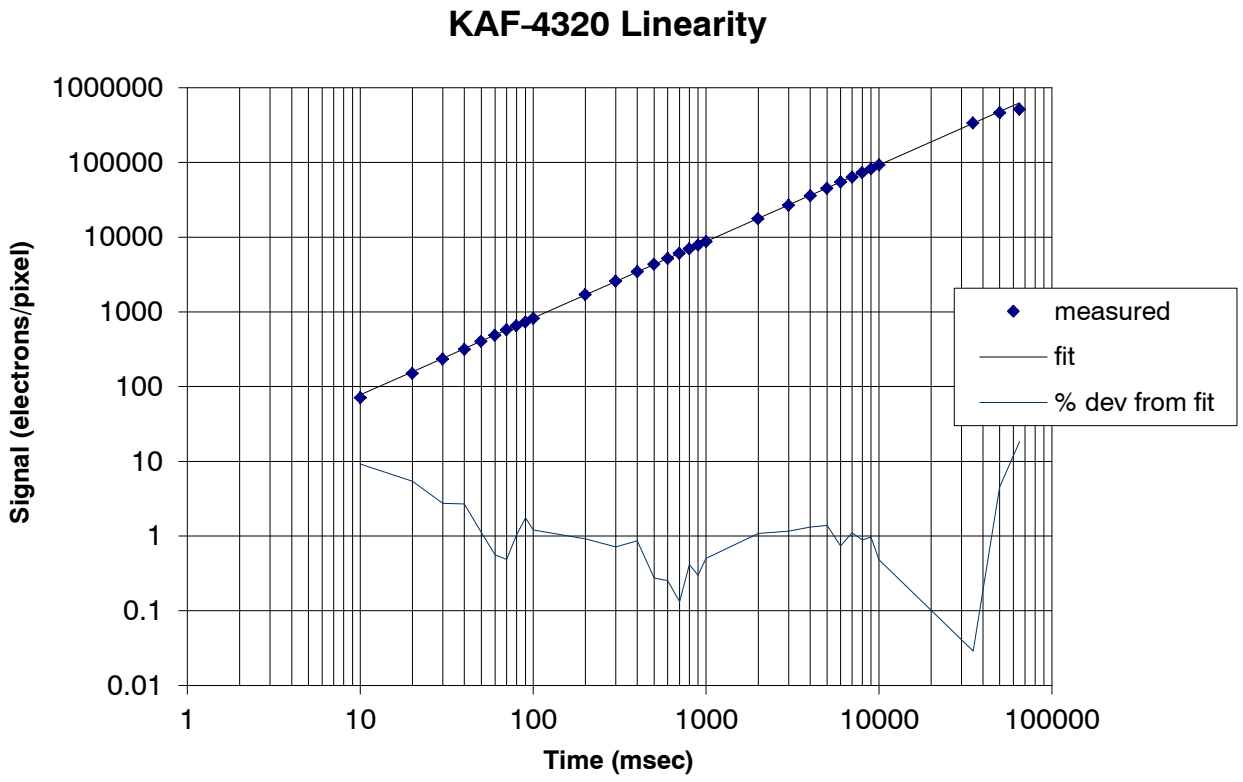

Figure 2. Measured Performance – Linearity

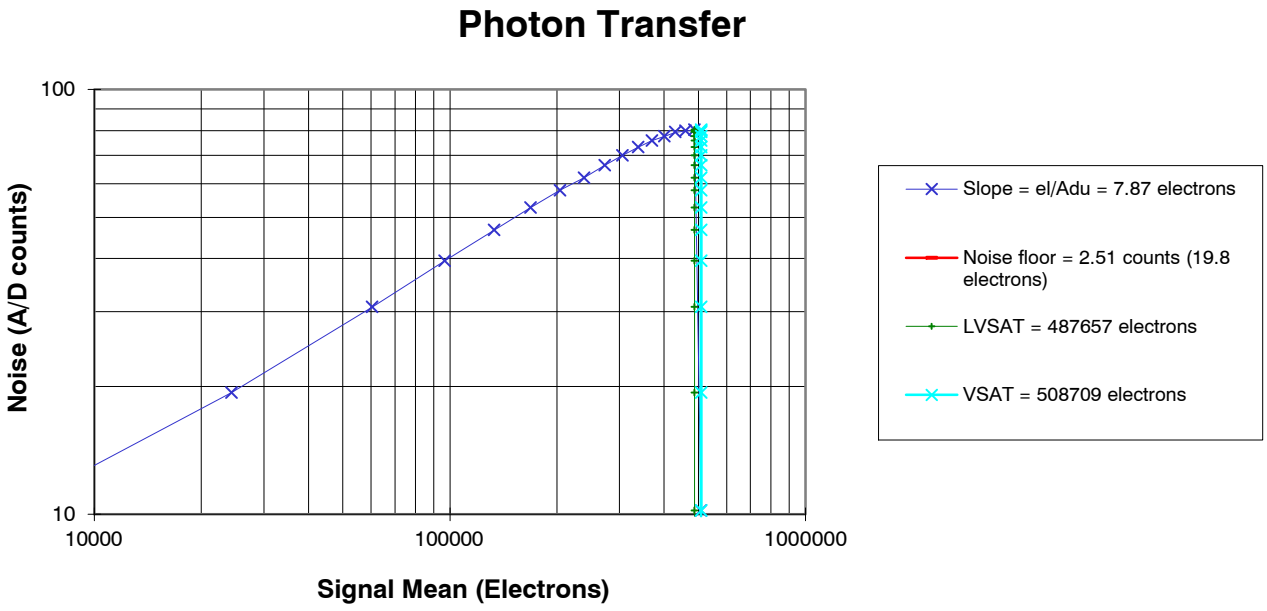

Figure 3. Measured Performance – Dynamic Range and Noise Floor

CONNECTOR ASSIGNMENTS AND PINOUTS

SMB Connectors J3−6

The emitter-follower buffered CCD_VOUT signals are driven from the Imager Board via the SMB connectors J3−6. Coaxial cable with a characteristic impedance of 75 Ω should be used to connect the imager board to the Timing Generator Board to match the series and terminating resistors used on these boards.

Table 7. J2 INTERFACE CONNECTOR PIN ASSIGNMENTS

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	AGND	4	AGND
5	TIMING_OUT11+	6	TIMING_OUT11−
7	AGND	8	AGND
9	TIMING_OUT10+	10	TIMING_OUT10−
11	AGND	12	AGND
13	TIMING_OUT9+	14	TIMING_OUT9−
15	AGND	16	AGND
17	TIMING_OUT8+	18	TIMING_OUT8−
19	AGND	20	AGND
21	TIMING_OUT7+	22	TIMING_OUT7−
23	AGND	24	AGND
25	TIMING_OUT6+	26	TIMING_OUT6−
27	AGND	28	AGND
29	TIMING_OUT5+	30	TIMING_OUT5−
31	AGND	32	AGND
33	TIMING_OUT4+	34	TIMING_OUT4−
35	AGND	36	AGND
37	TIMING_OUT3+	38	TIMING_OUT3−
39	AGND	40	AGND
41	TIMING_OUT2+	42	TIMING_OUT2−
43	AGND	44	AGND
45	TIMING_OUT1+	46	TIMING_OUT1−
47	N.C.	48	N.C.
49	AGND	50	AGND
51	N.C.	52	N.C.
53	VMINUS_MTR	54	VMINUS_MTR
55	N.C.	56	N.C.
57	AGND	58	AGND
59	TIMING_OUT0+	60	TIMING_OUT0−
61	−5 V_MTR	62	−5 V_MTR
63	N.C.	64	N.C.
65	AGND	66	AGND
67	N.C.	68	N.C.
69	+5 V_MTR	70	+5 V_MTR
71	N.C.	72	N.C.
73	AGND	74	AGND
75	N.C.	76	N.C.
77	VPLUS_MTR	78	VPLUS_MTR
79	N.C.	80	N.C.

Warnings and Advisories

ON Semiconductor is not responsible for customer damage to the Imager Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the Truesense Imaging Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of a an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

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