ESD Protection Diode

Ultra−Low Capacitance
Micro−Packaged Diodes for ESD Protection

ESD8472

The ESD8472 is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, high breakdown voltage, high linearity, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. It has industry leading capacitance linearity over voltage making it ideal for RF applications. This capacitance linearity combined with the extremely small package and low insertion loss makes this part well suited for use in antenna line applications for wireless handsets and terminals.

Features

- Industry Leading Capacitance Linearity Over Voltage
- Ultra−Low Capacitance: 0.2 pF
- Insertion Loss: 0.030 dBm
- Small Footprint: 0.62 mm x 0.32 mm
- Stand−off Voltage: 5.3 V
- Low Leakage: < 1 nA
- Low Dynamic Resistance: < 1 Ω
- 1000 ESD IEC61000−4−2 Strikes ±8 kV Contact / Air Discharged
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

Typical Applications

- RF Signal ESD Protection
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications
- USB 2.0, USB 3.0

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
IEC 61000−4−2 Level 4 (Contact) (Note 1) IEC 61000−4−2 Level 4 (Air) (Note 1)	ESD	±20 ±20	kV
Maximum Peak Pulse Current IEC 61000−4−5 8/20 μs (Lightning) (Note 2)	I_{PP}	2.4	A
Total Power Dissipation (Note 3) @ T_A = 25°C Thermal Resistance, Junction−to−Ambient	P_D $R_{\theta JA}$	300 400	mW °C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

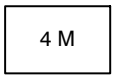
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−2 waveform.
2. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−5 waveform.
3. Mounted with recommended minimum pad size, DC board FR−4

X3DFN2
CASE 152AF

MARKING DIAGRAM

PIN 1



4 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
ESD8472MUT5G	X3DFN2 (Pb−Free)	10000 / Tape & Reel
SZESD8472MUT5G	X3DFN2 (Pb−Free)	15000 / Tape & Reel

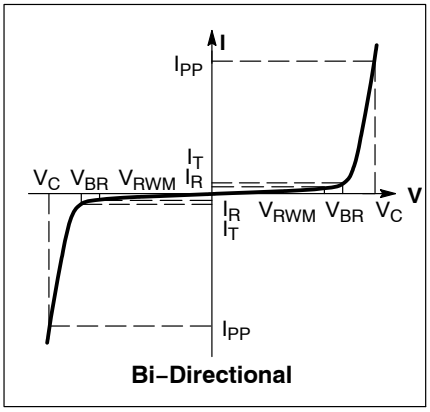
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				5.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA (Note 4)	7.0		12	V
Reverse Leakage Current	I_R	V_{RWM} = 5.3 V		< 1	50	nA
Clamping Voltage	V_C	I_{PP} = 1 A (Note 5)		11	15	V
Clamping Voltage	V_C	I_{PP} = 2.4 A (Note 5)		15	17.8	V
ESD Clamping Voltage	V_C	Per IEC61000−4−2	See Figures 1 and 2			
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz V_R = 0 V, f = 1 GHz		0.20 0.15	0.30 0.30	pF
Dynamic Resistance	R_{DYN}	TLP Pulse		0.75		Ω
Insertion Loss		f = 1 MHz f = 8.5 GHz		0.050 0.250		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
5. Non−repetitive current pulse at 25°C, per IEC61000−4−5 waveform (Figure 9).

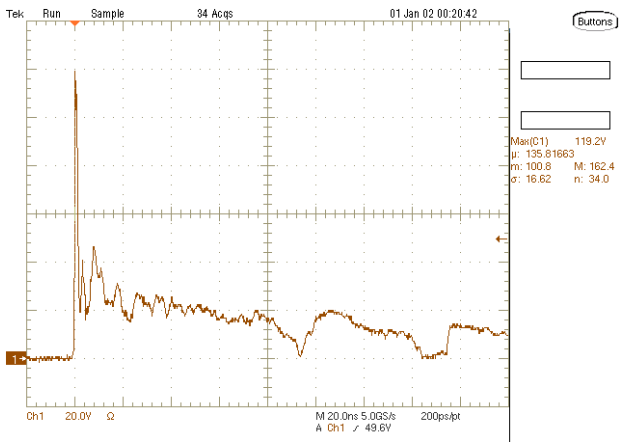


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

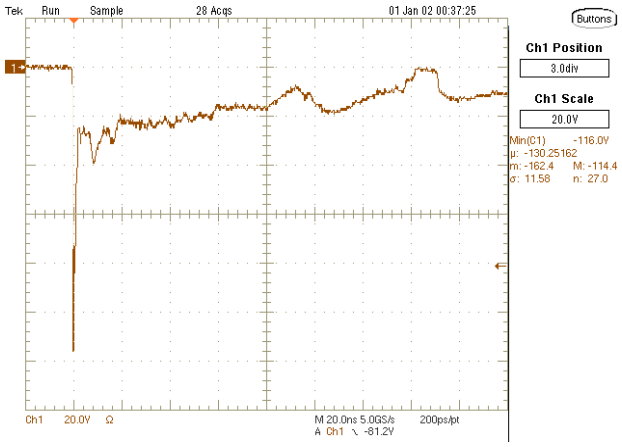


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

TYPICAL CHARACTERISTICS

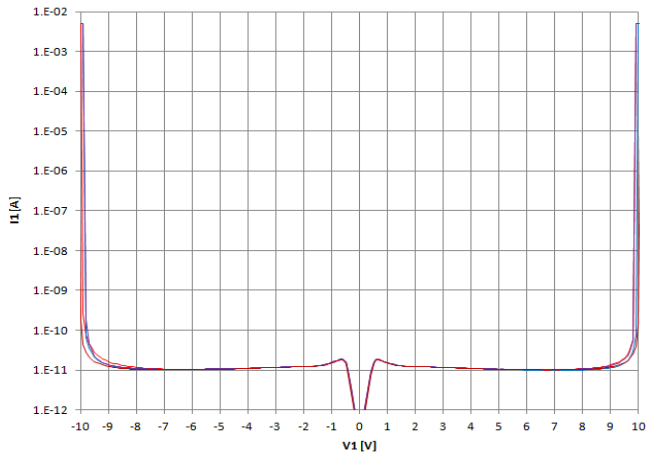


Figure 3. IV Characteristics

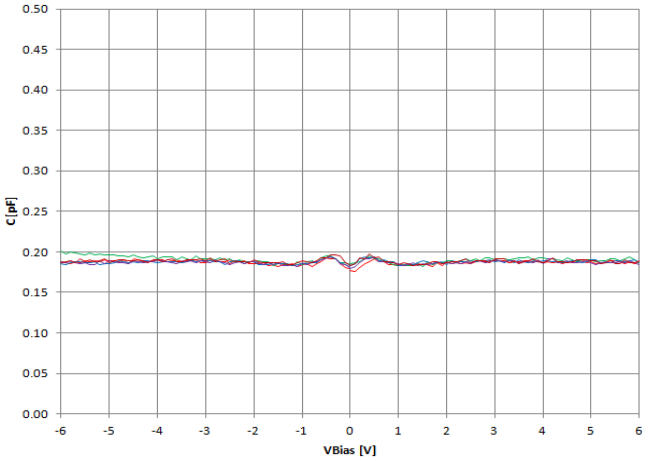


Figure 4. CV Characteristics

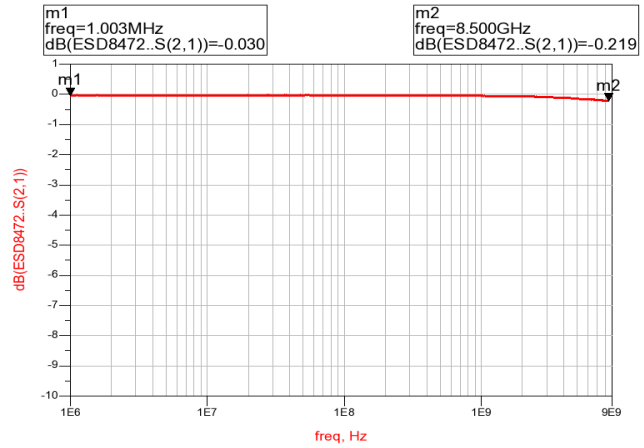


Figure 5. RF Insertion Loss

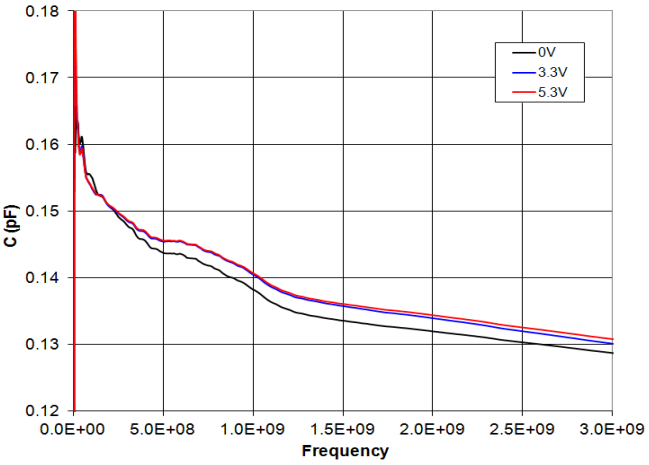


Figure 6. Capacitance over Frequency

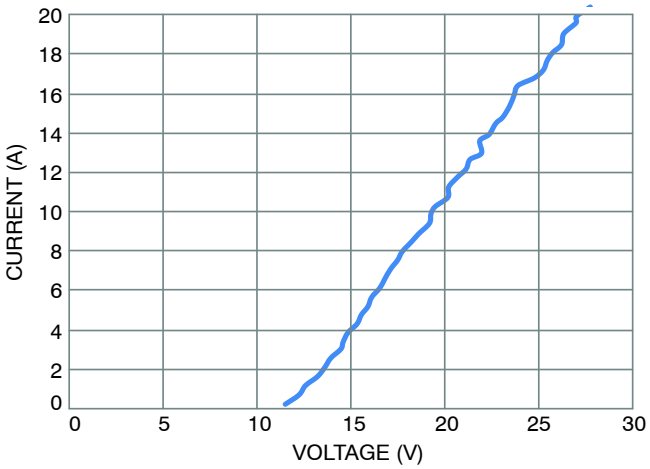


Figure 7. Positive TLP I−V Curve

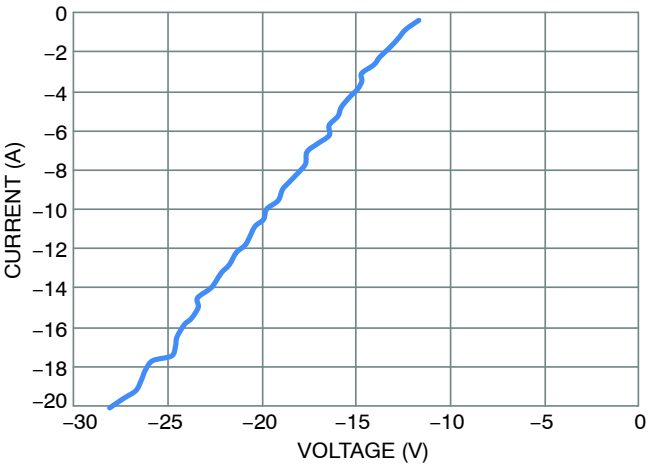


Figure 8. Negative TLP I−V Curve

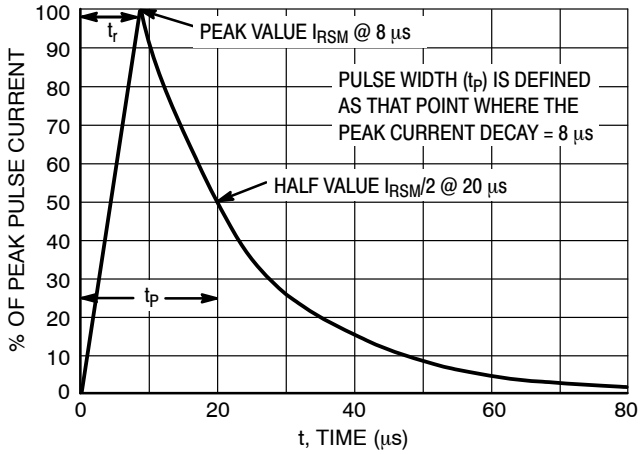
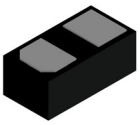
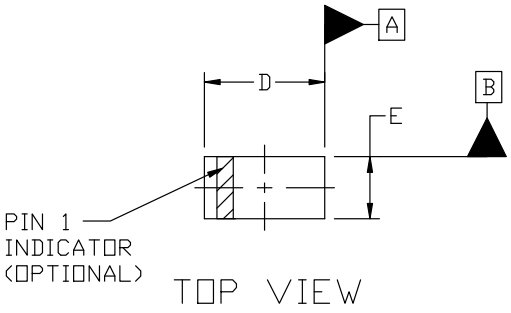


Figure 9. IEC 61000−4−5 8/20 μs Pulse Waveform

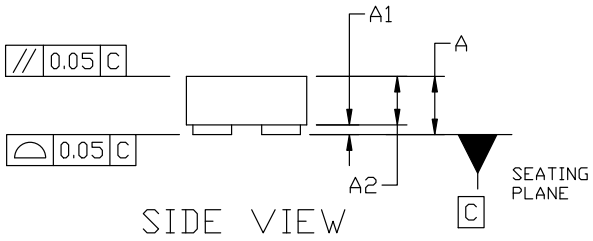


X3DFN2 0.62x0.32x0.24, 0.35P
CASE 152AF
ISSUE C

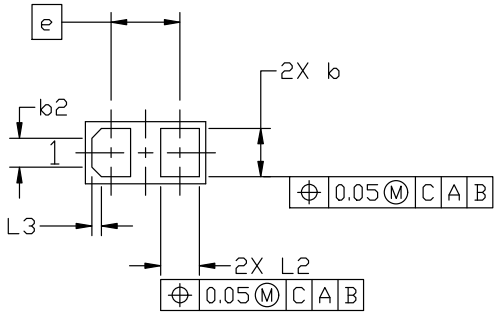
DATE 08 AUG 2023



TOP VIEW



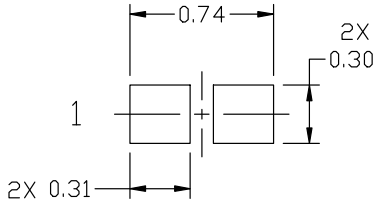
SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 0201

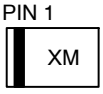
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.25	0.29	0.33
A1	0.00	---	0.05
A2	0.14	0.24	0.34
b	0.22	0.25	0.28
b2	0.150 REF		
D	0.58	0.62	0.66
E	0.28	0.32	0.36
e	0.355 BSC		
L2	0.17	0.20	0.23
L3	0.050 REF		



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**X3DFN2 0.62x0.32x0.24, 0.35P**		**PAGE 1 OF 1**

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