



ON Semiconductor®

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LV52204MT

Bi-CMOS IC

LED Boost Driver with PWM and 1-Wire Dimming

Overview

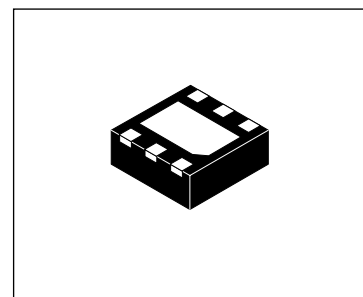
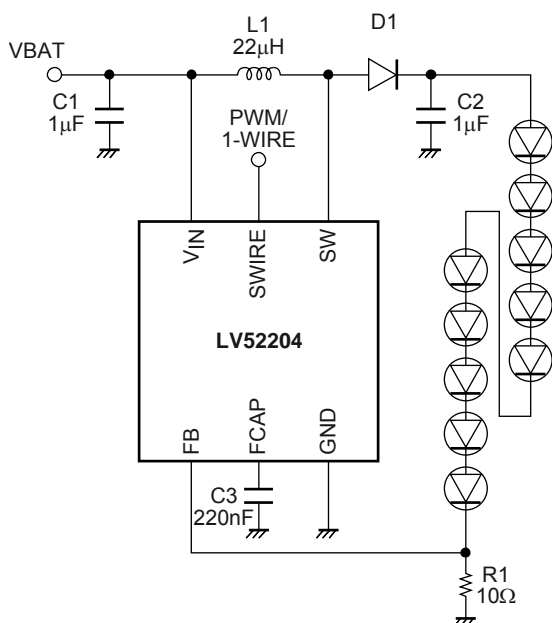
The LV52204MT is a high voltage boost driver for LED drive. LED current is set by the external resistor R1 and LED dimming can be done by changing FB voltage with PWM or 1-Wire.

Features

- Operating Voltage from 2.7V to 5.5V
- 1-Wire 32 level digital and PWM dimming
- Integrated 40V MOSFET
- 600kHz Switching Frequency

Typical Applications

- LED Display Backlight Control



WDFN6 2x2, 0.65P

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|-----------------|-------------|------|
| Maximum supply voltage | V _{CC} max | V _{CC} | 6.0 | V |
| Maximum pin voltage1 | V1 max | SW | 40 | V |
| Maximum pin voltage2 | V2 max | Other pin | 5.5 | V |
| Allowable power dissipation | Pd max | Ta = 25°C *1 | 2.05 | W |
| Operating temperature | Topr | | -30 to +85 | °C |
| Storage temperature | Tstg | | -55 to +125 | °C |

*1 Mounted on a specified board: 70mm×50mm×1.2mm (4 layer glass epoxy)

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommendation Operating Condition at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------|--------------------|-------------------------------------|-------------|------|
| Supply voltage range1 | V _{CC} op | V _{CC} | 2.7 to 5.5 | V |
| PWM frequency | Fpwm | PWM MODE | 300 to 100k | Hz |
| PWM minimum duty | Fduty | 10kHz, VIN ≥ 3.3V, -30°C to 85°C *2 | 2 | % |
| | | 20kHz, VIN ≥ 3.3V, -30°C to 85°C *2 | 4 | % |
| | | 30kHz, VIN ≥ 3.3V, -30°C to 85°C *2 | 6 | % |

*2 Guaranteed by design

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics Analog block at Ta = 25°C, V_{CC} = 3.6V, unless otherwise specified

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--------------------------------------|-------------------|---|---------|-----|-----------------|------|
| | | | min | typ | max | |
| Standby current dissipation | I _{CC} 1 | SHUTDOWN | | 0 | 5 | μA |
| DC/DC current dissipation | I _{CC} 2 | V _{OUT} = 30V, I _{LED} = 20mA | | | 1 | mA |
| FB voltage | Vfb | PWM duty 100% | 0.19 | 0.2 | 0.21 | V |
| FB pin leak current | I _{fb} | | | | 1 | μA |
| OVP voltage | Vovp | SW | 37 | 38 | 39 | V |
| SWOUT ON resistance | Ron | IL = 100mA | | 700 | | mΩ |
| NMOS switch current limit | ILIM | Vfb = 200mV | | 0.7 | | A |
| OSC frequency | Fosc | | | 600 | | kHz |
| High level input voltage | V _{INH} | SWIRE | 1.5 | | V _{CC} | V |
| Low level input voltage | V _{INL} | SWIRE | 0 | | 0.4 | V |
| Under voltage lockout | Vuvlo | V _{IN} falling | | 2.2 | | V |
| SWIRE output voltage for Acknowledge | Vack | Rpullup = 15kΩ | | | 0.4 | V |

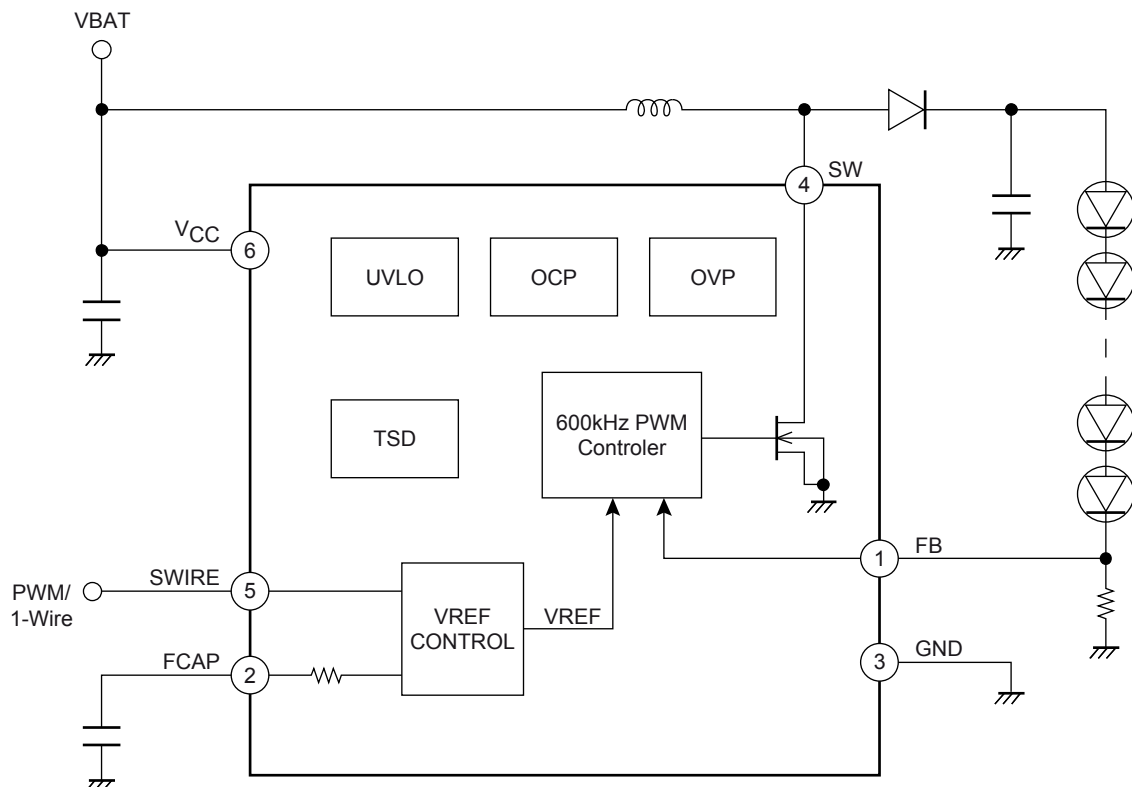
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Recommended SWIRE Timing at $T_a = 25^\circ\text{C}$, $V_{CC} = 3.6\text{V}$, unless otherwise specified

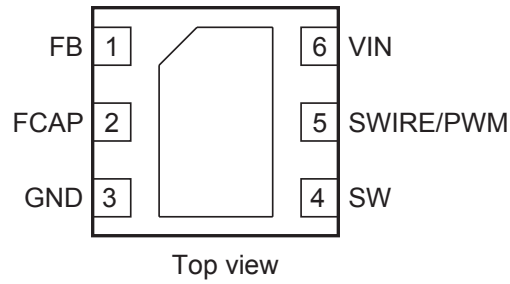
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|--------|--|-----------------------|-----|-----|---------------|
| | | | min | typ | max | |
| SWIRE setup time1 from shutdown | Ton1 | PWM duty more than 2%, $V_{IN} \geq 3.3\text{V}$, -30°C to 85°C *3 | 2 | | | μs |
| SWIRE setup time2 from shutdown | Ton2 | | 20 | | | μs |
| SWIRE mode selectable time | Tsel | | 1 | | 2.2 | ms |
| SWIRE delay time to start digital mode detection | Tw0 | | 100 | | | μs |
| SWIRE low time to switch to digital mode | Tw1 | | 260 | | | μs |
| SWIRE low time to shutdown | Toff | | 8.9 | | | ms |
| SWIRE start time for digital mode programming | Tstart | | 2 | | | μs |
| SWIRE end time for digital mode programming | Tend | | 2 | | 360 | μs |
| SWIRE High time of bit 0 | Th0 | Bit detection = 0 | 2 | | 180 | μs |
| SWIRE Low time of bit 0 | TI0 | Bit detection = 0 | $\text{Th0} \times 2$ | | 360 | μs |
| SWIRE High time of bit 1 | Th1 | Bit detection = 1 | $\text{TI1} \times 2$ | | 360 | μs |
| SWIRE Low time of bit1 | TI1 | Bit detection = 1 | 2 | | 180 | μs |
| DCDC startup delay | Tdel | | | 2 | | ms |
| Delay time of Acknowledge | Tackd | | | | 2 | μs |
| Duration of Acknowledge | Tack | | | | 512 | μs |

*3 Guaranteed by design

Block Diagram

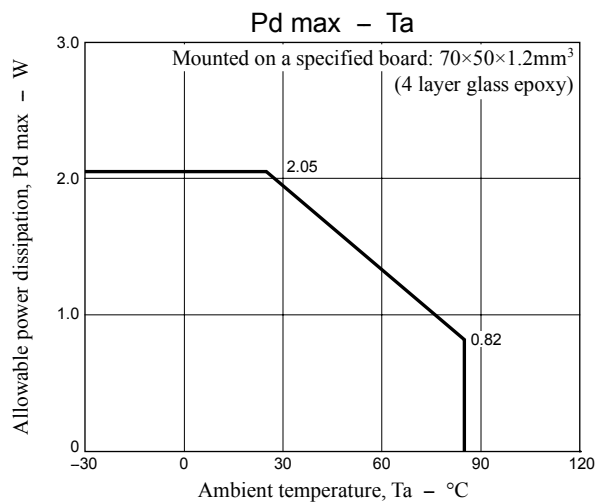


Pin Connections



Pin Function

| PIN # | Pin Name | Description |
|-------|-----------------|---|
| 1 | FB | Feedback pin. |
| 2 | FCAP | Filtering capacitor terminal for PWM mode. |
| 3 | GND | Ground |
| 4 | SW | Switch pin. Drain of the internal power FET. |
| 5 | SWIRE | 1-wire dimming control and PWM dimming input (active High). |
| 6 | V _{CC} | Supply voltage. |
| | Expose-pad | Connect to GND on PCB. |



LED Current Setting

LED current is set by an external resistor connected between the FB pin and ground.

$$I_{LED} = V_{FB}/R_{FB}.$$

The V_{FB} can be controlled by two dimming modes, PWM Mode or Digital Mode. In PWM mode, PWM input is converted into a near DC current by the internal resistor R that was equivalent to $60k\Omega (\pm 10\%)$ and the external capacitor C_{FCAP} as a low pass filter with a cut-off frequency $f_c = 1/2\pi R_{FCAP}$. The V_{FB} can be adjusted by altering the duty cycle of the PWM signal (See Fig.1).

$$V_{FB} = 200 \text{ (mV)} \times \text{PWM Duty (\%)}$$

On the other hand, V_{FB} can be selected one from among 32 steps in Digital Mode (See Fig.2).

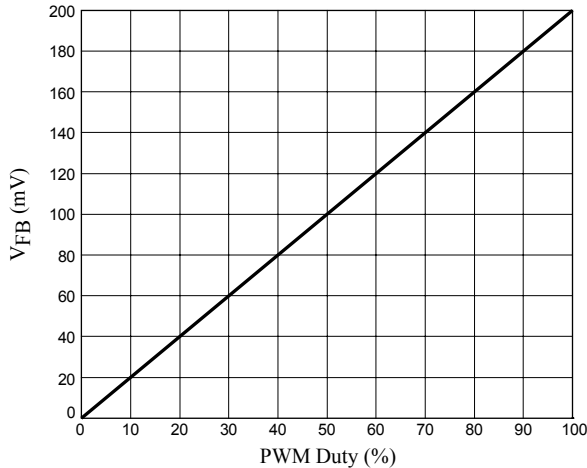


Fig1. V_{FB} vs. PWM Duty (PWM mode)

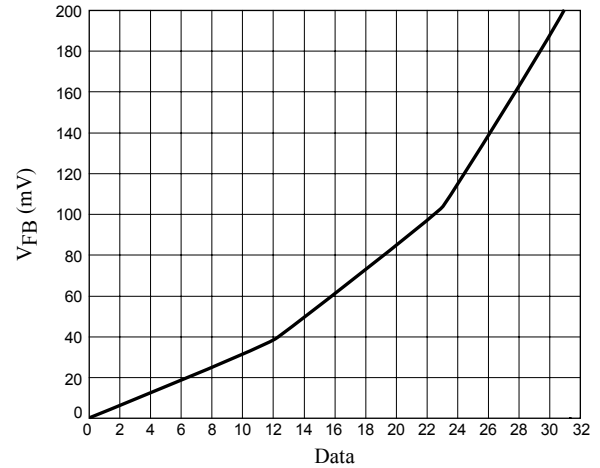


Fig2. V_{FB} vs. Data Register Value (Digital mode)

Dimming Mode Selection

Dimming Mode is selected by a specific pattern of the SWIRE within T_{sel} (1ms) from the startup of the device every time. In order to startup the device, the SWIRE must keep high for longer than T_{on} .

PWM Mode

The dimming mode is set to PWM mode when it is not recognized as a digital mode within T_{sel} . To enter Digital Mode, the SWIRE is required keeping in low state for T_{w1} (See Fig.4). If the PWM frequency is used faster than 6.6kHz, the dimming mode is set to PWM mode only. But slower than 6.6kHz, it is necessary to avoid entering the digital mode condition, such as SWIRE keeps high for longer than T_{sel} . PWM is enabled after T_{del} from T_{sel} .

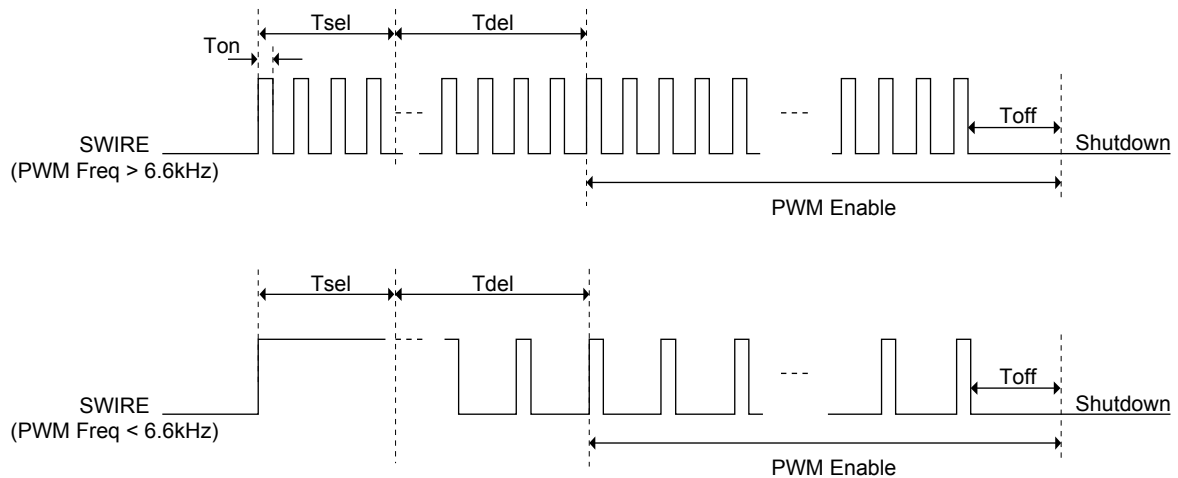


Fig3. SWIRE Timing Diagram in PWM mode

Digital Mode

To enter Digital Mode, SWIRE should be taken high for more than T_{w0} (100 μ s) from the first rising edge and keep low state for T_{w1} (260 μ s) before T_{sel} (1ms).

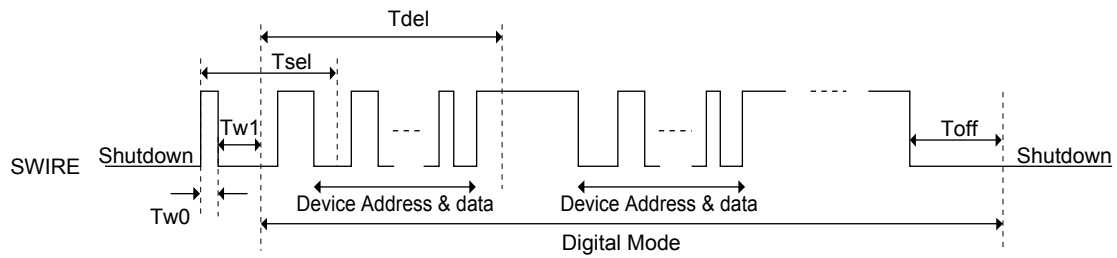


Fig4. SWIRE Timing Diagram in Digital mode

It is required sending the device address byte and the data byte to select V_{FB} . The bit detection is determined by the ratio of T_h and T_l (See Fig6). The start condition for the bit transmission required SWIRE high for at least T_{start} . The end condition is required SWIRE low for at least T_{end} . When data is not being transferred, SWIRE is set in the “H” state. These registers are initialized with POR (Power On Reset).

In the LV52204MT, the device address (DA7 to DA0) is specified as “01110010”. D7 is setting for the acknowledge response. If the device address and the data byte are transferred on $D7 = 1$, the ACK signal is sent from the receive side to the send side. The acknowledge signal is issued when SWIRE on the send side is released and SWIRE on the receive side is set to low state. D6 and D5 need to send 0. D4 to D0 allow to changing the FB voltage.

| | Register | BIT | Description |
|----------------|----------|-----|-------------|
| Device Address | DA7 | 7 | 0 |
| | DA6 | 6 | 1 |
| | DA5 | 5 | 1 |
| | DA4 | 4 | 1 |
| | DA3 | 3 | 0 |
| | DA2 | 2 | 0 |
| | DA1 | 1 | 1 |
| | DA0 | 0 | 0 |

Table1. Device Address Description

| | Register | BIT | Description |
|------|----------|-----|---|
| Data | D7 | 7 | 0 = Acknowledge disabled 1 = Acknowledge enabled |
| | D6 | 6 | 0 |
| | D5 | 5 | 0 |
| | D4 | 4 | Data bit 4 |
| | D3 | 3 | Data bit 3 |
| | D2 | 2 | Data bit 2 |
| | D1 | 1 | Data bit 1 |
| | D0 | 0 | Data bit 0 |

Table2. Data Description

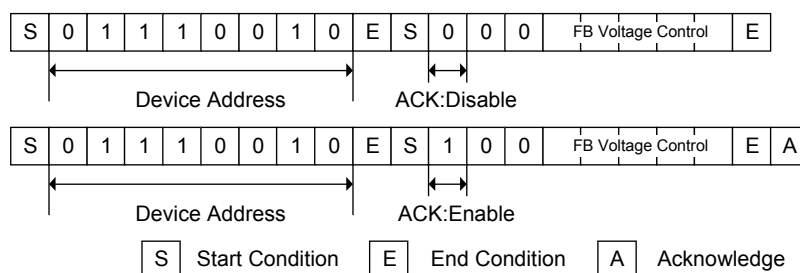


Fig5. Example of writing data

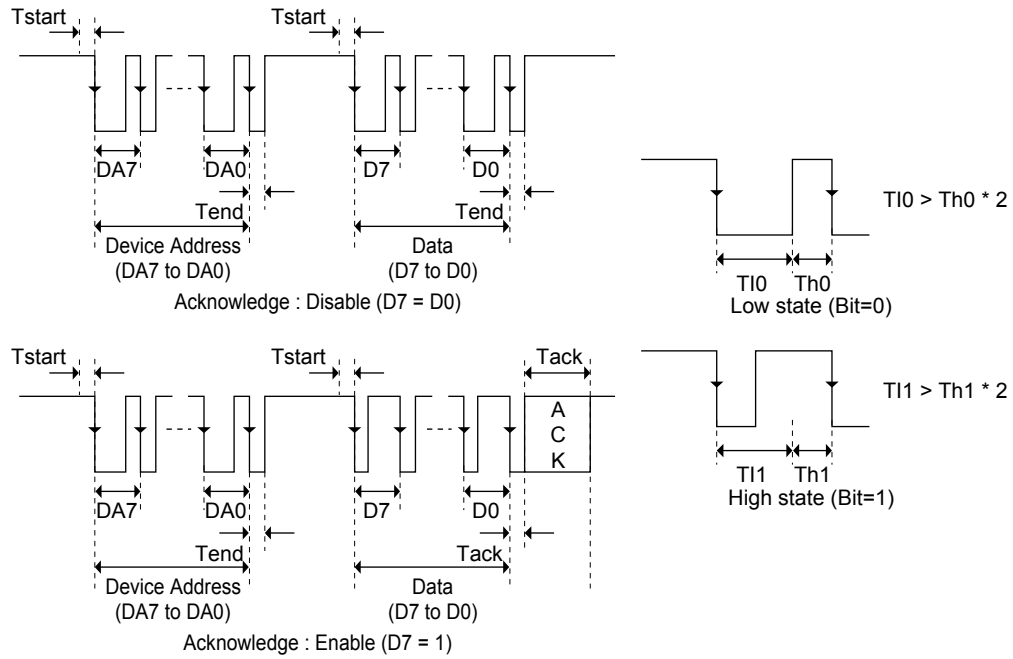


Fig6.Bit detection Diagram

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FB voltage (mV) |
|----|-----|----|----|----|----|----|----|----|-----------------|
| 0 | 1/0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1/0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 5 |
| 2 | 1/0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 8 |
| 3 | 1/0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 11 |
| 4 | 1/0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 14 |
| 5 | 1/0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 17 |
| 6 | 1/0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 20 |
| 7 | 1/0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 23 |
| 8 | 1/0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 26 |
| 9 | 1/0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 29 |
| 10 | 1/0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 32 |
| 11 | 1/0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 35 |
| 12 | 1/0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 38 |
| 13 | 1/0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 44 |
| 14 | 1/0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 50 |
| 15 | 1/0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 56 |
| 16 | 1/0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 62 |
| 17 | 1/0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 68 |
| 18 | 1/0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 74 |
| 19 | 1/0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 80 |
| 20 | 1/0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 86 |
| 21 | 1/0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 92 |
| 22 | 1/0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 98 |
| 23 | 1/0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 104 |
| 24 | 1/0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 116 |
| 25 | 1/0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 128 |
| 26 | 1/0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 140 |
| 27 | 1/0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 152 |
| 28 | 1/0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 164 |
| 29 | 1/0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 176 |
| 30 | 1/0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 188 |
| 31 | 1/0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | *200 |

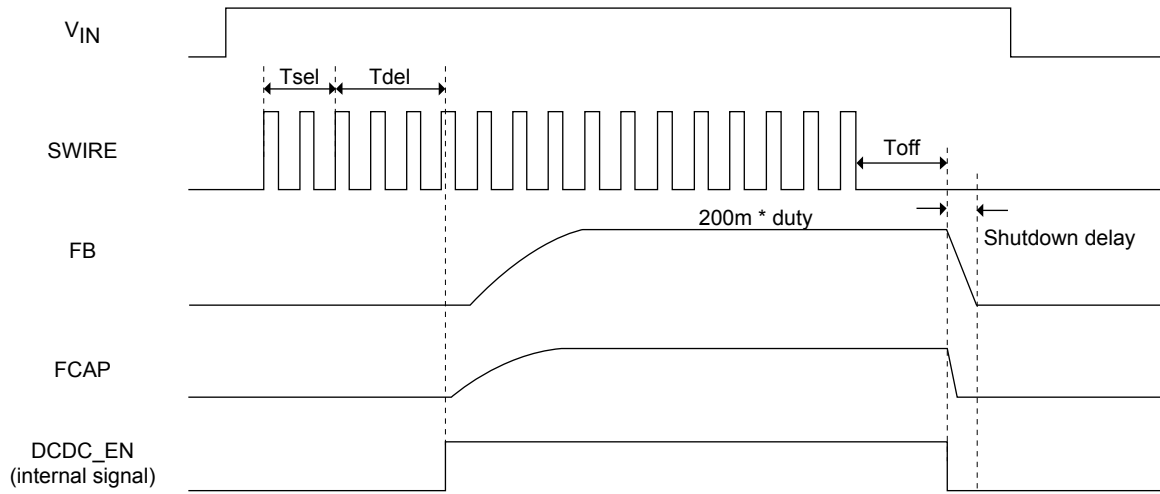
(*Default)

Table3. Data Register vs. FB Voltage

Start up and Shutdown

The device becomes enabled when SWIRE is initially taken high. The dimming mode is determined within T_{sel} and the boost converter start up after T_{del} . To place the device into shutdown mode, the SWIRE must be held low for T_{off} .

PWM MODE



Digital MODE

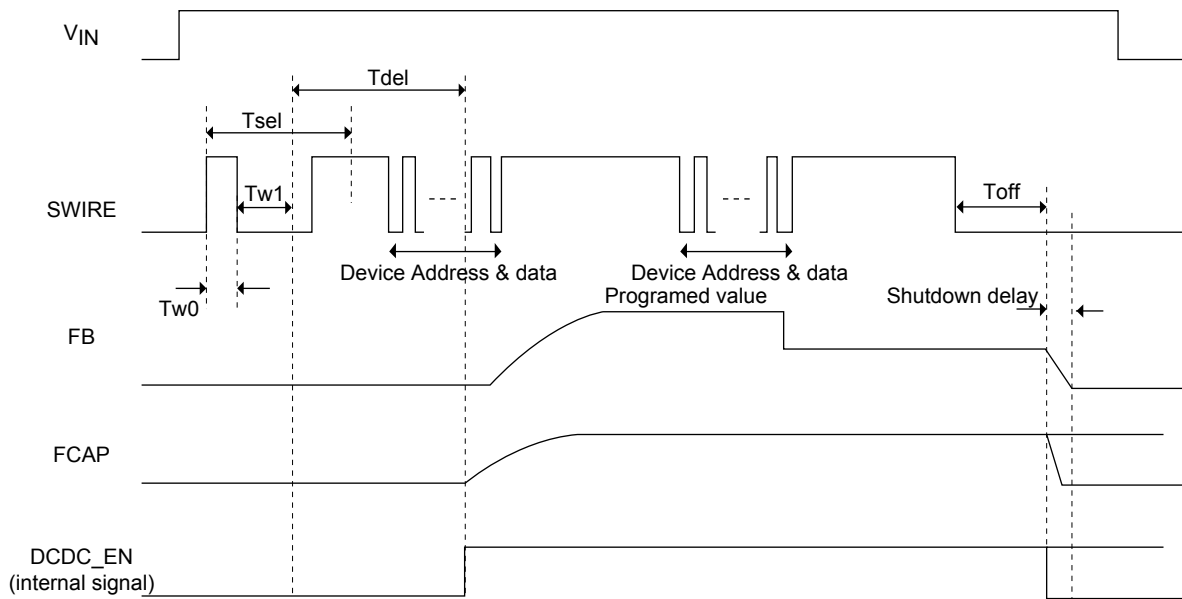


Fig7.Start up and shutdown diagram

Open LED Protection

If SW terminal voltage exceeds a threshold V_{ovp} (38V typ) for 8 cycles, boost converter enters shutdown mode. In order to restart the IC, SWIRE signal is required again.

Over Current Protection

Current limit value for built-in power MOS is around 0.7A. The power MOS is turned off for each switching cycle when peak current through it exceeds the limit value.

Under Voltage Lock Out (UVLO)

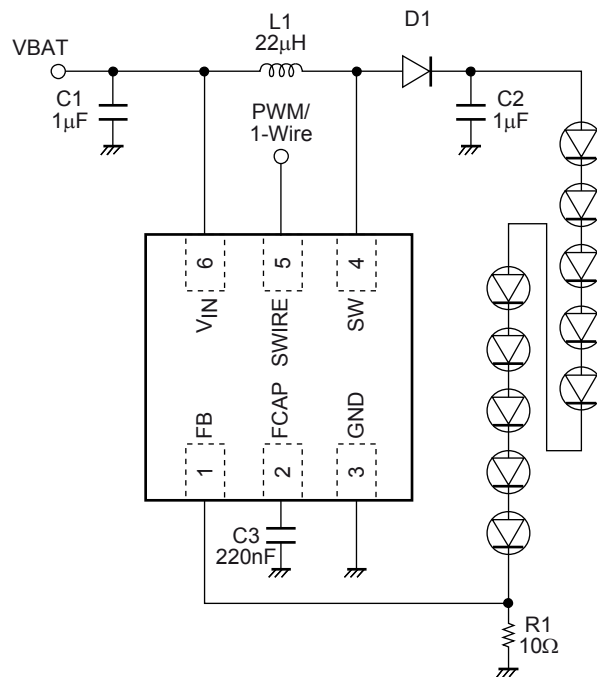
UVLO operation works when V_{IN} terminal voltage is below 2.2V.

Thermal Shutdown

When chip temperature is too high, boost converter is stopped.

Application Circuit Diagram

10LEDs

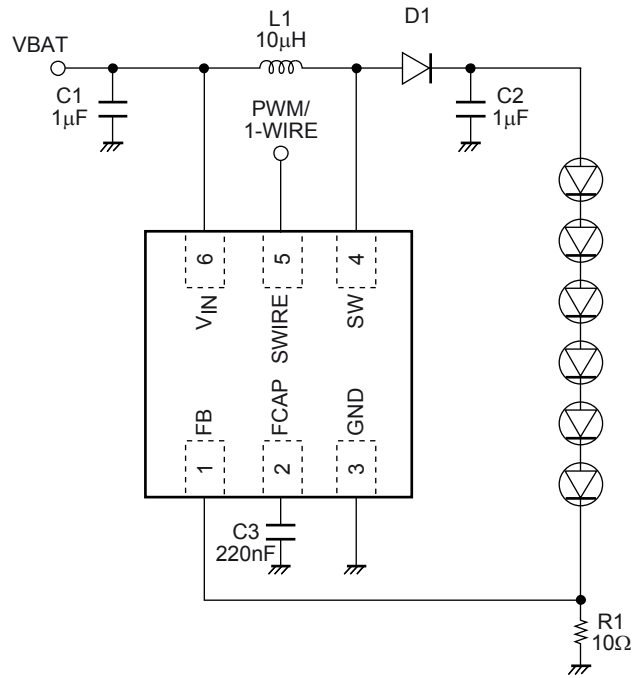


L1: VLS3012T-220M49 (TDK), VLF504015MT-220M (TDK)

D1: MBR0540T1 (ON semi), NSR05F40 (ONsemi)

C2: GRM21BR71H105K (Murata), C1608X5R1H105K (TDK)

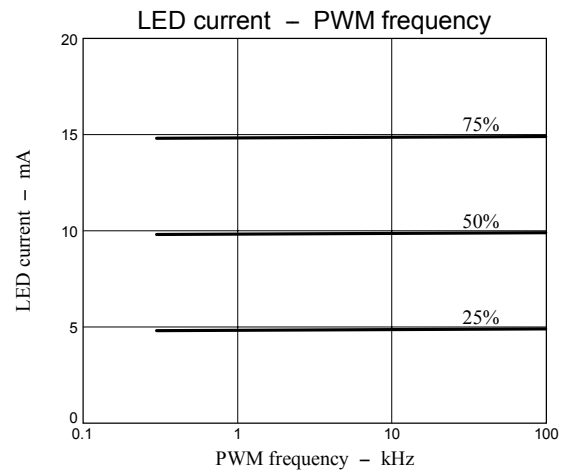
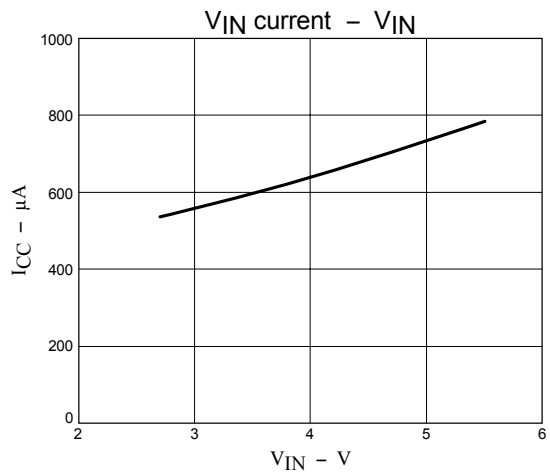
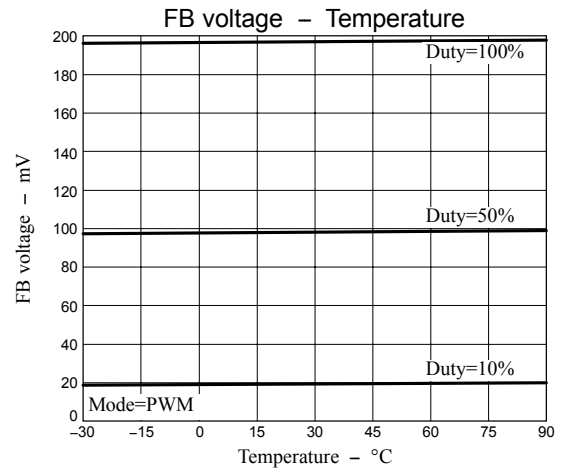
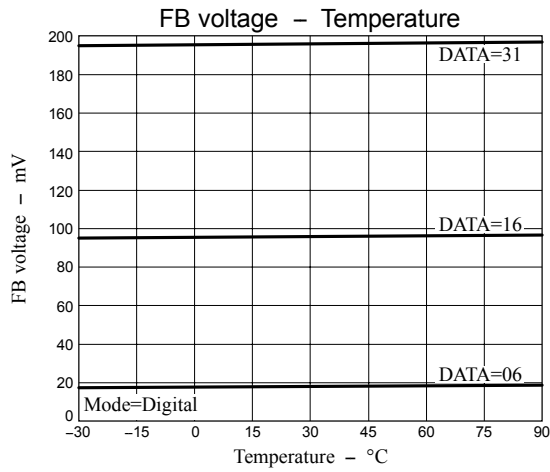
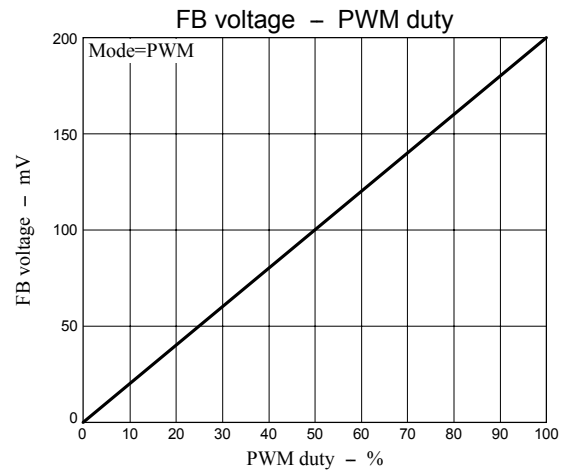
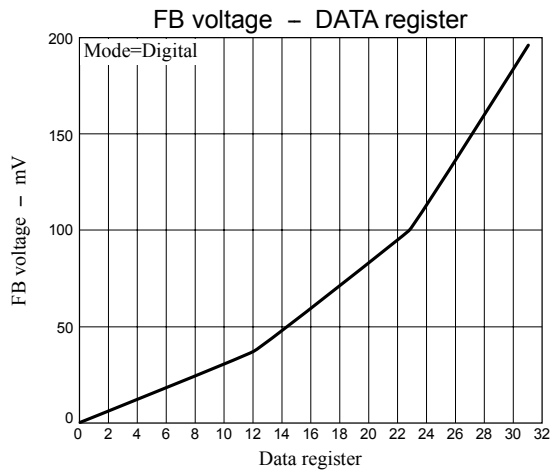
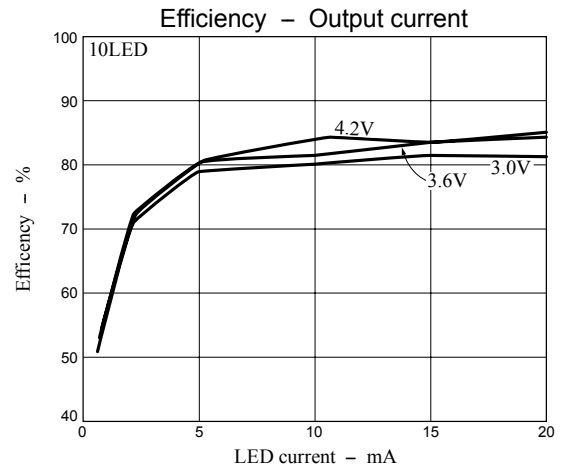
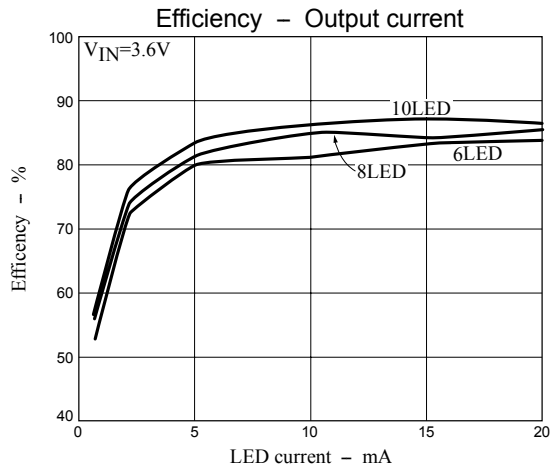
6LEDs



L1: VLS3012T-100M72 (TDK), VLF302512M-100M (TDK)
D1: MBR0540T1 (ON semi), NSR05F40 (ONsemi)
C2: GRM21BR71H105K (Murata), C1608X5R1H105K (TDK)

LV52204MT

Typical Characteristics ($V_{IN} = 3.6V$, $L = 22\mu H$, $T = 25^\circ C$, unless otherwise specified)

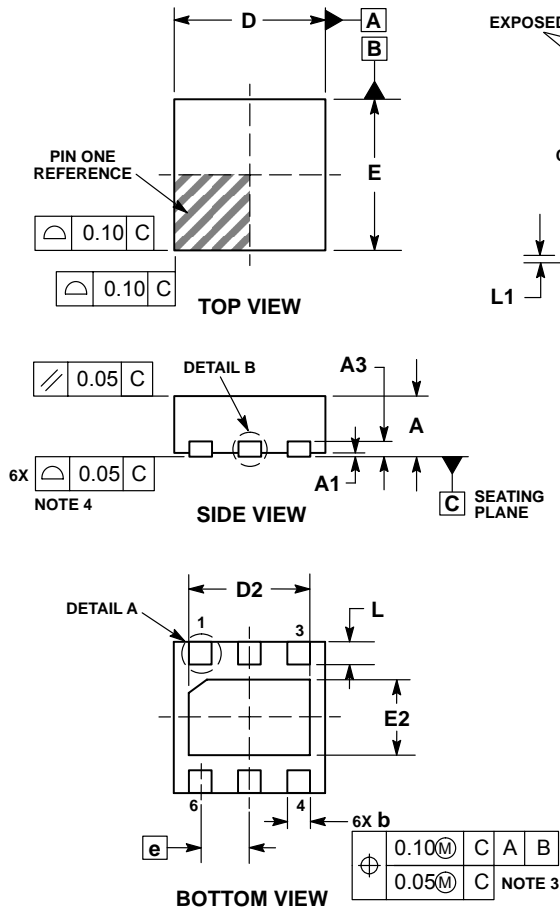


PACKAGE DIMENSIONS

WDFN6 2x2, 0.65P

CASE 511BR-01

ISSUE O

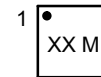


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 2.00 BSC | |
| D2 | 1.50 | 1.70 |
| E | 2.00 BSC | |
| E2 | 0.90 | 1.10 |
| e | 0.65 BSC | |
| L | 0.20 | 0.40 |
| L1 | --- | 0.15 |

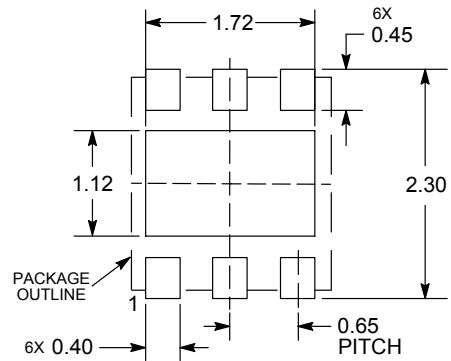
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, G or microdot ■, may or may not be present.

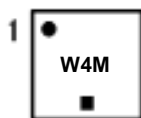
RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

LV52204MT is as follows.

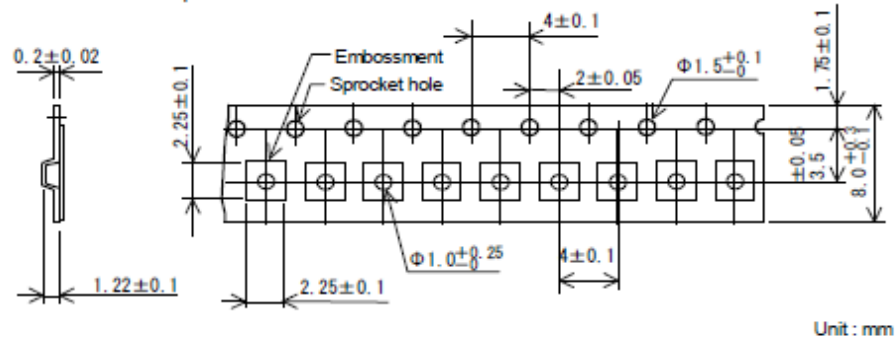
MARKING DIAGRAM



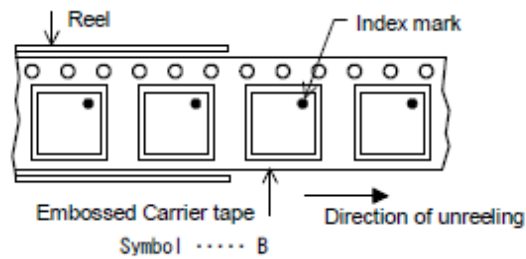
W4 = Device Code
M = Date Code
■ = Pb-Free Package

1.EMBOSSSED CARRIER TAPING

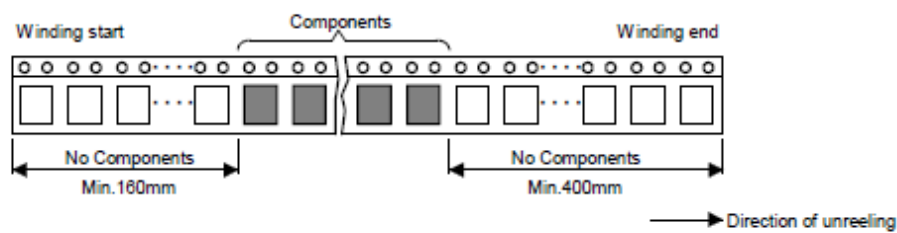
1 - 1 .Embossed carrier tape dimensions



1 -2 .Tape mounting direction



1 - 3 .Reel winding start and reel winding end



Packing Specification of Embossed Carrier Taping

P2/3

WDFN6(2.0*2.0) 3,000 pcs/reel

2.TAPE STRENGTH

2 - 1 .Tensile strength of the carrier tape : Min.10N

2 - 2 .Peel strength of the top cover tape

(a)Peel angle : 165° to 180° relative to the tape adhesive surface

(b)Peel rate : 300mm / minute

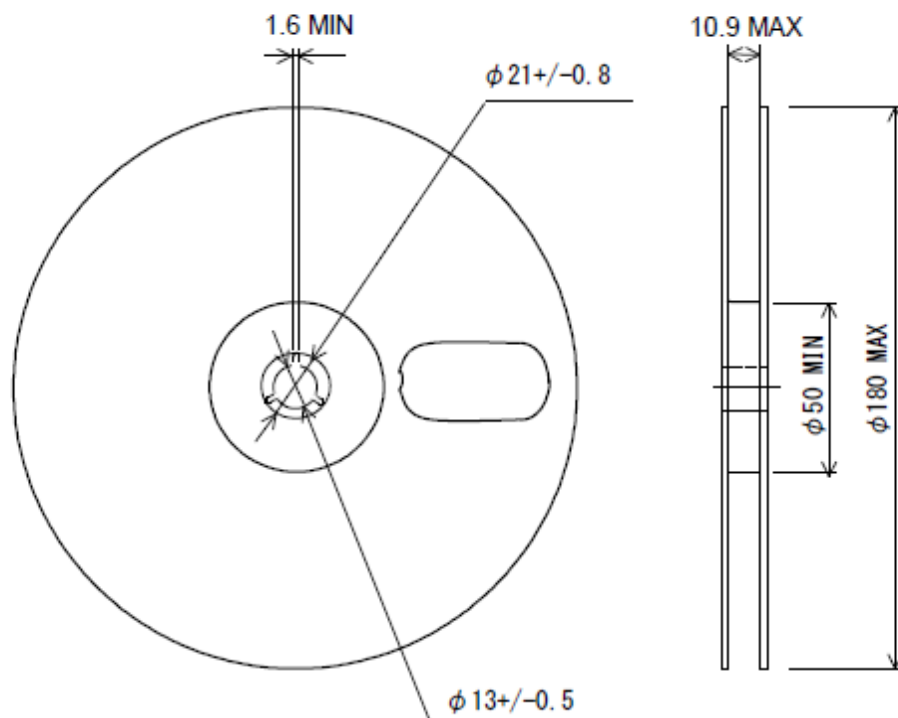
(c)Peel of strength : 0.1N to 1.0N

3 .PARTS No. ON BAR CODE LABEL

Type number T B G

Direction indication ↑ ↑ LEAD FREE symbol

4 .REEL DIMENSIONS



TYPE:P-RRM-08B

UNIT:mm

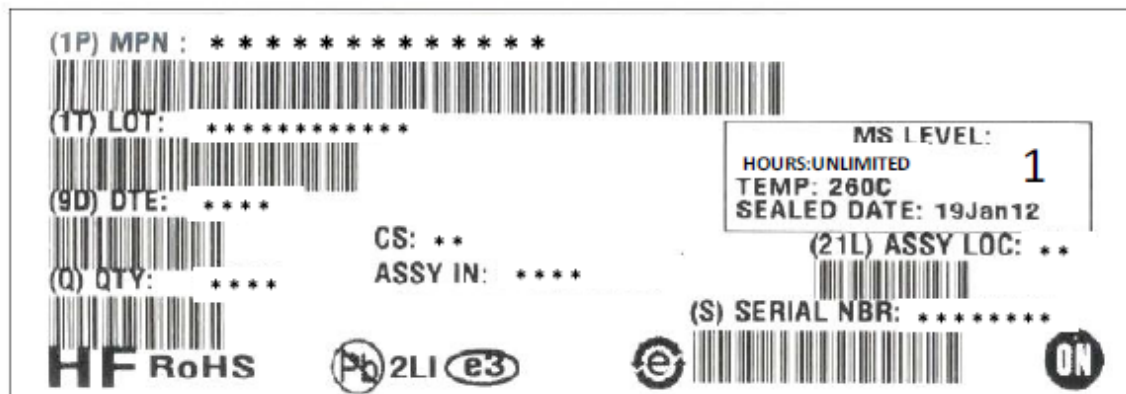
Packing Specification of Embossed Carrier Taping

P3/3

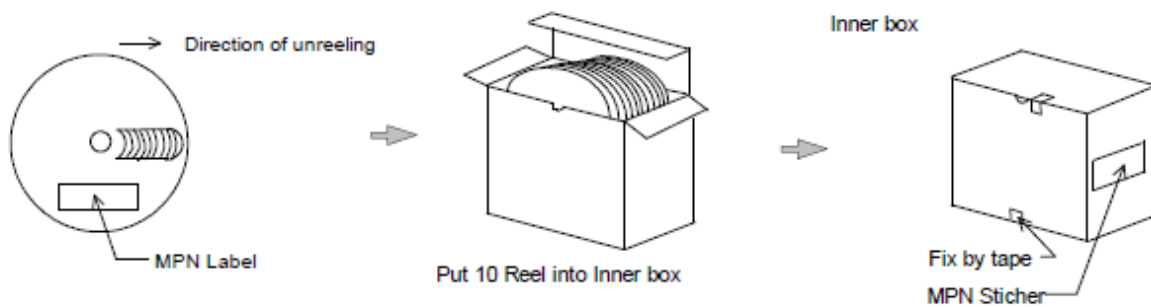
WDFN6(2.0*2.0) 3,000 pcs/reel

| Carrier tape type number | Package code | Maximum number of ICs contained (pcs.) | | Packing form |
|--------------------------|----------------|--|-----------|---|
| | | Reel | Inner box | |
| N16402D001 | WDFN6(2.0*2.0) | 3,000 | 30,000 | Inner box: B50766P001 10 Reels contained Dimensions:mm 190 × 136 × 186 |

MPN Label



Packing Method



ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|--------------|--------------------------|--------------------------|
| LV52204MTTBG | WDFN6 (2x2) (Pb-Free) | 3000 / Tape & Reel |

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