Ordering number : ENA2083

LV8824QA

Bi-CMOS IC

For Brushless Motor Drive
PWM Driver IC

ON Semiconductor®

http://onsemi.com

Overview

The LV8824QA is a PWM pre-driver IC suitable for use in 3-phase brushless motors. This IC was designed based on the assumption that Nch FETs are used as the upper and lower output transistors. The rotational speed is controllable by inputting PWM pulse or DC voltage externally and changing duty. LV8824QA incorporates latch-type constraint protection circuit.

Features

- I_O max = 50mA
- Speed control and synchronous rectification by PWM direct input (3.3V input-ready) and DC voltage.
- 3-Hall FG output
- Latch type constraint protection circuit (latch is released by S/B and F/R.)
- Forward/reverse switch circuit, Hall bias pin
- Power saving circuit
- Current limiter circuit, Low-voltage protection circuit, Thermal shut-down circuit
- Charge pump circuit (external Nch/Nch), 5V regulator output.
- Start/Brake circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max	V_{CC} pin	34	V
	V_G max	V_G pin	42	V
Output current	I_O max		50	mA
Allowable power dissipation	Pd max	Mounted on a circuit board.*1	1.45	W
Junction temperature	Tj max		150	°C
Operating temperature	Topr		-40 to +105	°C
Storage temperature	Tstg		-55 to +150	°C

*1 : Specified circuit board : 100mm × 100mm × 1.6mm, glass epoxy (double-layer board)

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		7.0 to 33	V
5V constant voltage output current	I_{REG}		0 to -10	mA
HB pin output current	I_{HB}		0 to -200	μA
3FG pin applied voltage	V_{3FG}		0 to 6	V
3FG pin output current	I_{3FG}		0 to 10	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$			5.0	6.0	mA
Supply current 2	$I_{CC}2$	Power saving		0.8	0.98	mA
Output block (UH, VH, WH, UL, VL, WL)						
Low-side output ON resistance 1	R_{ON} (L1)	Low level I_O = 10mA		20	30	Ω
Low-side output ON resistance 2	R_{ON} (L2)	High level I_O = -10mA		20	30	Ω
High-side output ON resistance 1	R_{ON} (H1)	Low level I_O = 10mA		25	40	Ω
High-side output ON resistance 2	R_{ON} (H2)	High level I_O = -10mA		65	90	Ω
5V Constant-voltage Output						
Output voltage	VREG	I_O = -5mA	4.8	5.1	5.4	V
Line regulation	ΔV (REG1)	V_{CC} = 7.0 to 33V, I_O = -5mA			50	mV
Load regulation	ΔV (REG2)	I_O = -5m to -10mA			100	mV
Hall Amplifier						
Input bias current	IB (HA)		-2			μA
Common-mode input voltage range 1	VICM1	When using Hall elements	0.3		VREG-1.7	V
Common-mode input voltage range 2	VICM2	At one-side input bias (Hall IC application)	0		VREG	V
Hall input sensitivity	VHIN	SIN wave	80			mVp-p
Hysteresis width	ΔV_{IN} (HA)		9	20	35	mV
Input voltage Low → High	VSLH		3	7.5	15	mV
Input voltage High → Low	VSHL		-19	-11	-5	mV
CSD oscillator circuit						
High level output voltage	V_{OH} (CSD)		2.7	3.0	3.3	V
Low level output voltage	V_{OL} (CSD)		0.9	1.1	1.3	V
Amplitude	V (CSD)		1.6	1.9	2.2	Vp-p
External capacitor charge current	ICHG1 (CSD)	VCHG1 = 2.0V	-14	-11.5	-9	μA
External capacitor discharge current	ICHG2 (CSD)	VCHG2 = 2.0V	9.5	12	14.5	μA
Oscillation frequency	f (CSD)	C = 0.022μF (Design target*)		130		Hz
Charge pump output (VG pin)						
Output voltage	VGOUT		V_{CC}+6.5	V_{CC}+7.0		V
CP1 pin						
Output ON resistance (High level)	V_{OH} (CP1)	ICP1 = -2mA		350	500	Ω
Output ON resistance (Low level)	V_{OL} (CP1)	ICP1 = 2mA		200	280	Ω
Charge pump frequency	f (CP)		82	103	124	kHz
Internal PWM frequency						
Oscillation frequency	f (PWM)		41	51.5	62	kHz
Current limiter operation						
Limiter voltage	VRF		0.18	0.20	0.22	V

* : Design target value and no measurement is made.

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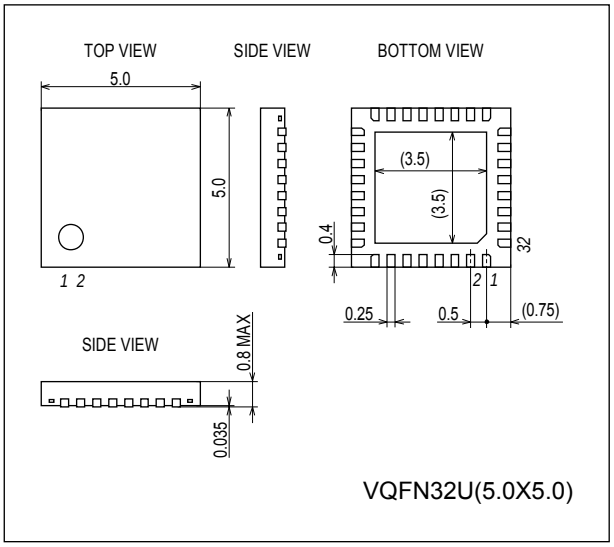
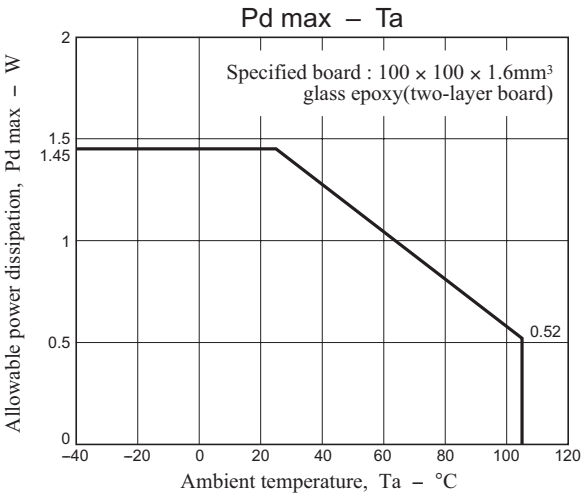
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
PWM oscillator						
Output High level voltage	V_OH(PWM)		2.8	3.05	3.3	V
Output Low level voltage	V_OL(PWM)		0.85	1.0	1.15	V
Amplitude	V(PWM)		1.7	2.0	2.3	Vp-p
External C charge current	I_{CHG}1(PWM)	V_{CHG}1 = 2.0V	-135	-110	-85	μA
External C discharge current	I_{CHG}2(PWM)	V_{CHG}2 = 2.0V	1.4	1.8	2.2	mA
Oscillation frequency	f(PWM)	C = 2200pF (Design target*)		25		kHz
CTL input voltage						
Input voltage 1	V_{CTL}1	Output Duty 100%	2.79	3.1	3.4	V
Input voltage 2	V_{CTL}2	Output Duty 0%	0.84	1.05	1.3	V
Thermal shutdown operation						
Operation temperature	TSD	Design target* (Junction temperature)	150	170		°C
Hysteresis width	ΔTSD	Design target* (Junction temperature)		30		°C
HB pin						
Output voltage	VHB	IHB = -100μA	3.6	3.8	4.0	V
Low-voltage protection (5V constant voltage output detection)						
Operation voltage	VSD		3.95	4.15	4.35	V
Hysteresis width	ΔVSD		0.2	0.3	0.4	V
3FG pin						
Output ON resistance	V_OL (3FG)	I3FG = 5mA		30	45	Ω
Output leakage current	IL (3FG)	V_O = 6V			10	μA
STIME pin						
Input threshold voltage 1	V_I1(TIME)		0		1.0	V
Input threshold voltage 2	V_I2(TIME)		1.5		2.25	V
Input threshold voltage 3	V_I3(TIME)		2.8		3.5	V
Input threshold voltage 4	V_I4(TIME)		4.2		VREG	V
MODE pin						
Input threshold voltage 1	V_I1(MODE)		0		1.0	V
Input threshold voltage 2	V_I2(MODE)		1.5		2.25	V
Input threshold voltage 3	V_I3(MODE)		2.8		3.5	V
Input threshold voltage 4	V_I4(MODE)		4.2		VREG	V
S/B pin						
High level input voltage	V_{IH} (SB)		2.0		VREG	V
Low level input voltage	V_{IL} (SB)		0		1.0	V
Input open voltage	V_{IO} (SB)		VREG-2.2	VREG-2.0	VREG-1.8	V
Hysteresis width	V_{IS} (SB)		0.25	0.33	0.4	V
High level input current	I_{IH} (SB)	V_{SB} = VREG	45	65	85	μA
Low level input current	I_{IL} (SB)	V_{SB} = 0V	-125	-95	-65	μA
PWMIN pin						
Recommended input frequency	f (PWIN)		0.5		60	kHz
High level input voltage	V_{IH} (PWIN)		2.0		VREG	V
Low level input voltage	V_{IL} (PWIN)		0		1.0	V
Input open voltage	V_{IO} (PWIN)		VREG-2.2	VREG-2.0	VREG-1.8	V
Hysteresis width	V_{IS} (PWIN)		0.25	0.33	0.4	V
High level input current	I_{IH} (PWIN)	VPWIN = VREG	45	65	85	μA
Low level input current	I_{IL} (PWIN)	VPWIN = 0V	-125	-95	-65	μA
F/R pin						
High level input voltage	V_{IH} (FR)	*Design target value	2.0		VREG	V
Low level input voltage	V_{IL} (FR)	*Design target value	0		1.0	V
Input open voltage	V_{IO} (FR)		VREG-2.2	VREG-2.0	VREG-1.8	V
Hysteresis width	V_{IS} (FR)	*Design target value	0.25	0.33	0.4	V
High level input current	I_{IH} (FR)	VF/R = VREG	45	65	85	μA
Low level input current	I_{IL} (FR)	VF/R = 0V	-125	-95	-65	μA

Package Dimensions

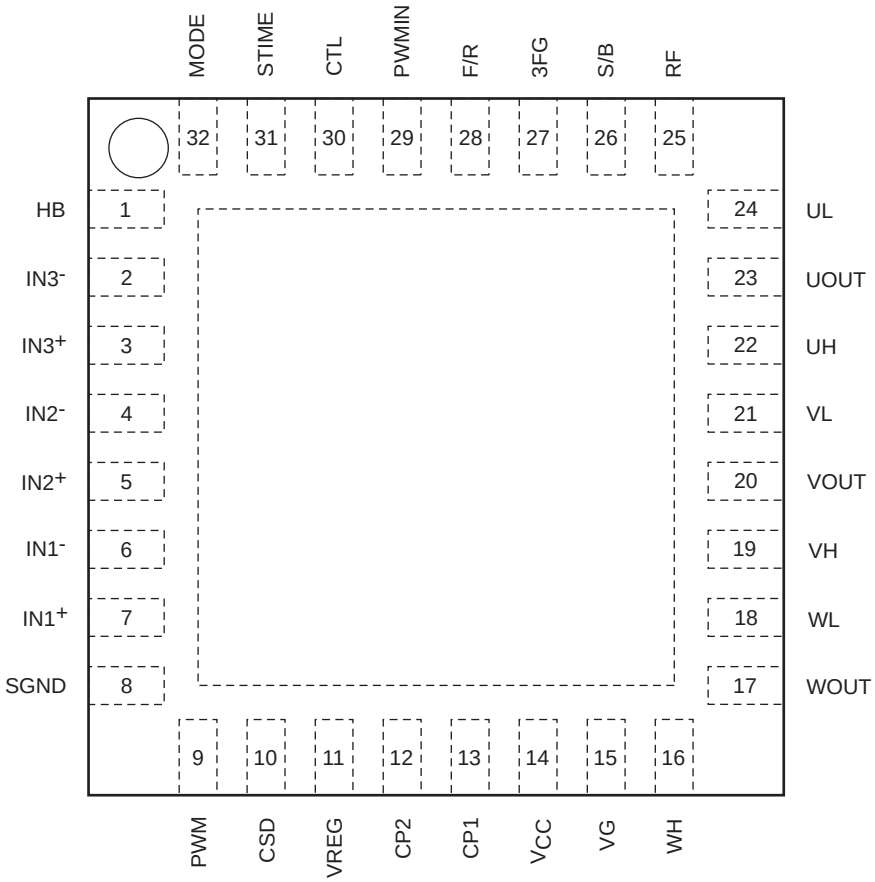
unit : mm (typ)

3436





Pin Assignment



Three-phase HALL logic truth table (IN = “High” means the following state: IN+ > IN-.)

("Upper gate = VH" and "lower gate = UL" mean the following state: the upper FET connected to VH pin is on and the lower FET connected to UL pin operates by PWM signal.)

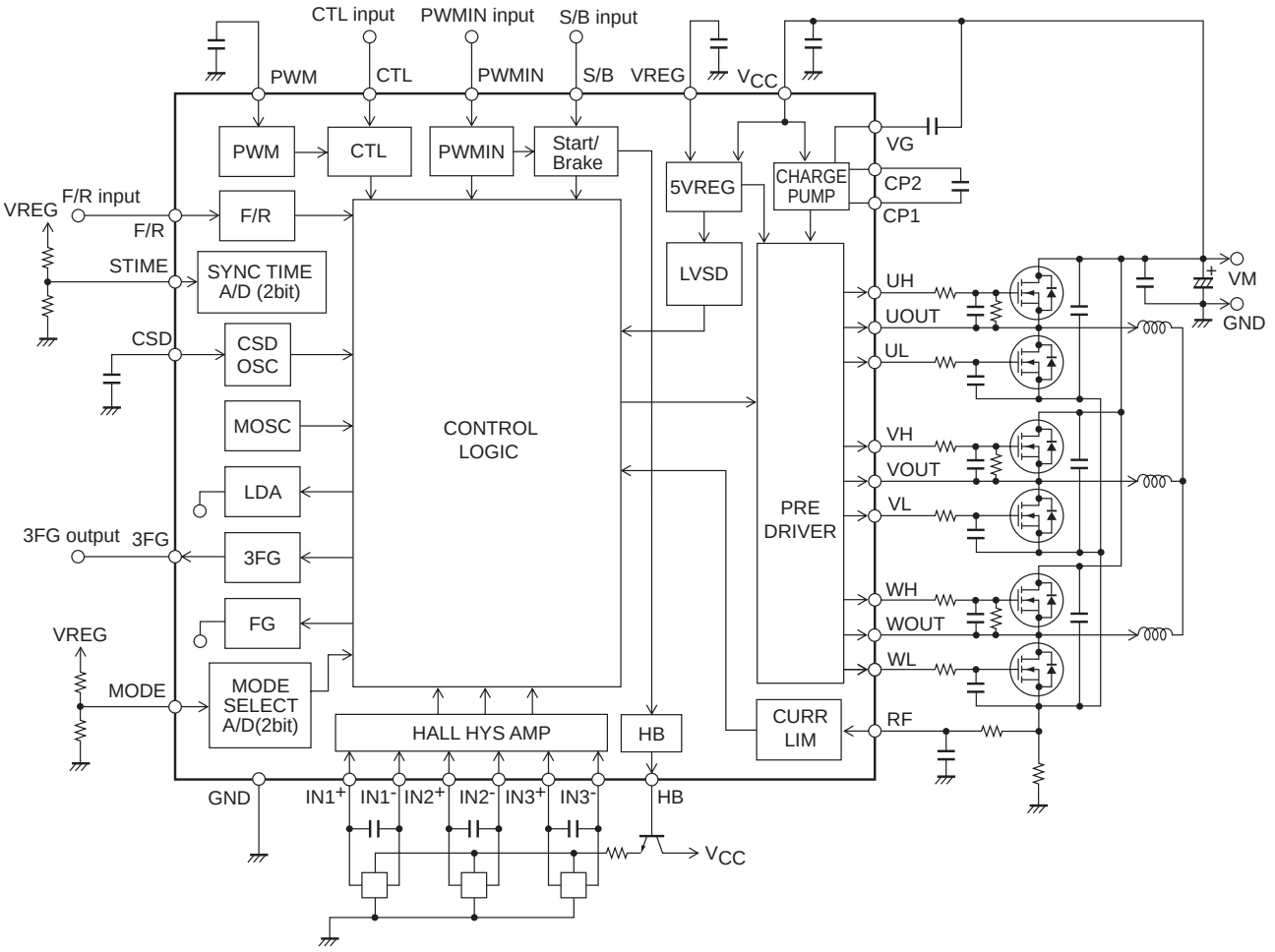
F/R = High			F/R = Low			Driving output	
IN1	IN2	IN3	IN1	IN2	IN3	Upper gate	Lower gate (PWM)
H	L	H	L	H	L	VH	UL
H	L	L	L	H	H	WH	UL
H	H	L	L	L	H	WH	VL
L	H	L	H	L	H	UH	VL
L	H	H	H	L	L	UH	WL
L	L	H	H	H	L	VH	WL

3FG output			
IN1	IN2	IN3	3FG
H	L	H	L
H	L	L	H
H	H	L	L
L	H	L	H
L	H	H	L
L	L	H	H

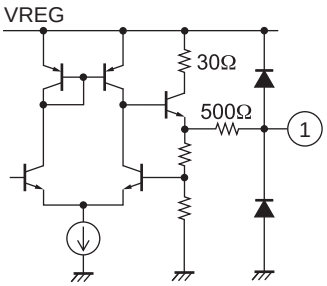
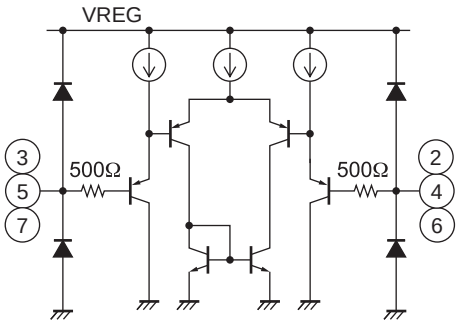
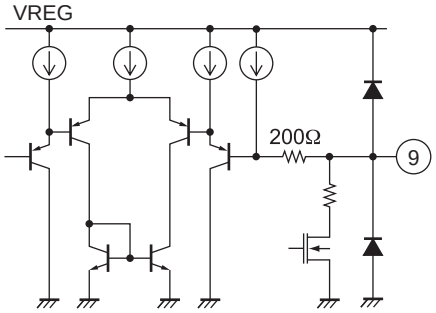
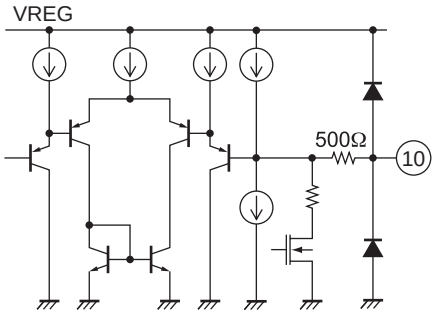
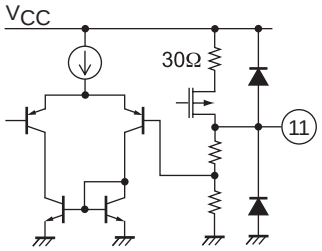
S/B pin, PWMIN pin

Input state	S/B pin	PWMIN pin
High or Open	Stop (short brake)	Output OFF
Low	Start	Output ON

Internal Equivalent Circuit and Sample External Component Circuit



Pin Functions

Pin No.	Pin Name	Pin function	Equivalent Circuit
1	HB	Hall bias pin (3.8Vtyp output). Connect NPN transistor. (See P.11"9.Hall input signal".) During power saving mode, output is turned off (0V). HB pin enable to reduce power consumption of Hall element to 0V during power saving mode.	
2 3 4 5 6 7	$IN3^-$ $IN3^+$ $IN2^-$ $IN2^+$ $IN1^-$ $IN1^+$	Hall input pin. Where $IN^+ > IN^-$, voltage level becomes High. Where $IN^+ < IN^-$, voltage level becomes Low. Desirably, the amplitude of Hall signal is 100mVp-p (differential) or higher. If the noise of Hall signal is an issue, connect a capacitor between IN^+ and IN^-.	
8	SGND	Ground pin for control circuitry.	
9	PWM	Triangular wave oscillation pin for PWM signal generation. Connect a capacitor between this pin and GND. (See P.9 "4. PWM oscillation frequency.")	
10	CSD	Timing setting pin for constraint protection detection as well as setting pin for initial reset pulse. Connect a capacitor between this pin and GND. When protection circuitry is not used, connect a resistor of 220kΩ and capacitor of 4700pF in parallel against GND. (See P.10 "5. Constraint protection circuit")	
11	VREG	5V regulator output pin (power supply for control circuitry). Desirably, connect a capacitor of 0.1μF between this pin and GND for stabilization. (See P.10 "8. VREG stabilization" and P.12 "15. Low voltage protection circuit")	

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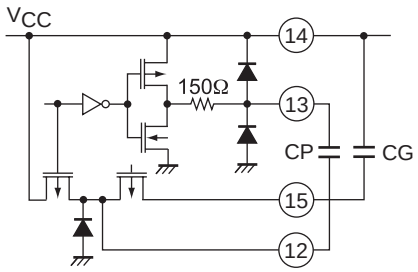
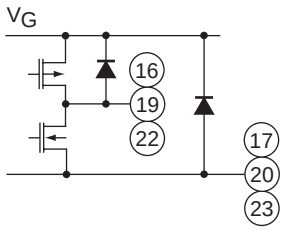
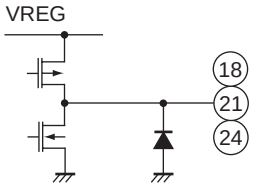
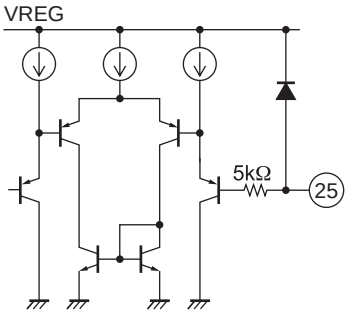
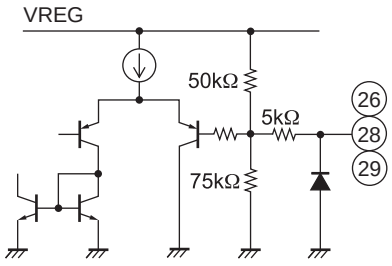
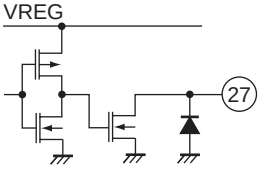
Pin No.	Pin Name	Pin function	Equivalent Circuit
12 13	CP2 CP1	Capacitor connect pin for charge pump. Connect a capacitor between CP1 and CP2.	
14	V_{CC}	Supply pin for control. Connect a capacitor between this pin and GND to reject noise. (See P.12 “14. Supply stabilization”)	
15	VG	Charge pump output pin. (Power supply for upper FET gate.) Connect a capacitor between this pin and V_{CC}. (See P.10 “7. Charge pump circuit”)	
16 19 22	WH VH UH	High side output pin. (Output pin for gate driver of upper side Nch power FET.) (See P.9 “1. Output driving circuit.”)	
17 20 23	WOUT VOUT UOUT	Voltage detection pin. (Source voltage detection pin of upper side Nch power FET.”) (See P.9 “1. Output driving circuit.”)	
18 21 24	WL VL UL	Low side output pin. (Output pin for gate driver of lower side Nch power FET.)	
25	RF	Output current detection pin. Connect a detection resistor (R_F) between this pin and GND. Current limit value is obtained as follow: I = VRF / R_F (VREF = 0.2Vtyp). (See P.9 “2. Current limiter circuit”)	
26	S/B	Start/Brake selector pin. “High or OPEN”: Short brake. “Low”: Start (See P.12 “13. Power saving circuit”)	
28	F/R	Selects forward/reverse rotation. Voltage level becomes High when this pin is open.	
29	PWMIN	PWM direct input pin. Output is controllable by the duty of the input pulse. When using PWMIN pin, make sure that CTL pin is set to High level voltage. (See P.9 “3. Speed control method”)	
27	3FG	3 Hall FG signal output pin. Open drain output.	

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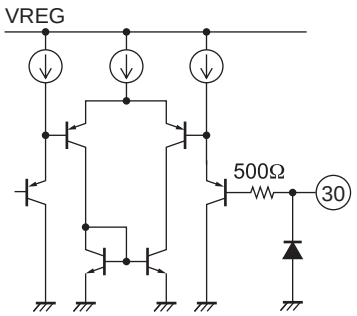
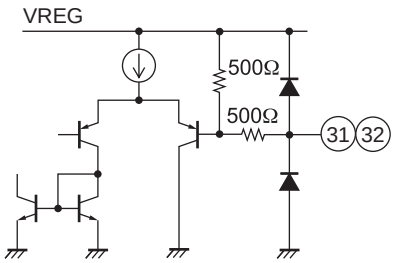
Pin No.	Pin Name	Pin function	Equivalent Circuit
30	CTL	Control input pin. Output On-duty is controllable using the comparison result of CTL pin voltage and PWM oscillation waveform. To use CTL pin, set PWMIN pin to Low level voltage. (See P.9 “3. Speed control method”)	
31	STIME	Dead-time setting pin for synchronous rectification. Depends on input voltage to STIME pin, 4 types of mode are selectable. (See P.10 “6. How to set STIME”)	
32	MODE	Operation MODE setting pin. Depends on input voltage to MODE pin, 4 types of mode are selectable. (See P.11 “10. MODE pin”)	

Overview of LV8824QA

1. Output driving circuit

LV8824QA is designed to use Nch FETs for upper and lower output. It adopts direct PWM driving method to reduce the power loss during output. You can adjust motor torque by changing the duty cycle of the output of lower FET. Make sure to connect capacitor at the proximity of each 3-phase output FET to prevent high frequency oscillation caused by leading pattern layout around the board (approx. 0.1μF between Supply and RF).

If the ON speed of FET is too fast, penetration current may flow. In this case, insert serial resistors to a gate to control speed. On the other hand, if excessively high resistor is inserted to the gate, the waveform of the gate can be distorted and when the duty cycle of PWM is low, gate voltage becomes insufficient and lower side FET may be damaged or destroyed by heat generation.

Or even without resistance, the same phenomenon as what happens with high gate capacitor for FET could occur. In this case, make sure to take ASO of the switching element into consideration and limit the usage lowest duty. Depends on types of FET, penetration current may flow when the duty cycle of PWM is low. As a countermeasure, you can insert capacitor between the gate and the source of the upper FET. However, caution is required since excessively high capacitor value slows down the speed of switching which may cause heat generation in the upper FET.

2. Current Limiter Circuit

The peak current of current limiter circuit is limited by the current determined as follows. $I = VRF/R_F$ (V_{RF} = 0.2V (typical), R_F: current detection resistance). Current is limited as the duty cycle of output of UL, VL and WL lowers. The operation of current limiter circuit is delayed approximately for 1.5μs to avoid operation error of current limiter when it mistakenly detects reverse current of diode driven by PWM. However, if the coil resistance or inductance of motor is too small, such delay may operate current limiter at higher current than the setting value because the current charge when starting up motor rotation is too fast (without back EMF of the motor). Hence, make sure to set current limiter value taking such increase of current caused by delay into consideration.

If noise leads to error operation, make sure to insert a filter.

*PWM frequency of current limiter circuit.

The PWM frequency of current limiter circuit is determined by the internal reference oscillator which is approx 50kHz .

3. Speed control method

The speed control input of LV8824 supports digital and analog input.

(1) Digital input

You can control output by the duty obtained as a result of inputting pulse to PWMIN pin.

PWMIN pin:

Low level input voltage → PWM side (lower side) output ON

High level input voltage → PWM side (lower side) output OFF

If you need to perform input with logic inversion, add external Tr (NPN).

If the input of PWMIN pin is at High level for a certain period (approx. 2.5ms), it is judged to be Duty = 0%. When power saving mode is selected, HB pin output is set to Low level.

*To use PWMIN pin, make sure to set CTL input to High level voltage.

(2) Analog input

Based on the comparison between CTL pin voltage and PWM oscillation waveform, you can control the duty cycle of output. By adjusting the CTL pin voltage approximately between 1V and 3V, on time of duty cycle is controllable from 0% to 100%.

When CTL pin voltage < 1.05V (typ) is observed for approximately 2.5ms, the duty is judged to be 0%. If power saving mode is selected, HB pin output turns Low level.

*To use CTL pin, make sure to set PWMIN input to Low level voltage.

4. PWM oscillation frequency

PWM oscillation frequency is configurable by the capacitance (C_{PWM}) connected to PWM pin.

$$\text{PWM oscillation frequency (kHz)} \approx 48 - 10.2 * C_{PWM}\ \text{(nF)}$$

When the capacitor of 2.2nF is connected, PWD oscillation frequency is approximately 25kHz.

5. Constraint protection circuit

LV8824 includes a constraint protection circuit to protect the IC and the motor that are under motor constraint mode. This circuit operates when the motor is under operation and the Hall signal does not switch over a certain period of time. Note that while this constraint protection circuit is under operation, lower side output transistor is off. Also during power saving mode, HB pin output is off.

(See P.15 “10. MODE pin” and P.16 “12. HB pin” for further details.)

Time is set by the value of capacitor connected the CSD pin.

Set time (s) ≈ 90 × C (μF)

When the capacitor of 0.022μF is connected, the protection time becomes approximately 2.0 seconds. The set time should allow margin taking motor startup time into consideration.

Conditions for releasing constraint protection state	Conditions for restarting motor rotation
S/B pin: H input (during power saving mode*1)	S/B pin: L input *2
S/B pin: H input (during FG output mode *1)	S/B pin: L input
F/R pin: input H/L switch	(immediately after releasing constraint protection)
After Duty = 0% is detected from PWM input and Duty Up is detected.	(immediately after releasing constraint protection)
Low voltage protection circuit is in operation.	After the recovery from low voltage state *2

*1 See P.15”10. MODE pin”

*2 Since this is an initial reset state, after satisfying the conditions for restarting motor operation where CSD pin voltage reaches to the defined voltage level, the motor starts up once again. The time for restart is approximately 1.0ms if the capacitor of 0.022μF is connected to CSD pin.

If thermal shutdown is running under the constraint protection, even after the temperature decreases, the constraint protection state continues.

CSD pin also functions as initial reset generation pin. If it is connected to GND, the logic circuit will go into a reset state and speed control cannot be performed. Therefore, when you do not use constraint protection, connect a resistor of approximately 220kΩ and a capacitor of approximately 4700pF in parallel to GND.

6. How to set STIME

STIME pin sets Dead-time for synchronous rectification.
This IC has the time for preventing “shoot-through current” when it makes synchronous rectification.
4 types of dead-time are configurable according to the input voltage to STIME pin.

STIME pin input voltage	Dead-time
● 0V to 1.0V	→ approx. 2.0μs
● 1.5V to 2.25V	→ approx. 1.5μs
● 2.8V to 3.5V	→ approx. 1.0μs
● 4.2V to (VREG)V	→ approx. 0.5μs

7. Charge pump Circuit

Charge pump circuit boosts the voltage to generate gate voltage in the upper-side output FET. The capacitor CP connected between CP1 pin and CP2 boosts the voltage which is stored in the capacitor CG between VG pin and V_{CC} pin. The relation of CP and CG capacitance should be as follows:

CG ≥ 4 × CP

The charge and discharge to CP capacitor is performed in the cycle of 100kHz. The greater the CP capacitor is, the higher the current capability of VG supply become. However, if the capacitance is too large, the charge and discharge operation becomes insufficient. Likewise, the larger the CG capacitor is, the more stable VG voltage becomes. However, if the capacitance is too large, generation time of VG voltage becomes longer at power supply. Hence, caution is required for setting capacitance.

The desirable capacitances of CP and CG are follows.

CP = 0.1μF
CG = 0.47μF

8. VREG Stabilization

Make sure to connect capacitor of 0.1μF higher to stabilize VREG voltage which is used as supply voltage to control circuit. In the layout, GND of the capacitor should be as close as possible to the GND pin of the IC.

9. Hall Input Signal

The amplitude of Hall input should be higher than the hysteresis width (35mV max).
The amplitude should be 100mVp-p or higher to take the influence of noise and phase gap into consideration. If output wave form is distorted by noise when switching from one phase to another, make sure to insert capacitor between hall inputs. In constraint protection circuit, Hall input is used as judgment signal. Although the circuit ignores noise to a certain level, caution is still required. If all 3 phases of Hall input signal turn to the same input state (HHH or LLL), all of the outputs are turned off. If you use Hall IC, by fixing one input side (either + or -) to the voltage within the range of common-mode input (0.3V to VREG-1.7V), the other input side accepts input from 0V to VREG.

Connection of Hall elements

Connection (1) (where three Hall elements in serial connection)

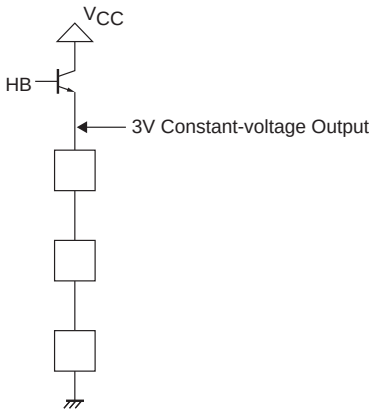
Merit

- Compared to parallel connection, current consumption is less because serial connection enables sharing current among 3 Hall elements.
- Current limiter resistance is reducible.
- Amplitude variation caused by temperature is less.

Demerit

- Amplitude may not be sufficient because each Hall element is powered with 1V only.
- Current may fluctuate depends on temperature.
- HALL amplitude tends to be affected by the fluctuation of Hall elements (especially for input resistor).

(1)



Connection (2) (three Hall elements in parallel connection)

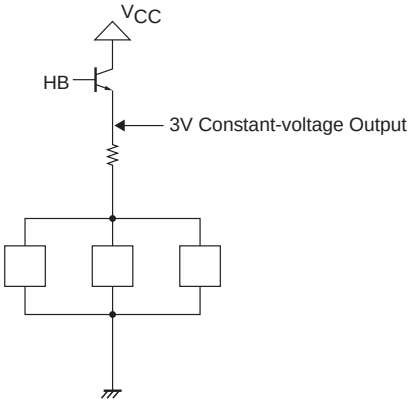
Merit

- The current for Hall elements is adjustable with current limiter resistance.
- Amplitude is sufficient because supply voltage to Hall elements is adjustable.

Demerit

- Current consumption is large because each Hall element requires current independently.
- Requires resistor for current limiter.
- Amplitude may fluctuate depends on temperature.

(2)



10. MODE pin

MODE pin allows selecting functions of the IC.
MODE pin sets 4 functions based on input voltage.

MODE pin input voltage	mode
● 0V to 1.0V	→ mode B & power saving mode
● 1.5V to 2.25V	→ mode B & FG output mode
● 2.8V to 3.5V	→ mode A & FG output mode
● 4.2V to (VREG)V	→ mode A & power saving mode

	mode A (suitable for fan)	mode B (suitable for office equipments)
When Duty cycle = 0% is detected	Synchronous rectifier OFF (free operation)	Short brake
When frequency of PWM input is low (approx. 7.5kHz or lower)	Synchronous rectifier OFF	Synchronous rectifier ON
When the Duty cycle of PWM input is low (ex. Frequency: 20kHz, Duty cycle: 3% or lower)	Synchronous rectifier OFF	Synchronous rectifier ON
Reverse current detection function	Yes (during detection, synchronous rectifier is OFF)	No

Power saving mode: When S/B pin = Brake, power saving mode is set. When Duty = 0% is detected as well as when constraint protection circuit is in operation, HB pin output is turned OFF.
(See “12. HB pin” and “13. Power saving circuit” for further details.)

DG output is always feasible since FG output mode: Power saving mode and HB pin output OFF are not set.

11. How to see STIME pin and MODE pin

The input voltage of STIME pin and MODE pin are configurable by the following methods.

- 0V to 1.0V → short-circuit the pins to GND
- 1.5V to 2.25V → connect the resistors of 33kΩ and 22kΩ between VREG and GND in series.
- 2.8V to 3.5V →connect the resistors of 33kΩ and 22kΩ between VREG and GND in series.
- 4.2V to (VREG)V → Leave the pins open or short-circuit VREG.

12. HB pin *When power saving mode is selected.

HB pin is used to reduce current to Hall elements during standby mode (for power saving).
After the motor operation is stopped, HB pin output is turned off in the following states:

- When S/B is in brake mode.
- When duties of the input of PWMIN and CTL pin voltage are 0%.
- When constraint protection circuit is under operation.

13. Power Saving Circuit (Start/Brake circuit) *When power saving mode is selected.

In brake state, after the motor is stopped, majority of the circuits are stopped to reduce current consumption. By using HB pin, current consumption during power saving is less than 1mA. Also, the output is fixed to short-brake state (lower-side is shorted). Even in the power saving state, 5V regulator voltage is output.

14. Supply Stabilization

The supply line of LV8824 is unstable because it adopts switching driving method. Hence, you need to connect sufficient capacitor between V_{CC} and GND to stabilize power supply (electrolysis capacitor). If such capacitor (electrolytic capacitor) cannot be connected at the proximity of the pin, make sure to insert a ceramic capacitor of approx. 0.1μF by the pin.
If you insert diode to supply line to prevent reverse connection, make sure to select a larger capacitor.

15. Low voltage protection circuit

This IC incorporates comparator which uses band gap voltage as reference. Where S/B pin is at Low voltage level, VREG pin voltage (5V) is monitored and when this voltage decreases to 4.15V or lower (typ), protection circuit operates.
In this case, output transistor of each phase is fixed to the following states according to the input voltage of MODE pin and S/B pin.

MODE pin input voltage	S/B pin input voltage	Source side	Sink side
0V to 2.25V	L/H	All OFF	All ON
2.8V to (VREG)V	H	All OFF	All ON
	L	All OFF	All OFF

16. Thermal shutdown Circuit

When the junction temperature of the IC exceeds 170°C (design target), thermal shutdown circuit operates and all the output transistors are turned off.
When the temperature decreases by 30°C (design target), each output transistor returns to operation state. However, the thermal shutdown operates when a junction temperature exceeds the ratings and this does not protect an application against breakdown.

17. Exposed die pad

The exposed die pad should be GND or open.

18. Cautions for usage

This IC operates at synchronous rectification for high efficiency.
The synchronous rectification is effective for reducing heat generation and improving efficiency because it reduces the loss of output transistor.
However, synchronous rectification may increase supply voltage depends on usage conditions.

- If output duty decreases drastically.
- If PWM input frequency is low, etc.

To prevent the voltage to exceed the maximum ratings as a result of increased supply voltage, following measures are highly recommended.

- Select an optimum capacitor between power supply and GND.
- Insert a Zener diode between power supply and GND.

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