



2SC4482

Bipolar Transistor 20V, 5A, Low $V_{CE(sat)}$, NPN Single NMP

ON Semiconductor®

<http://onsemi.com>

Features

- Low saturation voltage
- Large current capacity
- High-speed switching

Specifications

Absolute Maximum Ratings at $T_a=25^\circ\text{C}$

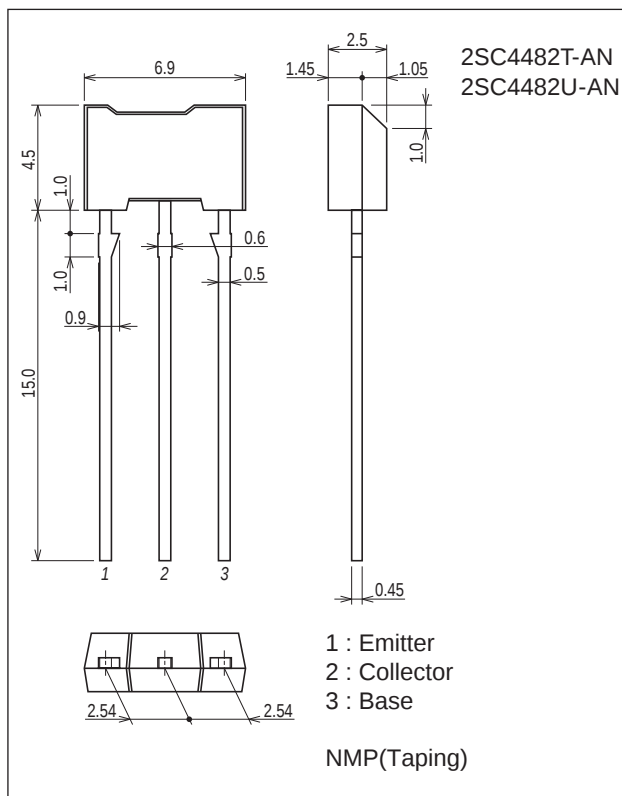
Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		60	V
Collector-to-Emitter Voltage	V_{CEO}		20	V
Emitter-to-Base Voltage	V_{EBO}		6	V
Collector Current	I_C		5	A
Collector Current (Pulse)	I_{CP}		8	A
Collector Dissipation	P_C		1	W
Junction Temperature	T_j		150	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

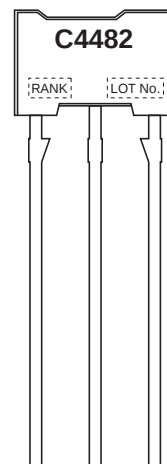
7540-001



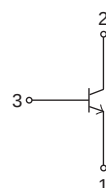
Product & Package Information

- Package : NMP(Taping)
- JEITA, JEDEC : SC-71
- Minimum Packing Quantity : 2,500 pcs./box

Marking(NMP(Taping))



Electrical Connection



Electrical Characteristics at Ta=25°C

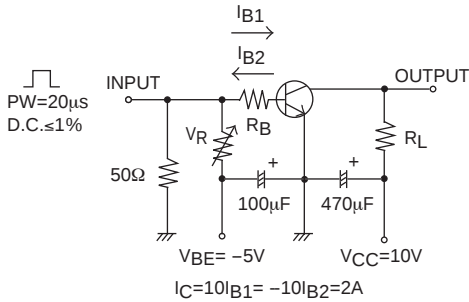
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	$V_{CB}=50V, I_E=0A$			100	nA
Emitter Cutoff Current	I_{EBO}	$V_{EB}=5V, I_C=0A$			100	nA
DC Current Gain	h_{FE1}	$V_{CE}=2V, I_C=500mA$	200*		560*	
	h_{FE2}	$V_{CE}=2V, I_C=3A$	95			
Gain-Bandwidth Product	f_T	$V_{CE}=10V, I_C=50mA$		150		MHz
Output Capacitance	C_{ob}	$V_{CB}=10V, f=1MHz$		45		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=3A, I_B=60mA$		220	500	mV
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C=3A, I_B=60mA$			1.5	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=10\mu A, I_E=0A$	60			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=1mA, R_{BE}=\infty$	20			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E=10\mu A, I_C=0A$	6			V
Turn-ON Time	t_{on}	See specified Test Circuit.		30		ns
Storage Time	t_{stg}			300		ns
Fall Time	t_f			40		ns

* : The 2SC4482 is classified by 500mA h_{FE} as follows :

Rank	T	U
h_{FE}	200 to 400	280 to 560

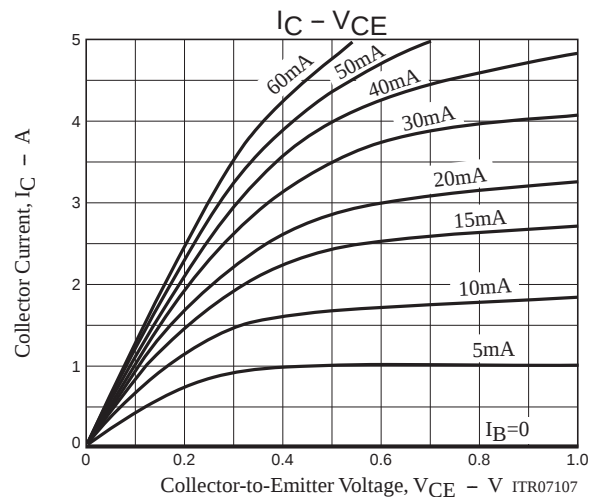
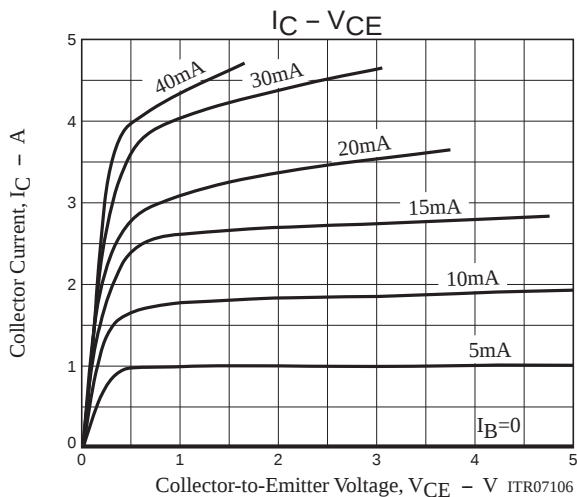
Switching Time Test Circuit

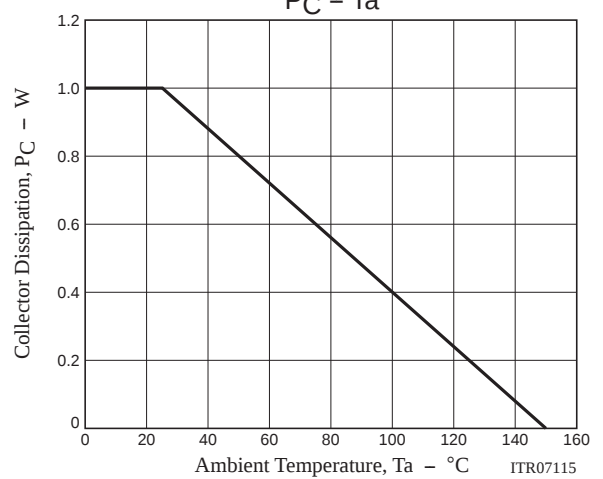
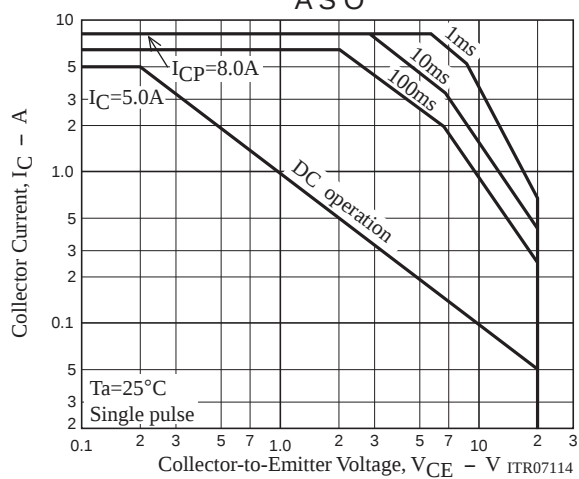
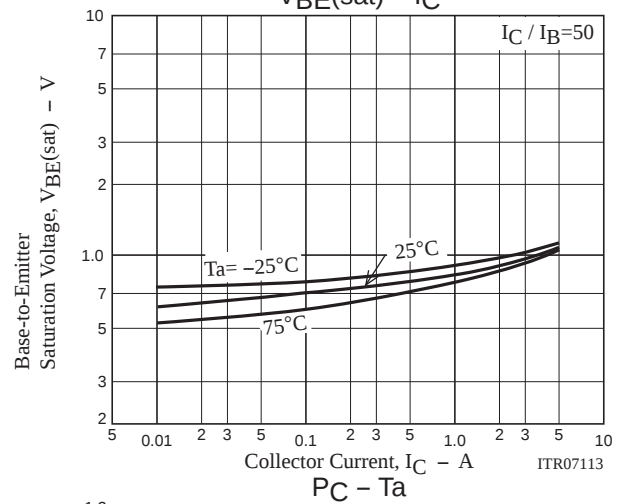
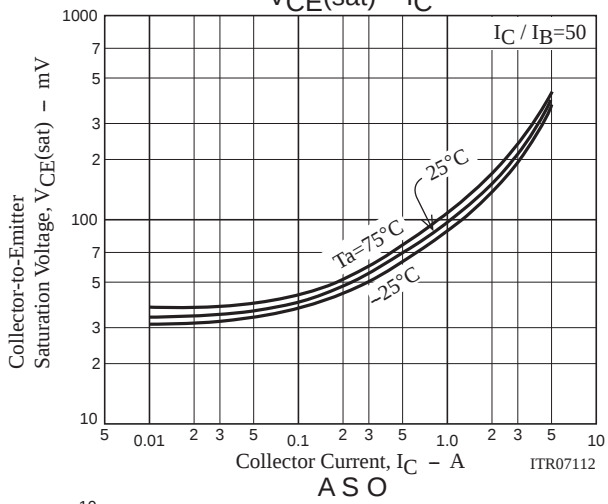
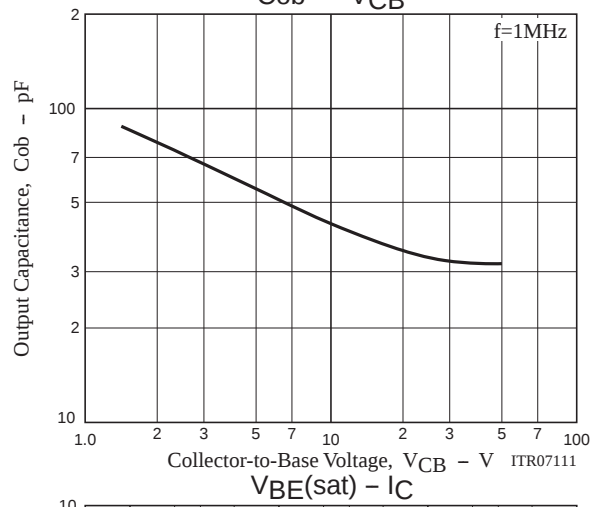
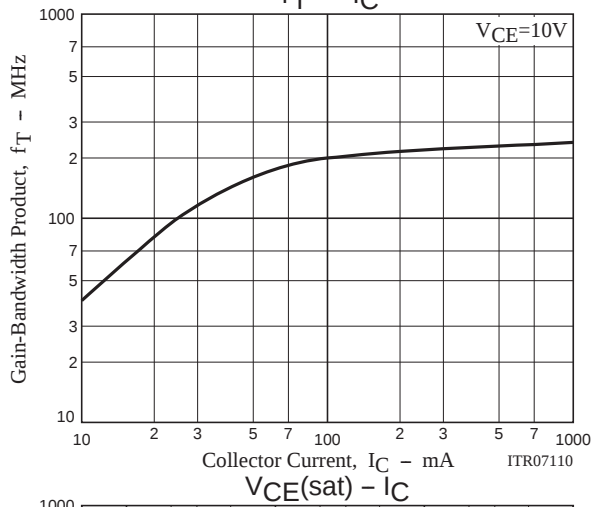
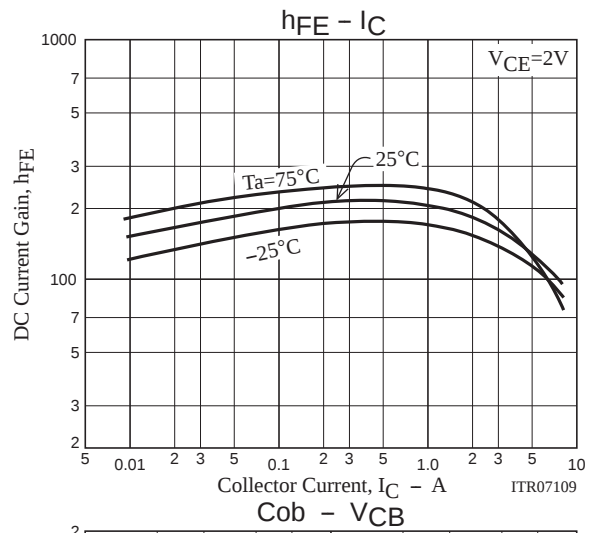
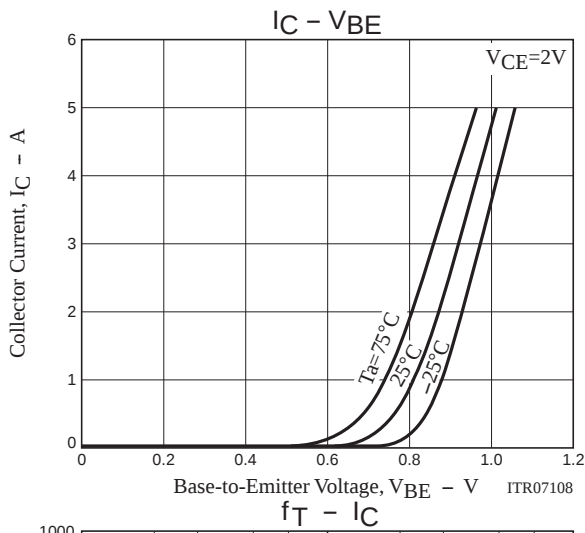
2SC4482



Ordering Information

Device	Package	Shipping	memo
2SC4482T-AN	NMP(Taping)	2,500pcs./box	Pb Free
2SC4482U-AN	NMP(Taping)	2,500pcs./box	





Bag Packing Specification

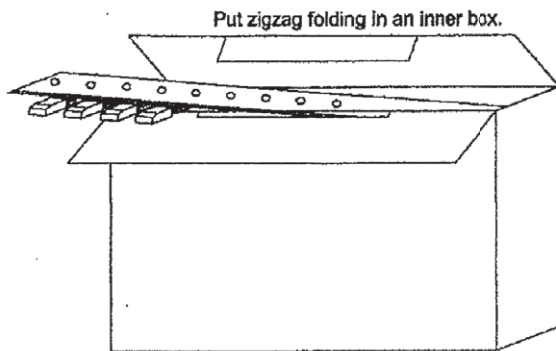
2SC4482T-AN, 2SC4482U-AN

NMP (Zigzag folding)

Storage package Outline name	Package type	Maximum Number of devices contained (pcs.)		Packing format	
		Inner box No.	Storage quantity	Outer box (C-6)	Outer box (C-8)
NMP	AN/AZ	C-3 Inner box Dimensions :mm(external) 330×45×125	2,500	8 inner boxes contained(20,000pcs.) Outer box Dimensions:mm(external) 585×345×195	4 inner boxes contained(10,000pcs.) Outer box Dimensions:mm(external) 345×300×195

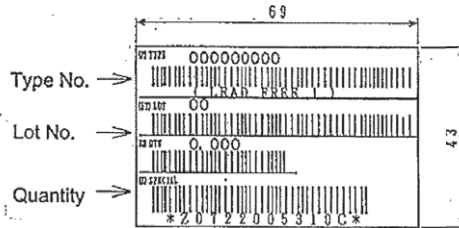
1. Packing format

Packing method



2. Bar code label

(Unit : mm)

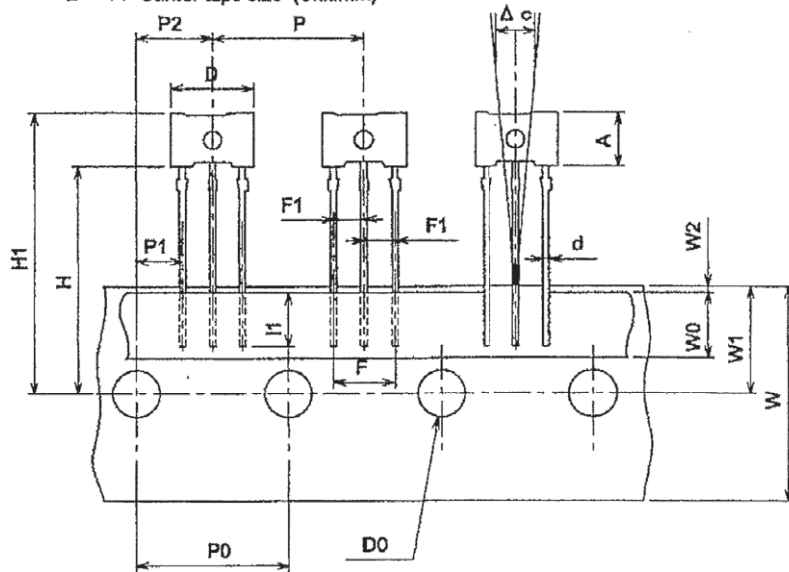


*LEAD FREE 1:

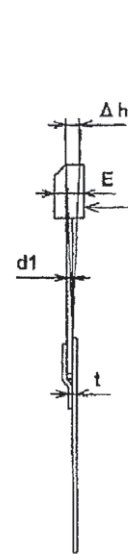
Lead-free External terminal surface treatment product.

2. Taping specifications

2-1. Carrier tape size (Unit:mm)



Marking surface



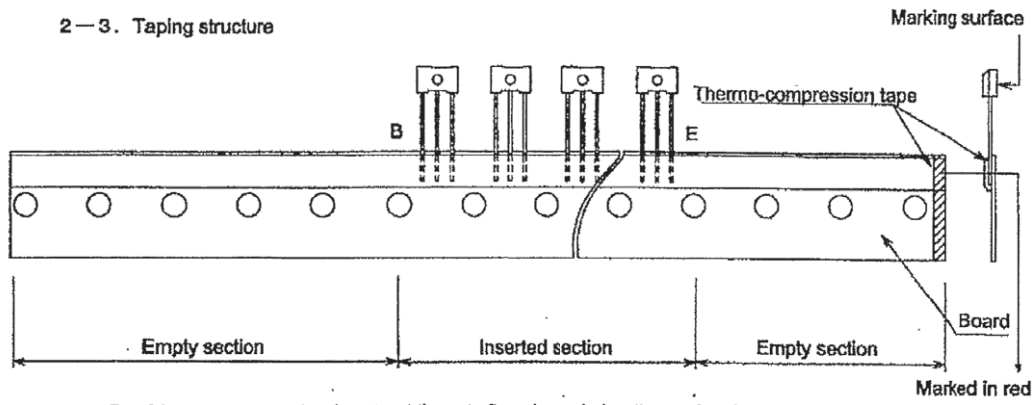
2-2. Taping size standard

Item	Symbol	Standard	Tolerance
Work piece outside diameter	D	6.9	±0.2
	E	2.5	±0.2
Work piece height	A	4.5	±0.2
Lead wire diameter	d	0.5	±0.1
Lead wire thickness	d1	0.45	±0.1
Bonded lead wire	I1	3.0MIN	
Pitch between products	P	12.7	±0.5
Pitch between perforations	P0	12.7	±0.2
Total pitch for 21 perforations	P0×20	254.0	±1.0
Distance between lead wire	F	5.0	+0.8 -0.2
Lead wire pitch distance	F1	2.54	+0.4 -0.1
Displacement of perforations	P1	3.81	±0.3
	P2	6.35	±0.3
Displacement of tape	W2	0~0.5	

Unit:mm

Item	Symbol	Standard	Tolerance
Tape width	W	18.0	±0.5
Adhesive tape	W0	6.0	±0.5
Displacement of perforations	W1	9.0	±0.5
Work piece bottom surface position	H	19.0	+1.0 -0.5
Work piece upper limit position	H1	23.5	±1.0
Perforations diameter	D0	φ4.0	±0.2
Tape thickness (total thickness)	t	0.6	±0.2
Product inclination	Δc	0	±0.7
Product inclination	Δh	0	±1.0

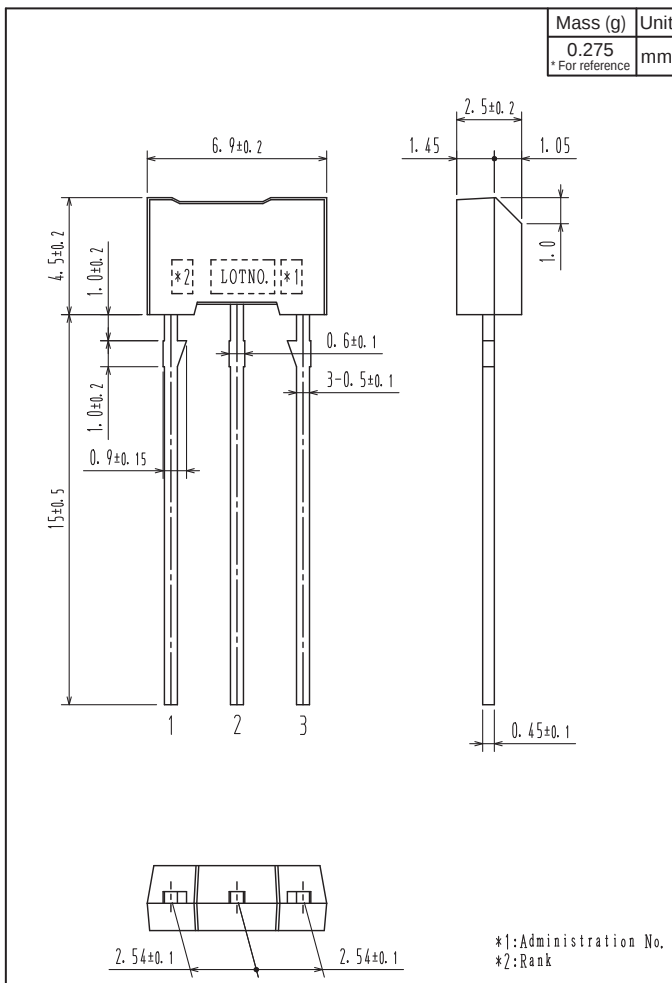
2—3. Taping structure



- Provide an empty section for about three to five pieces in leading and end portions of the tape.
- Provide an empty section in the fold-back portion.
- Provide marking in red to the E-side end of the board.

Outline Drawing

2SC4482T-AN, 2SC4482U-AN



ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[2SC4482T-AN](#) [2SC4482U-AN](#)