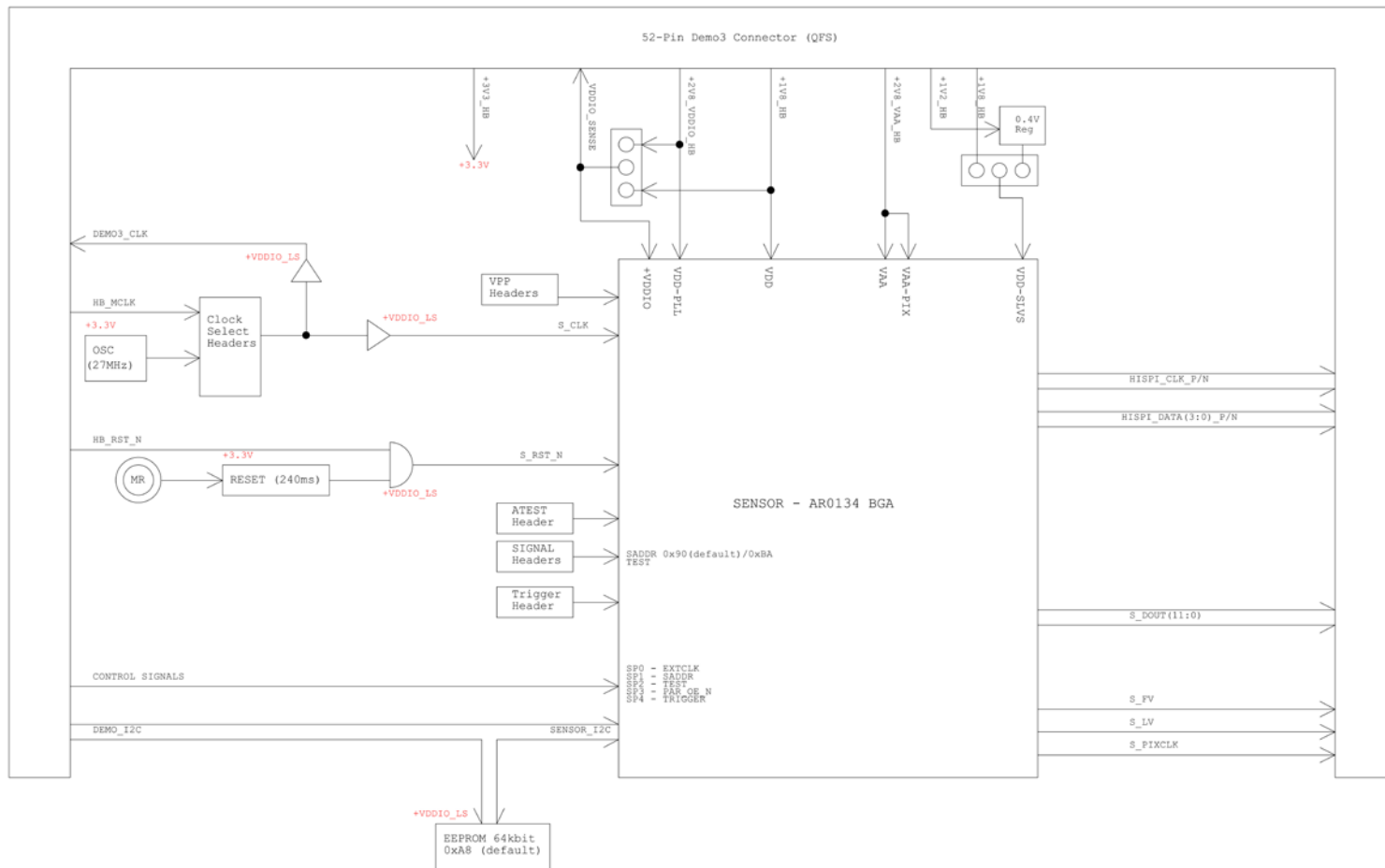


Schematic for the AR0134CSSC00SUEAH3-GEVB Evaluation Board

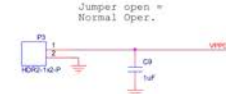
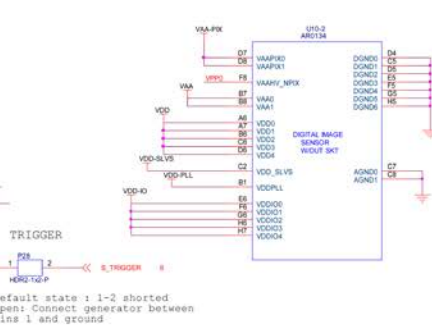
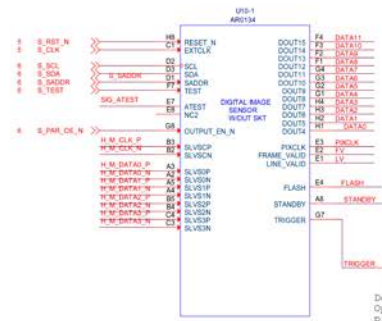
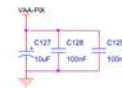
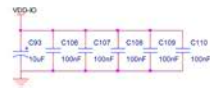
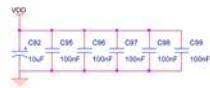
Block Diagram



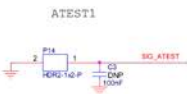
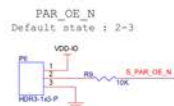
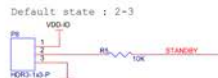
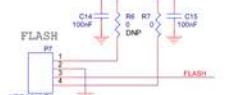
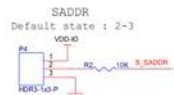
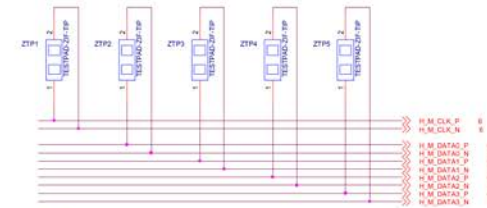


Sensor

VDD	4	VDD	4
VDDQ	4	VDDQ	4
VDDQ_L1	4	VDDQ_L1	4
VDDQ_L2	4	VDDQ_L2	4
VDDQ_L3	4	VDDQ_L3	4
VDDQ_L4	4	VDDQ_L4	4
VDDQ_L5	4	VDDQ_L5	4
VDDQ_L6	4	VDDQ_L6	4
VDDQ_L7	4	VDDQ_L7	4
VDDQ_L8	4	VDDQ_L8	4
VDDQ_L9	4	VDDQ_L9	4
VDDQ_L10	4	VDDQ_L10	4
VDDQ_L11	4	VDDQ_L11	4
VDDQ_L12	4	VDDQ_L12	4
VDDQ_L13	4	VDDQ_L13	4
VDDQ_L14	4	VDDQ_L14	4
VDDQ_L15	4	VDDQ_L15	4
VDDQ_L16	4	VDDQ_L16	4
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VDDQ_L91	4	VDDQ_L91	4
VDDQ_L92	4	VDDQ_L92	4
VDDQ_L93	4	VDDQ_L93	4
VDDQ_L94	4	VDDQ_L94	4
VDDQ_L95	4	VDDQ_L95	4
VDDQ_L96	4	VDDQ_L96	4
VDDQ_L97	4	VDDQ_L97	4
VDDQ_L98	4	VDDQ_L98	4
VDDQ_L99	4	VDDQ_L99	4
VDDQ_L100	4	VDDQ_L100	4

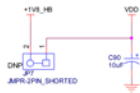


(Note for layout: - Place these testpads near the Demo3 I/F connector at the top side of PCB)

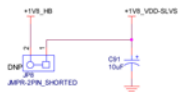


Debug Headers: Cut away the shorted trace and mount header for power debugging

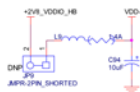
VDD 1.8V SUPPLY



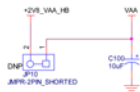
VDD-SLVS 1.8V SUPPLY



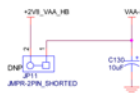
VDD-PLL 2.8V SUPPLY



VAA 2.8V SUPPLY

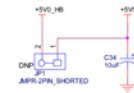


VAA-PIX 2.8V SUPPLY



Power

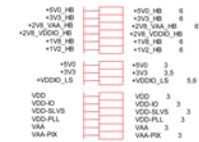
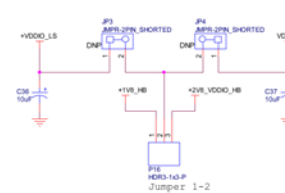
PERIPHERAL 5V SUPPLY



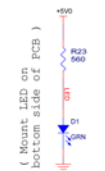
PERIPHERAL 3.3V SUPPLY



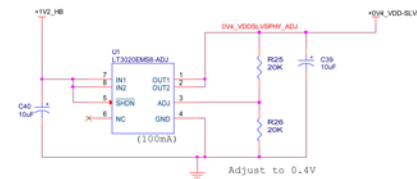
VDDIO & VDDIO LS 1.8V/2.8V SUPPLY



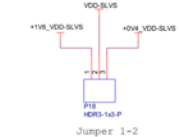
5V LED



VDDSLVSPHY 0.4V SUPPLY



Selection of 0.4V or 1.2V/1V8 for VDDSLVSPHY supply

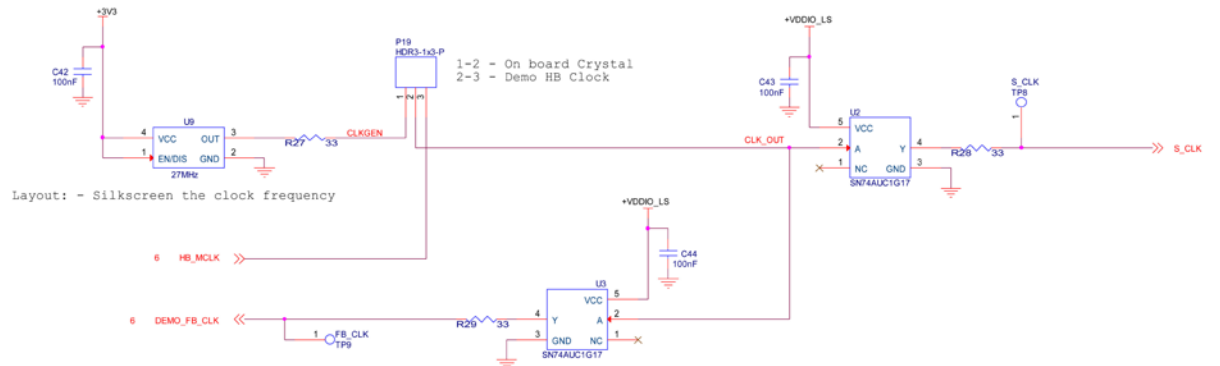




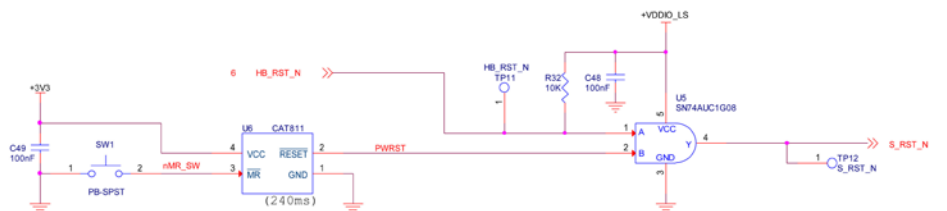
Clock and Reset

+5V0 3.4
+3V3 3.4
+VDDIO_LS 4.6

CLOCK CIRCUIT



RESET CIRCUIT



+5V0_HB		+5V0_HB	4
+3V3_HB		+3V3_HB	4
+2V8_VAA_HB		+2V8_VAA_HB	4
+2V8_VDDIO_HB		+2V8_VDDIO_HB	4
+1V8_HB		+1V8_HB	4
+1V2_HB		+1V2_HB	4
+3V3		+3V3	3.4.5
+VDDIO_LS		+VDDIO_LS	4.5

[illegible]

Diagram illustrating the HD96-20-P connector pin configuration. The diagram shows two rows of pins. The top row (pins 1-4) is connected to +VDD0_1.5 and includes capacitors C03 (100nF) and C04 (100nF). The bottom row (pins 5-8) is connected to DEMO_SDA and DEMO_SCL. The HD96-20-P connector is shown with pins 1-2 and 3-4 labeled as "Jumper: 1-2 & 3-4 (default status)".

EEPROM Address Switch Settings:

A2 = HIGH, A1 = LOW, A0 = LOW; Address =>	0xA8 (default)
A2 = HIGH, A1 = HIGH, A0 = LOW; Address =>	0xAC
A2 = LOW, A1 = HIGH, A0 = LOW; Address =>	0xA4
A2 = LOW, A1 = LOW, A0 = LOW; Address =>	0xAA

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