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FAIRCHILD SEMICONDUCTOR®

May 2007

74VHC161
4-Bit Binary Counter with Asynchronous Clear

Features

- High Speed: f_{MAX} = 185MHz (Typ.) at T_A = 25°C
- Synchronous counting and loading
- High-speed synchronous expansion
- Low power dissipation: I_{CC} = 4µA (Max.) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power down protection provided on all inputs
- Low noise: V_{OLP} = 0.8V (Max.)
- Pin and function compatible with 74HC161

General Description

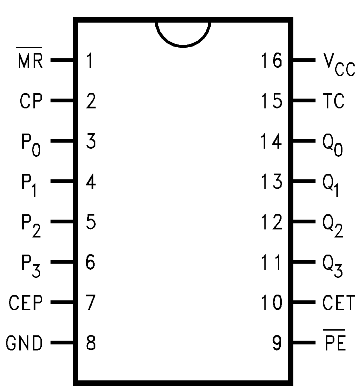
The VHC161 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC161 is a high-speed synchronous modulo-16 binary counter. This device is synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The VHC161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Ordering Information

Order Number	Package Number	Package Description
74VHC161M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC161SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC161MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

Connection Diagram



Pin Description

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$	Asynchronous Master Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Inputs
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

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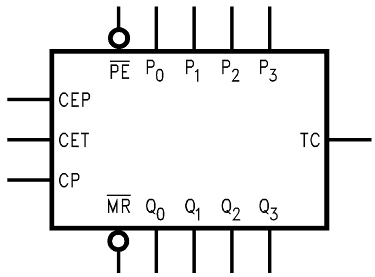
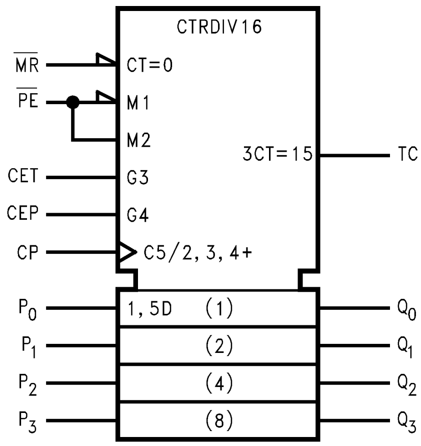
Logic Symbols



IEEE/IEC



Functional Description

The VHC161 counts in modulo-16 binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the VHC161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Five control inputs—Master Reset, Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The VHC161 uses D-type edge-triggered flip-flops and changing the $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative CET to TC delays of the intermediate stages, plus the CET to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min to start its final cycle. Since this final cycle requires 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to TC delay of the first stage plus the CEP to CP setup time of the last stage. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters.

Logic Equations:

Count Enable = CEP • CET • $\overline{PE}$

TC = Q_0 • Q_1 • Q_2 • Q_3 • CET

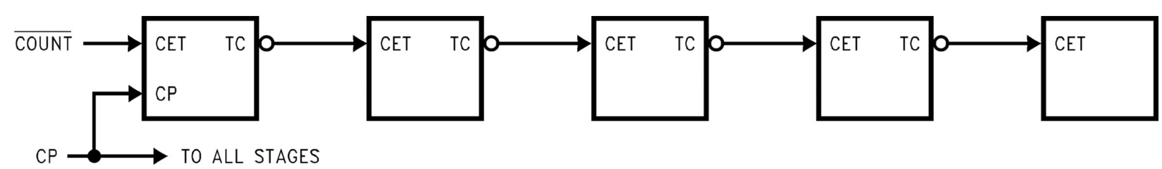


Figure 1. Multistage Counter with Ripple Carry

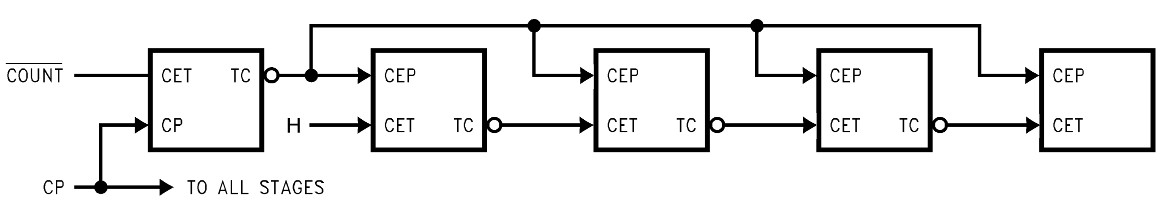


Figure 2. Multistage Counter with Lookahead Carry

Mode Select Table

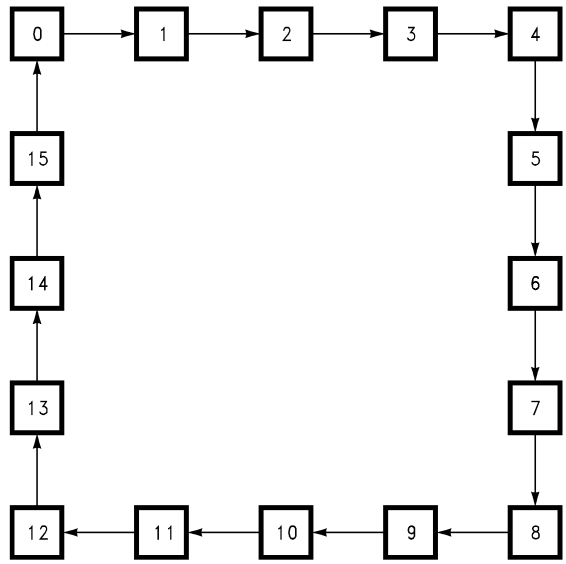
$\overline{MR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⎍)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level

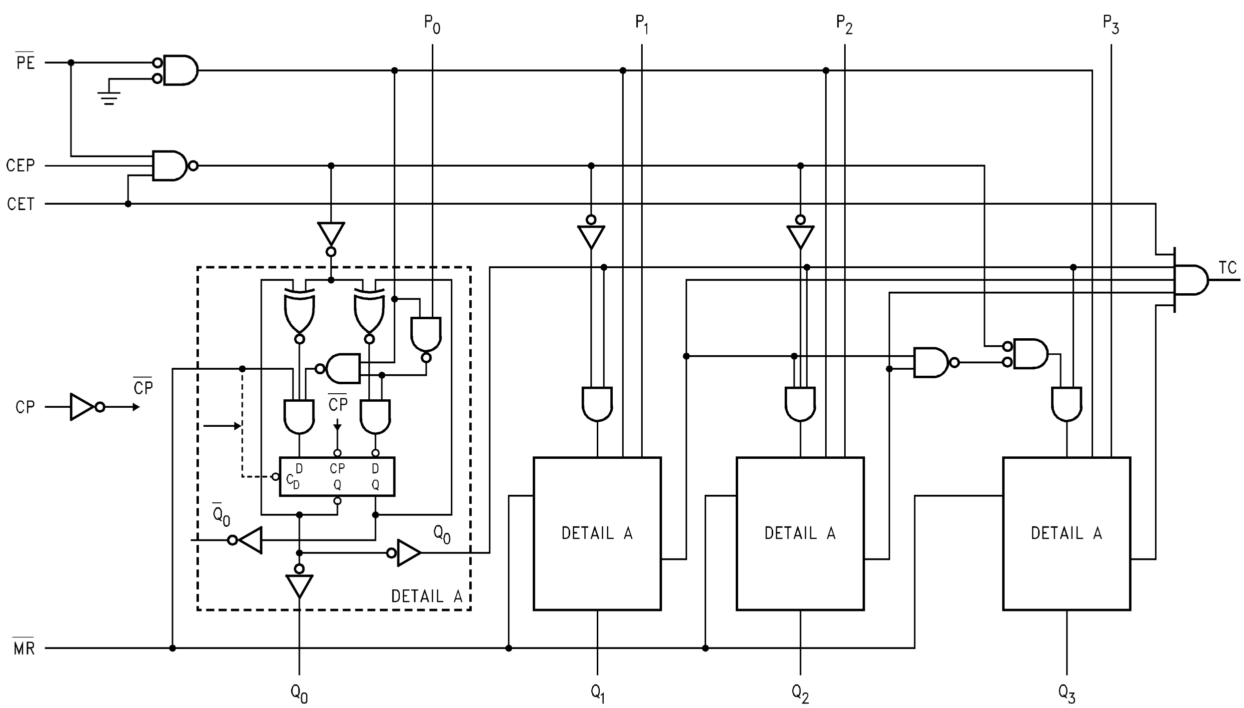
L = LOW Voltage Level

X = Immaterial

State Diagram



Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC} / GND Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time,	
	V_{CC} = 3.3V ± 0.3V	0ns/V ~ 100ns/V
	V_{CC} = 5.0V ± 0.5V	0ns/V ~ 20ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		$T_A = 25°C$			$T_A = –40°C$ to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V
		3.0–5.5			0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V
		3.0–5.5					0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = –50μA$	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		$I_{OH} = –4mA$	2.58			2.48		
		4.5		$I_{OH} = –8mA$	3.94			3.80		
V_{OL}	LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50μA$		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		$I_{OL} = 4mA$			0.36		0.44	
		4.5		$I_{OL} = 8mA$			0.36		0.44	
I_{IN}	Input Leakage Current	0–5.5	V_{IN} = 5.5V or GND				±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND				4.0		40.0	μA

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$		Units
				Typ.	Limits	
V_{OLP}(2)	Quiet Output Maximum Dynamic V_{OL}	5.0	$C_L = 50pF$	0.4	0.8	V
V_{OLV}(2)	Quiet Output Minimum Dynamic V_{OL}	5.0	$C_L = 50pF$	–0.4	–0.8	V
V_{IHD}(2)	Minimum HIGH Level Dynamic Input Voltage	5.0	$C_L = 50pF$		3.5	V
V_{ILD}(2)	Maximum LOW Level Dynamic Input Voltage	5.0	$C_L = 50pF$		1.5	V

Note:

2. Parameter guaranteed by design.

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AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$ Min.	$T_A = 25°C$ Typ.	$T_A = 25°C$ Max.	$T_A = -40°$ to $+85°C$ Min.	$T_A = -40°$ to $+85°C$ Max.	Units
t_{PLH}, t_{PHL}	Propagation Delay Time (CP–Q_n)	3.3 ± 0.3	C_L = 15pF		8.3	12.8	1.0	15.0	ns
			C_L = 50pF		10.8	16.3	1.0	18.5	
		5.0 ± 0.5	C_L = 15pF		4.9	8.1	1.0	9.5	ns
			C_L = 50pF		6.4	10.1	1.0	11.5	
t_{PLH}, t_{PHL}	Propagation Delay Time (CP–TC, Count)	3.3 ± 0.3	C_L = 15pF		8.7	13.6	1.0	16.0	ns
			C_L = 50pF		11.2	17.1	1.0	19.5	
		5.0 ± 0.5	C_L = 15pF		4.9	8.1	1.0	9.5	ns
			C_L = 50pF		6.4	10.1	1.0	11.5	
t_{PLH}, t_{PHL}	Propagation Delay Time (CP–TC, Load)	3.3 ± 0.3	C_L = 15pF		11.0	17.2	1.0	20.0	ns
			C_L = 50pF		13.5	20.7	1.0	23.5	
		5.0 ± 0.5	C_L = 15pF		6.2	10.3	1.0	12.0	ns
			C_L = 50pF		7.7	12.3	1.0	14.0	
t_{PLH}, t_{PHL}	Propagation Delay Time (CET–TC)	3.3 ± 0.3	C_L = 15pF		7.5	12.3	1.0	14.5	ns
			C_L = 50pF		10.5	15.8	1.0	18.0	
		5.0 ± 0.5	C_L = 15pF		4.9	8.1	1.0	9.5	ns
			C_L = 50pF		6.4	10.1	1.0	11.5	
t_{PHL}	Propagation Delay Time ($\overline{MR}$ –Q_n)	3.3 ± 0.3	C_L = 15pF		8.9	13.6	1.0	16.0	ns
			C_L = 50pF		11.2	17.1	1.0	19.5	
		5.0 ± 0.5	C_L = 15pF		5.5	9.0	1.0	10.5	ns
			C_L = 50pF		7.0	11.0	1.0	12.5	
t_{PHL}	Propagation Delay Time ($\overline{MR}$ –TC)	3.3 ± 0.3	C_L = 15pF		8.4	13.2	1.0	15.5	ns
			C_L = 50pF		10.9	16.7	1.0	19.0	
		5.0 ± 0.5	C_L = 15pF		5.0	8.6	1.0	10.0	ns
			C_L = 50pF		6.5	10.6	1.0	12.0	
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	C_L = 15pF	80	130		70		MHz
			C_L = 50pF	55	85		50		
		5.0 ± 0.5	C_L = 15pF	135	185		115		MHz
			C_L = 50pF	95	125		85		
C_{IN}	Input Capacitance		V_{CC} = Open		4	10		10	pF
C_{PD}	Power Dissipation Capacitance		(3)		23				pF

Note:

3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

   I_{CC} (opr) = $C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

   When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and ΔI_{CC} which is obtained from the following formula:

$$\Delta I_{CC} = F_{CP} \bullet V_{CC} \left(\frac{C_{QO}}{2} + \frac{C_{Q1}}{4} + \frac{C_{Q2}}{8} + \frac{C_{Q3}}{16} + \frac{C_{TC}}{16} \right)$$

   C_{Q0}–C_{Q3} and C_{TC} are the capacitances at Q0–Q3 and TC, respectively. F_{CP} is the input frequency of the CP.

AC Operating Requirements

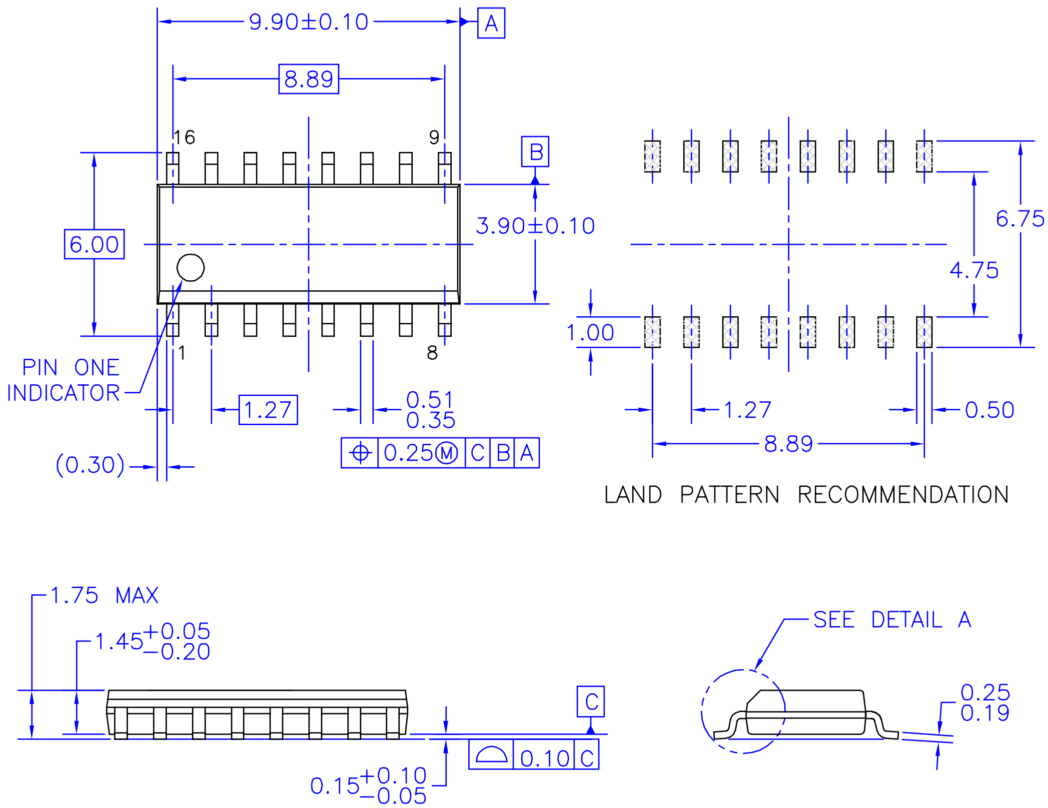
Symbol	Parameter	V_{CC} (V)[4]	$T_A = 25°C$ Typ.	$T_A = 25°C$ Guaranteed Minimum	$T_A = -40°C$ to $+85°C$ Guaranteed Minimum	Units
t_S	Minimum Setup Time (P_n–CP)	3.3		5.5	6.5	ns
		5.0		4.5	4.5	
t_S	Minimum Setup Time ($\overline{PE}$ –CP)	3.3		8.0	9.5	ns
		5.0		5.0	6.0	
t_S	Minimum Setup Time (CEP or CET–CP)	3.3		7.5	9.0	ns
		5.0		5.0	6.0	
t_H	Minimum Hold Time (P_n–CP)	3.3		1.0	1.0	ns
		5.0		1.0	1.0	
t_H	Minimum Hold Time ($\overline{PE}$ –CP)	3.3		1.0	1.0	ns
		5.0		1.0	1.0	
t_H	Minimum Hold Time (CEP or CET–CP)	3.3		1.0	1.0	ns
		5.0		1.0	1.0	
t_W(L), t_W(H)	Minimum Pulse Width CP (Count)	3.3		5.0	5.0	ns
		5.0		5.0	5.0	
t_W(L)	Minimum Pulse Width ($\overline{MR}$)	3.3		5.0	5.0	ns
		5.0		5.0	5.0	
t_{REC}	Minimum Removal Time	3.3		2.5	2.5	ns
		5.0		1.5	1.5	

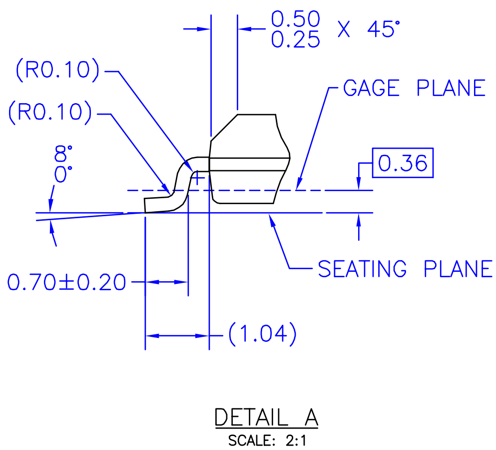
Note:

4. V_{CC} is 3.3 ± 0.3V or 5.0 ± 0.5V.

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.





NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS−012, VARIATION AC, ISSUE C, DATED MAY 1990.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

D) STANDARD LEAD FINISH: 200 MICROINCHES / 5.08 MICRONS MIN. LEAD/TIN (SOLDER) ON COPPER.

M16AREVK

Figure 3. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

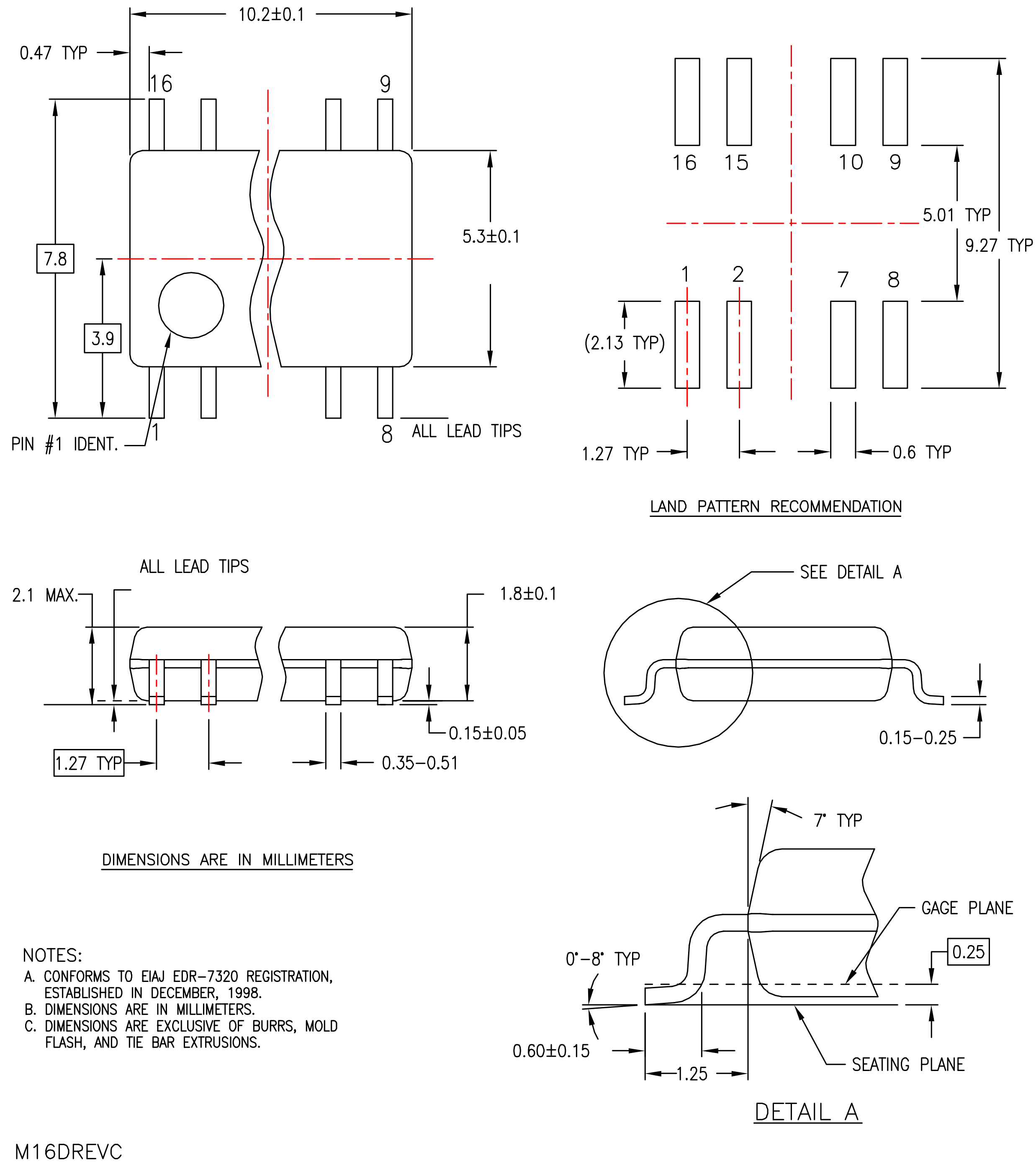
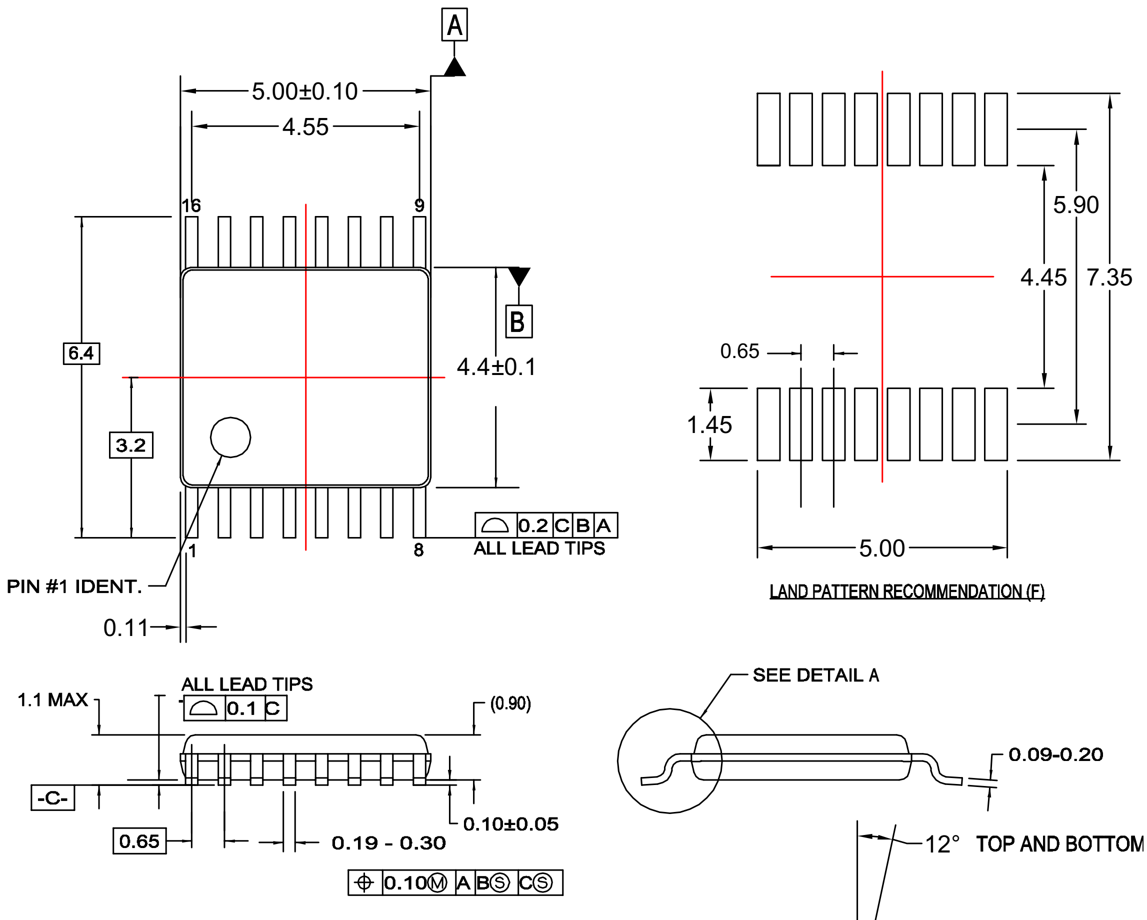
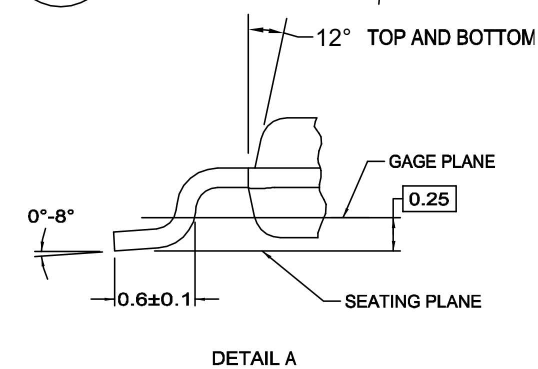


Figure 4. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.





NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REV4
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 5. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16

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Definition of Terms

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