

74LVC32A

Low-Voltage CMOS Quad 2-Input OR Gate

With 5 V-Tolerant Inputs

The 74LVC32A is a high performance, quad 2-input OR gate operating from a 1.2 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows 74LVC32A inputs to be safely driven from 5.0 V devices.

Current drive capability is 24 mA at the outputs.

Features

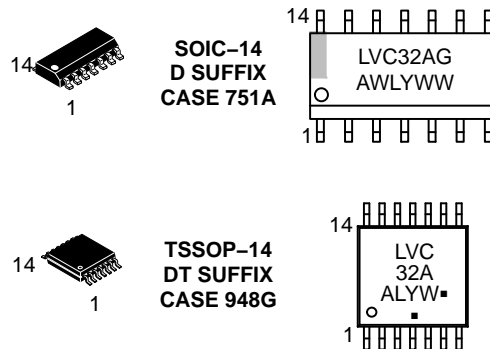
- Designed for 1.2 V to 3.6 V V_{CC} Operation
- 5.0 V Tolerant Inputs – Interface Capability With 5.0 V TTL Logic
- 24 mA Output Sink and Source Capability
- Near Zero Static Supply Current (10 μ A) Substantially Reduces System Power Requirements
- ESD Performance: Human Body Model >2000 V
Machine Model >200 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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MARKING DIAGRAMS



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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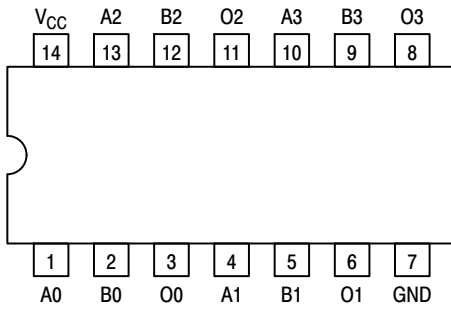


Figure 1. Pinout: 14-Lead (Top View)

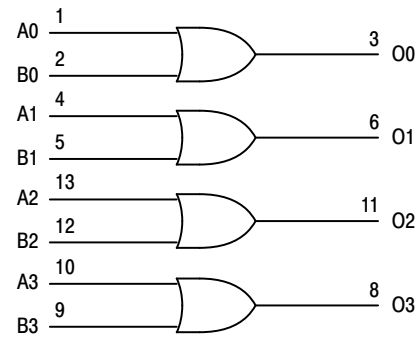


Figure 2. Logic Diagram

PIN NAMES

| Pins | Function |
|--------|-------------|
| An, Bn | Data Inputs |
| On | Outputs |

TRUTH TABLE

| Inputs | | Outputs |
|--------|----|---------|
| An | Bn | On |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

H = High Voltage Level

L = Low Voltage Level

For I_{CC} reasons, DO NOT FLOAT Inputs

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MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Unit |
|---------------|--|-----------------------------------|---|------|
| V_{CC} | DC Supply Voltage | -0.5 to +6.5 | | V |
| V_I | DC Input Voltage | $-0.5 \leq V_I \leq +6.5$ | | V |
| V_O | DC Output Voltage | $-0.5 \leq V_O \leq V_{CC} + 0.5$ | Output in HIGH or LOW State (Note 1) | V |
| I_{IK} | DC Input Diode Current | -50 | $V_I < GND$ | mA |
| I_{OK} | DC Output Diode Current | -50 | $V_O < GND$ | mA |
| | | +50 | $V_O > V_{CC}$ | mA |
| I_O | DC Output Source/Sink Current | ± 50 | | mA |
| I_{CC} | DC Supply Current Per Supply Pin | ± 100 | | mA |
| I_{GND} | DC Ground Current Per Ground Pin | ± 100 | | mA |
| T_{STG} | Storage Temperature Range | -65 to +150 | | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds | $T_L = 260$ | | °C |
| T_J | Junction Temperature Under Bias | $T_J = 135$ | | °C |
| θ_{JA} | Thermal Resistance (Note 2) | SOIC = 85 TSSOP = 100 | | °C/W |
| MSL | Moisture Sensitivity | | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
|---------------------|---|-------------|-----|-----------------|-------|
| V_{CC} | Supply Voltage Operating Functional | 1.65 1.2 | | 3.6 3.6 | V |
| V_I | Input Voltage | 0 | | 5.5 | V |
| V_O | Output Voltage HIGH or LOW State 3-State | 0 0 | | V_{CC} 5.5 | V |
| I_{OH} | HIGH Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ | | | -24 -12 | mA |
| I_{OL} | LOW Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ | | | 24 12 | mA |
| T_A | Operating Free-Air Temperature | -40 | | +125 | °C |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate $V_{CC} = 1.65\text{ V to } 2.7\text{ V}$ $V_{CC} = 2.7\text{ V to } 3.6\text{ V}$ | 0 0 | | 20 10 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | -40°C to +85°C | | | -40°C to +125°C | | | Unit |
|------------------|---------------------------|---|------------------------|-----------------|------------------------|------------------------|-----------------|------------------------|------|
| | | | Min | Typ (Note 3) | Max | Min | Typ (Note 3) | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | 1.08 | – | – | 1.08 | – | – | V |
| | | V _{CC} = 1.65 V to 1.95 V | 0.65 x V _{CC} | – | – | 0.65 x V _{CC} | – | – | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | – | – | 1.7 | – | – | |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | – | – | 2.0 | – | – | |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.2 V | – | – | 0.12 | – | – | 0.12 | V |
| | | V _{CC} = 1.65 V to 1.95 V | – | – | 0.35 x V _{CC} | – | – | 0.35 x V _{CC} | |
| | | V _{CC} = 2.3 V to 2.7 V | – | – | 0.7 | – | – | 0.7 | |
| | | V _{CC} = 2.7 V to 3.6 V | – | – | 0.8 | – | – | 0.8 | |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | V |
| | | I _O = –100 µA; V _{CC} = 1.65 V to 3.6 V | V _{CC} – 0.2 | – | – | V _{CC} – 0.3 | – | – | |
| | | I _O = –4 mA; V _{CC} = 1.65 V | 1.2 | – | – | 1.05 | – | – | |
| | | I _O = –8 mA; V _{CC} = 2.3 V | 1.8 | – | – | 1.65 | – | – | |
| | | I _O = –12 mA; V _{CC} = 2.7 V | 2.2 | – | – | 2.05 | – | – | |
| | | I _O = –18 mA; V _{CC} = 3.0 V | 2.4 | – | – | 2.25 | – | – | |
| | | I _O = –24 mA; V _{CC} = 3.0 V | 2.2 | – | – | 2.0 | – | – | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | V |
| | | I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V | – | – | 0.2 | – | – | 0.3 | |
| | | I _O = 4 mA; V _{CC} = 1.65 V | – | – | 0.45 | – | – | 0.65 | |
| | | I _O = 8 mA; V _{CC} = 2.3 V | – | – | 0.6 | – | – | 0.8 | |
| | | I _O = 12 mA; V _{CC} = 2.7 V | – | – | 0.4 | – | – | 0.6 | |
| | | I _O = 24 mA; V _{CC} = 3.0 V | – | – | 0.55 | – | – | 0.8 | |
| I _I | Input leakage current | V _I = 5.5V or GND; V _{CC} = 3.6 V | – | ±0.1 | ±5 | – | ±0.1 | ±20 | µA |
| I _{OFF} | Power-off leakage current | V _I or V _O = 5.5 V; V _{CC} = 0.0 V | – | ±0.1 | ±10 | – | ±0.1 | ±20 | µA |
| I _{CC} | Supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 3.6 V | – | 0.1 | 10 | – | 0.1 | 40 | µA |
| ΔI _{CC} | Additional supply current | per input pin; V _I = V _{CC} – 0.6 V; I _O = 0 A; V _{CC} = 2.7 V to 3.6 V | – | 5 | 500 | – | 5 | 5000 | µA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. All typical values are measured at T_A = 25°C and V_{CC} = 3.3 V, unless stated otherwise.

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AC ELECTRICAL CHARACTERISTICS ($t_R = t_F = 2.5 \text{ ns}$)

| Symbol | Parameter | Conditions | -40°C to +85°C | | | -40°C to +125°C | | | Unit |
|-------------|----------------------------|--|----------------|------------------|-----|-----------------|------------------|------|------|
| | | | Min | Typ ¹ | Max | Min | Typ ¹ | Max | |
| t_{pd} | Propagation Delay (Note 5) | $V_{CC} = 1.2 \text{ V}$ | – | 10.0 | – | – | – | – | ns |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 0.5 | 4.2 | 9.0 | 0.5 | – | 10.4 | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.0 | 2.4 | 4.9 | 1.0 | – | 5.7 | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 1.0 | 2.5 | 4.4 | 1.0 | – | 5.5 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.0 | 2.2 | 3.8 | 1.0 | – | 5.0 | ns |
| $t_{sk(0)}$ | Output Skew Time (Note 6) | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | – | – | 1.0 | – | – | 1.5 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Typical values are measured at $T_A = 25^\circ\text{C}$ and $V_{CC} = 3.3 \text{ V}$, unless stated otherwise.

5. t_{pd} is the same as t_{PLH} and t_{PHL} .

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Characteristic | Condition | $T_A = +25^\circ\text{C}$ | | | Unit |
|-----------|-------------------------------------|--|---------------------------|--------------|-----|------|
| | | | Min | Typ | Max | |
| V_{OLP} | Dynamic LOW Peak Voltage (Note 7) | $V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ $V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ | | 0.8 0.6 | | V |
| V_{OLV} | Dynamic LOW Valley Voltage (Note 7) | $V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ $V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ | | -0.8 -0.6 | | V |

7. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Unit |
|-----------|--|--|---------|------|
| C_{IN} | Input Capacitance | $V_{CC} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CC}$ | 4.0 | pF |
| C_{OUT} | Output Capacitance | $V_{CC} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CC}$ | 5.0 | pF |
| C_{PD} | Power Dissipation Capacitance (Note 8) | Per input; $V_I = \text{GND or } V_{CC}$ | | pF |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 4.7 | |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 8.0 | |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 11.0 | |

8. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

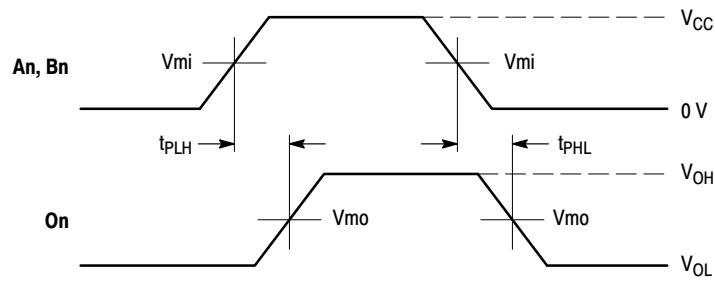
f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF V_{CC} = supply voltage in Volts

N = number of outputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

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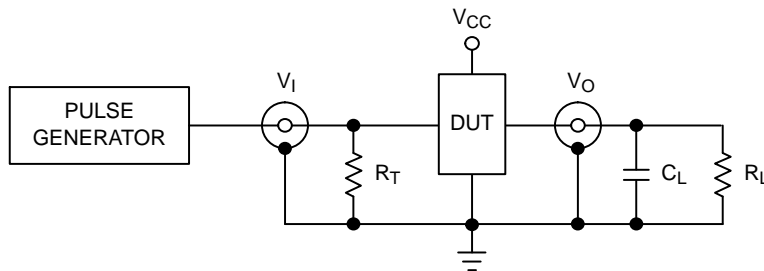


WAVEFORM 1 – PROPAGATION DELAYS

$t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$

| Symbol | Vcc | | |
|--------|-------------------|-------|-------------|
| | 3.3 V \pm 0.3 V | 2.7 V | Vcc < 2.7 V |
| Vmi | 1.5 V | 1.5 V | Vcc/2 |
| Vmo | 1.5 V | 1.5 V | Vcc/2 |

Figure 3. AC Waveforms



C_L includes jig and probe capacitance
 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

| Supply Voltage | Input | | Load | |
|----------------|-------|-----------------------|-------|--------------|
| Vcc (V) | Vi | tr, tf | CL | RL |
| 1.2 | Vcc | $\leq 2 \text{ ns}$ | 30 pF | 1 k Ω |
| 1.65 – 1.95 | Vcc | $\leq 2 \text{ ns}$ | 30 pF | 1 k Ω |
| 2.3 – 2.7 | Vcc | $\leq 2 \text{ ns}$ | 30 pF | 500 Ω |
| 2.7 | 2.7 V | $\leq 2.5 \text{ ns}$ | 50 pF | 500 Ω |
| 3 – 3.6 | 2.7 V | $\leq 2.5 \text{ ns}$ | 50 pF | 500 Ω |

Figure 4. Test Circuit

ORDERING INFORMATION

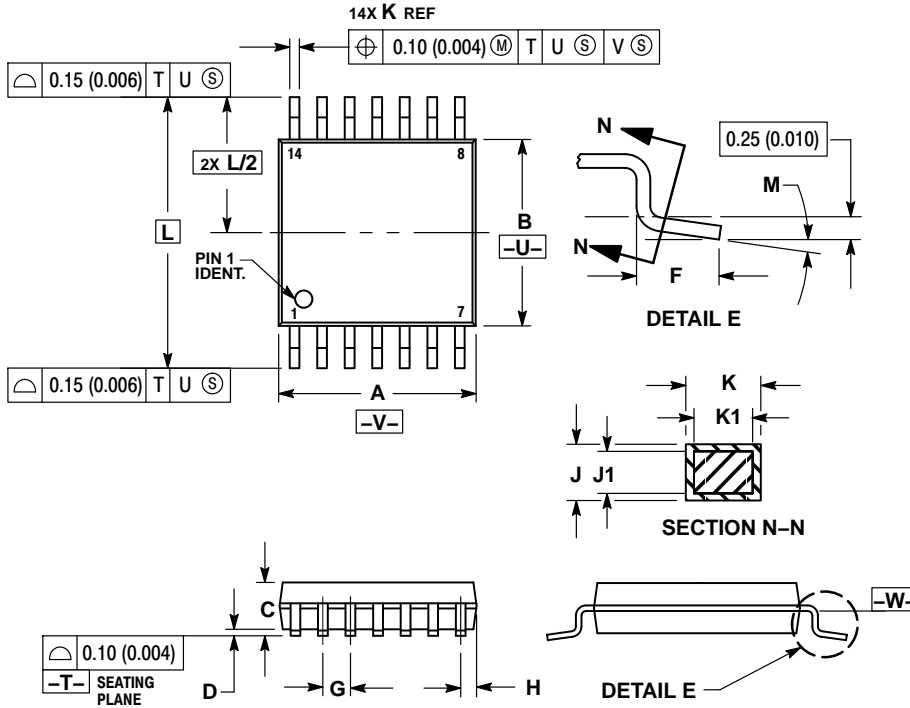
| Device | Package | Shipping [†] |
|---------------|-----------------------|-----------------------|
| 74LVC32ADR2G | SOIC-14 (Pb-Free) | 2500 / Tape & Reel |
| 74LVC32ADTR2G | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

TSSOP-14
CASE 948G
ISSUE B

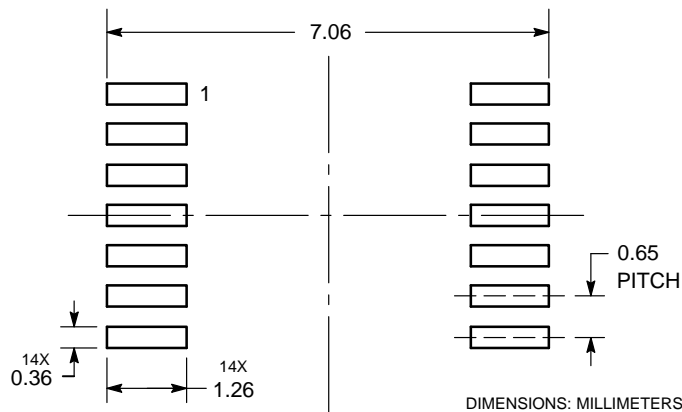


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | — | 1.20 | — | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*

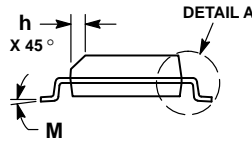
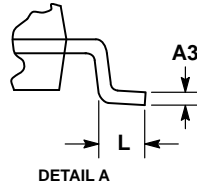
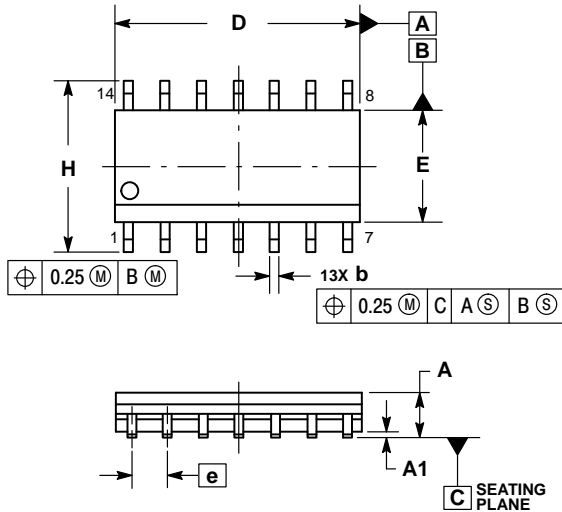


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 ISSUE K

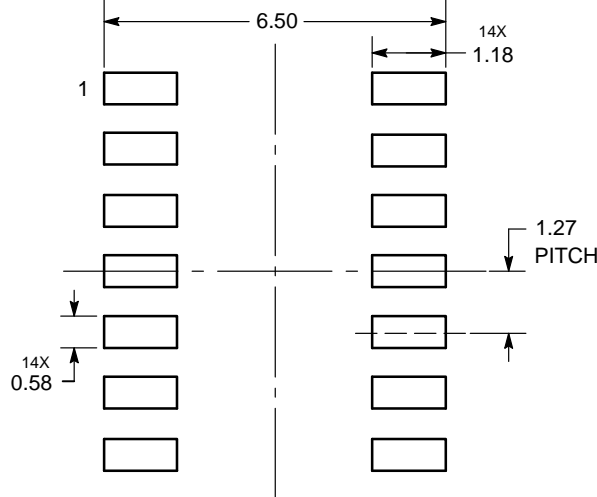


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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