

# Low Voltage Hex Inverter with 5 V Tolerant Schmitt Trigger Inputs

## 74LCX14

### General Description

The LCX14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The LCX14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0 V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

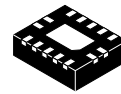
The inputs tolerate voltages up to 7 V allowing the interface of 5 V, 3 V and 2.5 V systems.

The 74LCX14 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

### Features

- 5 V Tolerant Inputs
- 1.65 V–5.5 V  $V_{CC}$  Specifications Provided
- 6.5ns  $t_{PD}$  Max. ( $V_{CC} = 3.3$  V), 10  $\mu$ A  $I_{CC}$  Max.
- Power Down High Impedance Inputs and Outputs
- $\pm 24$  mA Output Drive ( $V_{CC} = 3.0$  V)
- Implements Proprietary Noise/EMI Reduction Circuitry
- Latch-up Performance Exceeds JEDEC 78 Conditions
- ESD Performance:
  - ♦ Human Body Model > 2000 V
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

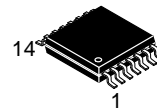
### MARKING DIAGRAMS



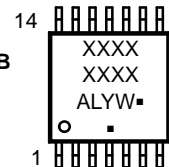
QFN14 3.0x2.5, 0.5P  
CASE 510CB

ZXYKK  
XXXXXX

XXXXXX = Specific Device Code  
Z = Assembly Plant Code  
XY = Date Code (Year & Week)  
KK = Lot Run Traceability Code



TSSOP-14 WB  
DT SUFFIX  
CASE 948G



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

74LCX14

Connection Diagrams

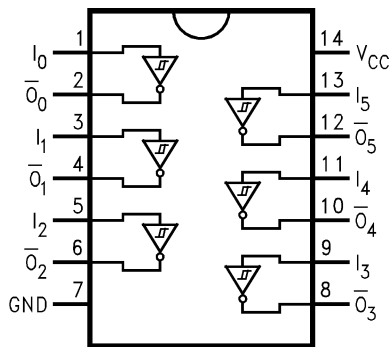


Figure 1. Pin Assignment for TSSOP

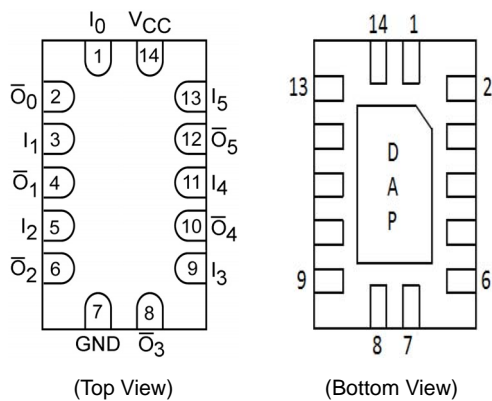


Figure 2. Pin Assignment for DQFN

Logic Symbol

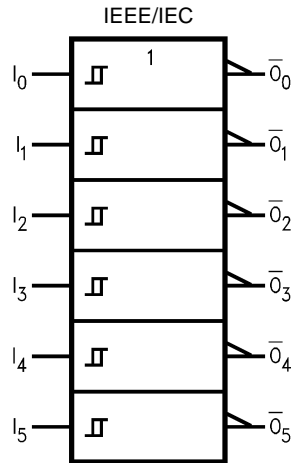


Figure 3. Logic Symbol

TRUTH TABLE

Input	Output
A	$\bar{O}$
L	H
H	L

PIN DESCRIPTION

Pin Names	Description
$I_n$	Inputs
$\bar{O}_n$	Outputs
DAP	No Connect

1. DAP (Die Attach Pad)

# 74LCX14

## MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
$V_{CC}$	DC Supply Voltage		–0.5 to +6.5	V
$V_I$	DC Input Voltage (Note 2)		–0.5 to +6.5	V
$V_O$	DC Output Voltage (Note 2)	Active–Mode (High or Low State)	–0.5 to $V_{CC} + 0.5$	V
		Tri–State Mode	–0.5 to +6.5	
		Power–Down Mode ( $V_{CC} = 0$ V)	–0.5 to +6.5	
$I_{IK}$	DC Input Diode Current $V_I < GND$		–50	mA
$I_{OK}$	DC Output Diode Current $V_O < GND$		–50	mA
$I_O$	DC Output Source/Sink Current		$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC Supply Current per Supply Pin or Ground Pin		$\pm 100$	mA
$T_{STG}$	Storage Temperature Range		–65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
$T_J$	Junction Temperature under Bias		+150	°C
$\theta_{JA}$	Thermal Resistance (Note 2)	QFN14	130	°C/W
		TSSOP–14	150	
$P_D$	Power Dissipation in Still Air at 125°C	QFN14	962	mW
		TSSOP–14	833	
MSL	Moisture Sensitivity		Level 1	
$F_R$	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage (Note 4)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- $I_O$  absolute maximum rating must be observed.
- Measured with minimum pad spacing on an FR4 board, using 76 mm–by–114 mm, 2–ounce copper trace no air flow per JESD51–7.
- HBM tested to EIA / JESD22–A114–A. CDM tested to JESD22–C101–A. JEDEC recommends that ESD qualification to EIA/JESD22–A115A (Machine Model) be discontinued.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	Operating	1.65	2.5, 3.3	5.5	V
		Data Retention Only	1.5	2.5, 3.3	5.5	
$V_I$	Digital Input Voltage		0	–	5.5	V
$V_O$	Output Voltage	Active Mode (High or Low State)	0	–	$V_{CC}$	V
		Tri–State Mode	0	–	5.5	
		Power Down Mode ( $V_{CC} = 0$ V)	0	–	5.5	
$T_A$	Operating Free–Air Temperature		–40	–	+125	°C
$t_r, t_f$	Input Rise or Fall Rate		0	–	No Limit	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

# 74LCX14

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		T <sub>A</sub> = -40°C to +125°C		Unit
				Min	Max	Min	Max	
V <sub>T+</sub>	Positive-Input Threshold Voltage		1.65	–	1.4	–	1.4	V
			2.5	0.9	1.7	0.9	1.7	
			3.0	1.2	2.2	1.2	2.2	
			4.5	–	3.1	–	3.1	
			5.5	–	3.6	–	3.6	
V <sub>T-</sub>	Negative-Input Threshold Voltage		1.65	0.2	–	0.2	–	V
			2.5	0.4	1.1	0.4	1.1	
			3.0	0.6	1.5	0.6	1.5	
			4.5	1	–	1	–	
			5.5	1.2	–	1.2	–	
V <sub>H</sub>	Hysteresis Voltage		1.65	0.1	0.9	0.1	0.9	V
			2.5	0.3	1.0	0.3	1.0	
			3.0	0.4	1.2	0.4	1.2	
			4.5	0.6	1.5	0.6	1.5	
			5.5	0.7	1.7	0.7	1.7	
V <sub>OH</sub>	High-Level Output Voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.65 to 5.5	V <sub>CC</sub> – 0.1	–	V <sub>CC</sub> – 0.1	–	V
		I <sub>OH</sub> = –100 μA	1.65	1.29	–	1.29	–	
		I <sub>OH</sub> = –4 mA	2.3	1.8	–	1.8	–	
		I <sub>OH</sub> = –8 mA	2.7	2.2	–	2.2	–	
		I <sub>OH</sub> = –12 mA	3.0	2.4	–	2.4	–	
		I <sub>OH</sub> = –16 mA	3.0	2.2	–	2.2	–	
		I <sub>OH</sub> = –24 mA	4.5	3.7	–	3.7	–	
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.65 to 5.5	–	0.1	–	0.1	V
		I <sub>OL</sub> = 100 μA	1.65	–	0.24	–	0.24	
		I <sub>OL</sub> = 4 mA	2.3	–	0.3	–	0.3	
		I <sub>OL</sub> = 8 mA	2.7	–	0.4	–	0.4	
		I <sub>OL</sub> = 12 mA	3.0	–	0.4	–	0.4	
		I <sub>OL</sub> = 16 mA	3.0	–	0.55	–	0.55	
		I <sub>OL</sub> = 24 mA	4.5	–	0.6	–	0.6	
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>I</sub> = 5.5 V or V <sub>O</sub> = 5.5 V	0	–	10	–	10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = 5.5 V or GND	3.6	–	10	–	10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> – 0.6 V	2.3 to 3.6	–	500	–	500	μA

# 74LCX14

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		T <sub>A</sub> = -40°C to +125°C		Unit
				Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, Input to Output	See Figures 3 and 4	1.65 to 1.95	–	15.7	–	15.7	ns
			2.3 to 2.7	1.5	7.8	1.5	7.8	
			2.7	1.5	7.5	1.5	7.5	
			3.0 to 3.6	1.5	6.5	1.5	6.5	
			4.5 to 5.5	–	5.6	–	5.6	
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	
			4.5 to 5.5	–	–	–	–	

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

## DYNAMIC SWITCHING CHARACTERISTICS

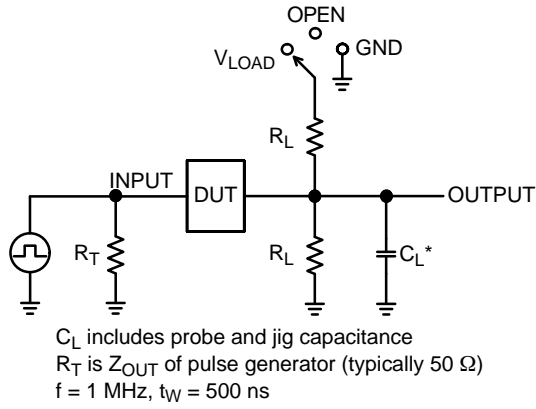
Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C	Unit
				Typ	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V	2.5	0.6	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	–0.8	V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V	2.5	–0.6	

## CAPACITANCE

Symbol	Parameter	Condition	Typ	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0 V or V <sub>CC</sub>	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub> , f = 10 MHz	25	pF

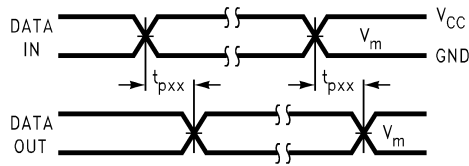
## 74LCX14

### AC Loading and Waveforms (Generic for LCX Family)

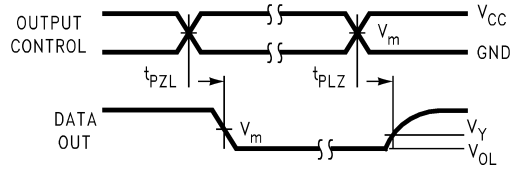


Test	Switch Position
$t_{PLH} / t_{PHL}$	Open
$t_{PLZ} / t_{PZL}$	$V_{LOAD}$
$t_{PHZ} / t_{PZH}$	GND

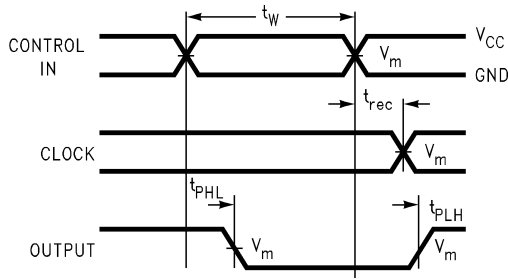
Figure 4. Test Circuit



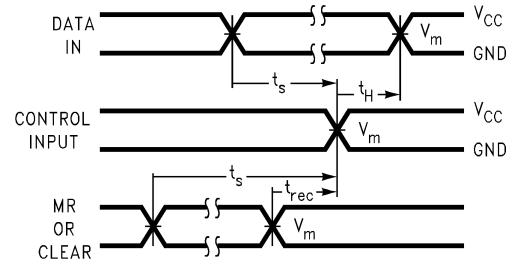
Waveform for Inverting and Non-Inverting Functions



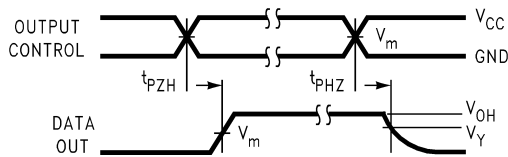
3-STATE Output High Enable and Disable Times for Logic



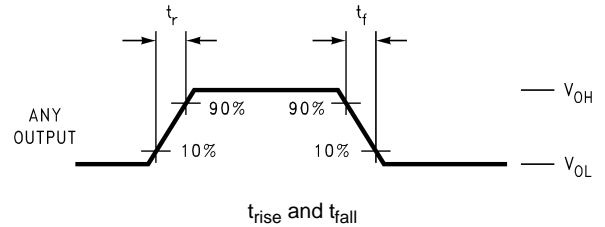
Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic



$V_{CC}$ , V	$R_L$ , $\Omega$	$C_L$ , pF	$V_{LOAD}$	$V_m$ , V	$V_Y$ , V
1.65 to 1.95	500	30	$2 \times V_{CC}$	$V_{CC} / 2$	0.15
2.3 to 2.7	500	30	$2 \times V_{CC}$	$V_{CC} / 2$	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	$2 \times V_{CC}$	$V_{CC} / 2$	0.3

Figure 5. Waveforms (Input Characteristics;  $f = 1$  MHz,  $t_r = t_f = 2.5$  ns)

# 74LCX14

## Schematic Diagram (Generic for LCX Family)

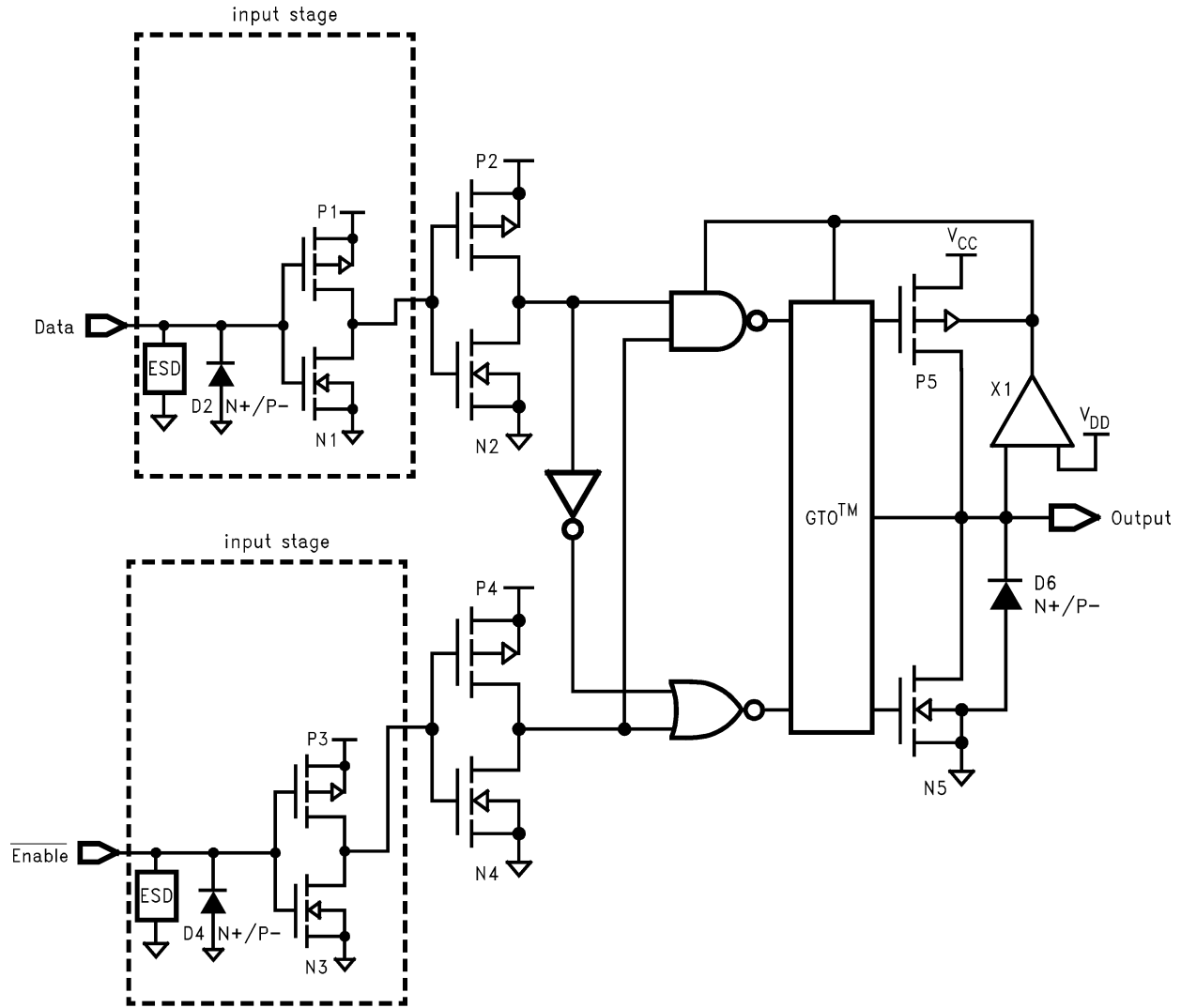


Figure 6. Schematic Diagram

## ORDERING INFORMATION

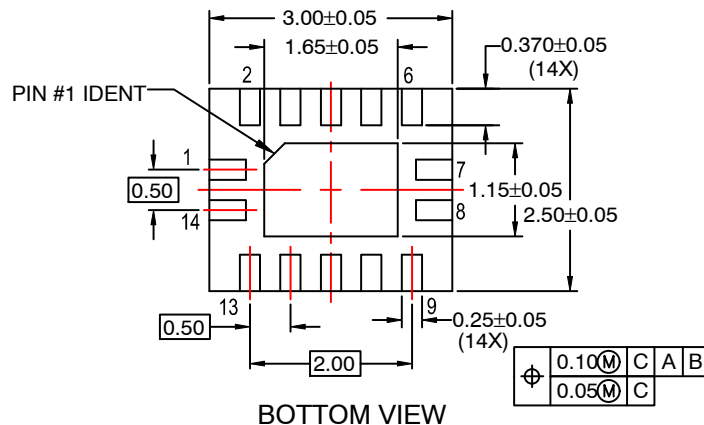
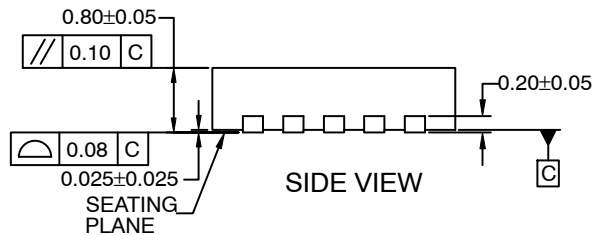
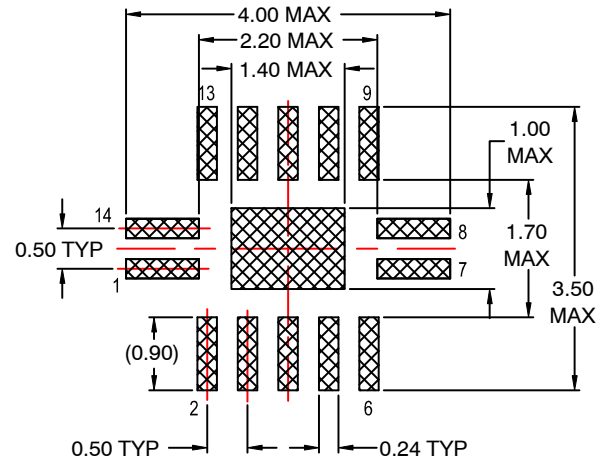
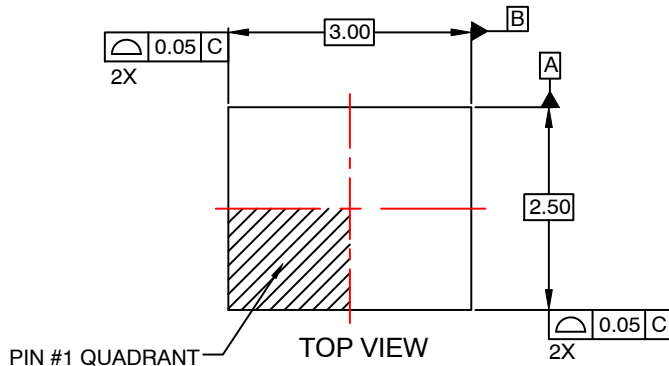
Device	Marking	Package	Shipping†
74LCX14MTCX	LCX 14	TSSOP-14 (Pb-Free, Halide Free)	2500 Units / Tape & Reel
74LCX14BQX	LCX14	QFN14 (Pb-Free, Halide Free)	3000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

**QFN14 3.0x2.5, 0.5P**  
CASE 510CB  
ISSUE O

DATE 31 AUG 2016



**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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<b>DESCRIPTION:</b>	<b>QFN14 3.0X2.5, 0.5P</b>	<b>PAGE 1 OF 1</b>

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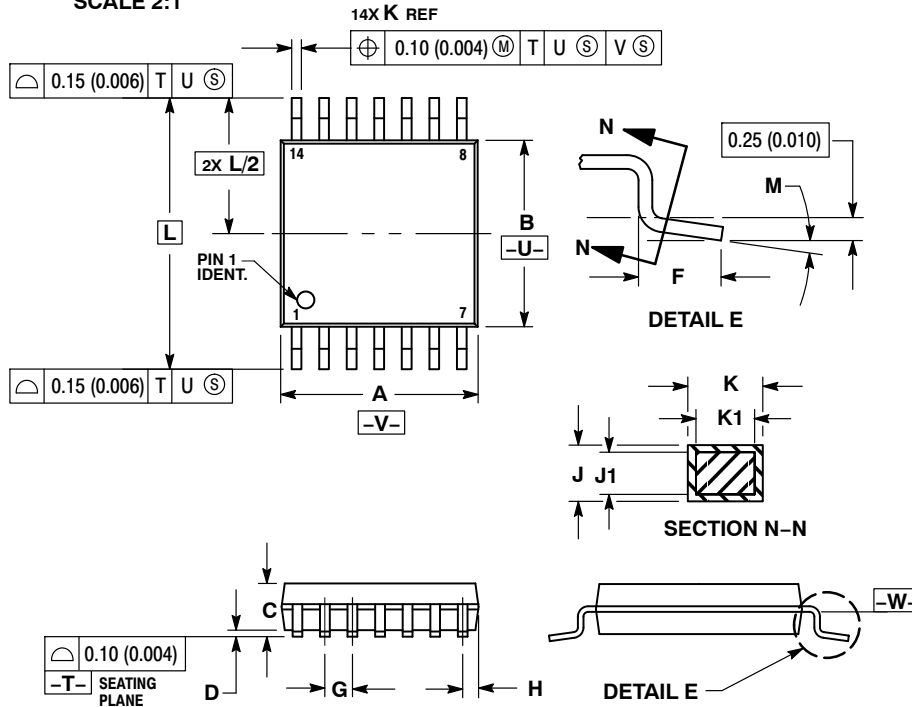




SCALE 2:1

**TSSOP-14 WB**  
CASE 948G  
ISSUE C

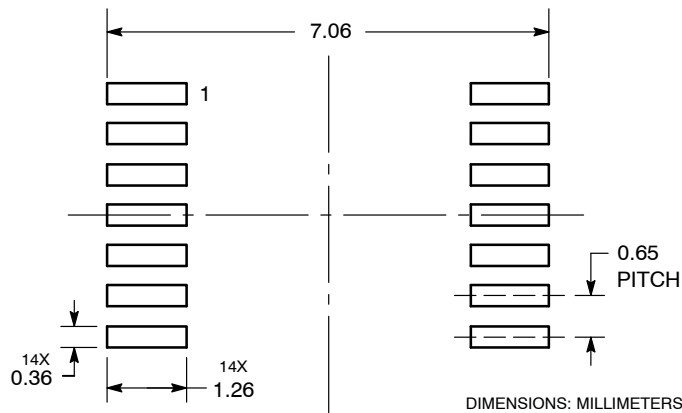
DATE 17 FEB 2016



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED  
SOLDERING FOOTPRINT\***


\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**DOCUMENT NUMBER:** 98ASH70246A

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**DESCRIPTION:** TSSOP-14 WB

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