

NCP4206

VR11.1 Digital Programmable Multi-Phase Synchronous Buck Converter with SMBus

The NCP4206 is an integrated power control IC with a SMBus interface. The NCP4206 is a highly efficient, multiphase, synchronous buck switching regulator controller, which aids design of High Efficiency and High Density solutions. The NCP4206 can be programmed for 1-, 2-, 3-, 4-, 5- or 6 phase operation, allowing for the construction of up to 6 complementary buck switching stages.

The NCP4206 supports $\overline{\text{PSI}}$, which is a power state indicator and can be used to reduce the number of operating phases at light loads. The SMBus interface enables digital programming of key system parameters to optimize system performance and provide feedback to the system.

The NCP4206 has a built in shunt regulator that allows the part to be powered from the +12 V system supply through a series resistor. The NCP4206 is specified over the extended commercial temperature range of 0°C to +85°C and is available in a 48 Lead QFN package.

Features

- Selectable 1-, 2-, 3-, 4-, 5- or 6 Phase Operation at Up to 1.5 MHz per Phase
- Logic-level PWM Outputs for Interface to External High Power Drivers
- Fast-Enhanced PWM Flex Mode for Excellent Load Transient Performance
- Active Current Balancing Between All Output Phases
- Built-in Power-good/Crowbar Blanking Supports On-the-Fly VID Code Changes
- Digitally Programmable 0.375 V to 1.6 V Output Supports VR11.1 Specifications
- Short-Circuit Protection With Latch-off Delay
- Supports $\overline{\text{PSI}}\#$ – Power Saving Mode During Light Loads
- This is a Pb-Free Device

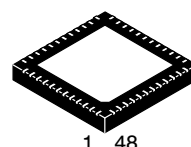
Typical Applications

- Desktop PC
- Servers



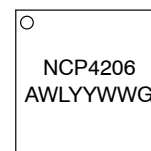
ON Semiconductor®

<http://onsemi.com>



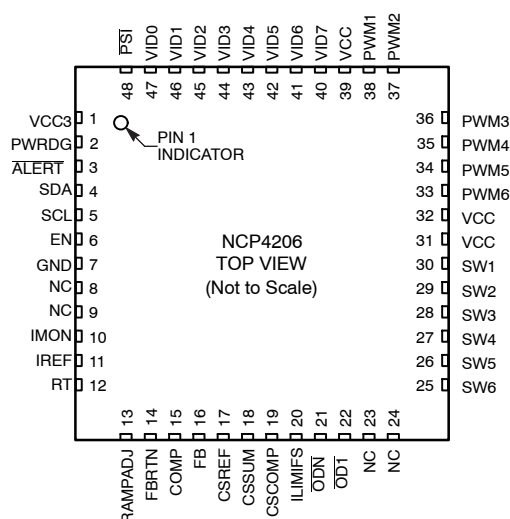
QFN 48
CASE 485AJ

MARKING DIAGRAM



A = Assembly Lot
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

PIN ASSIGNMENT



ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|-----------------|--------------------|
| NCP4206MNR2G | QFN48 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP4206

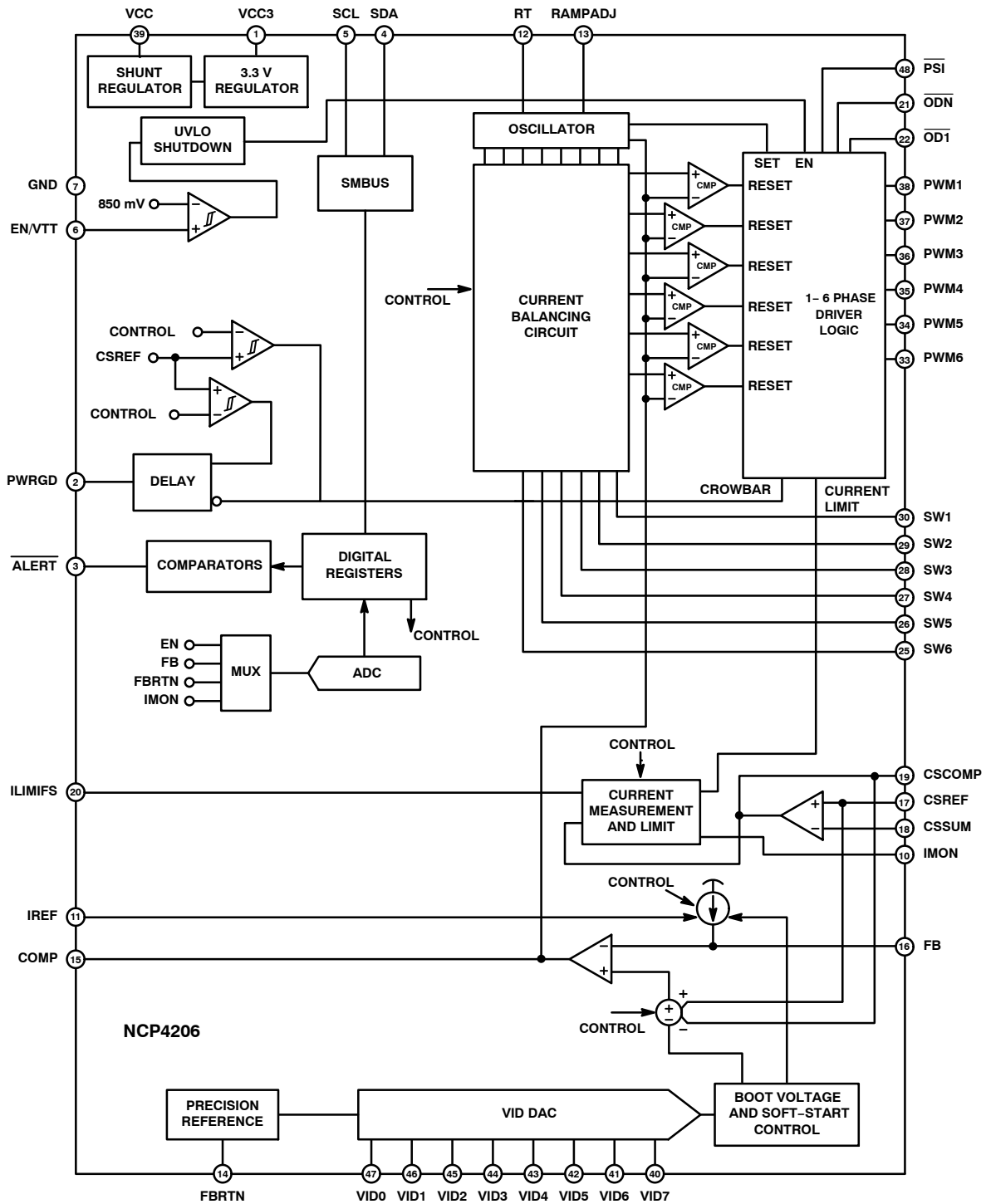


Figure 1. Simplified Block Diagram

NCP4206

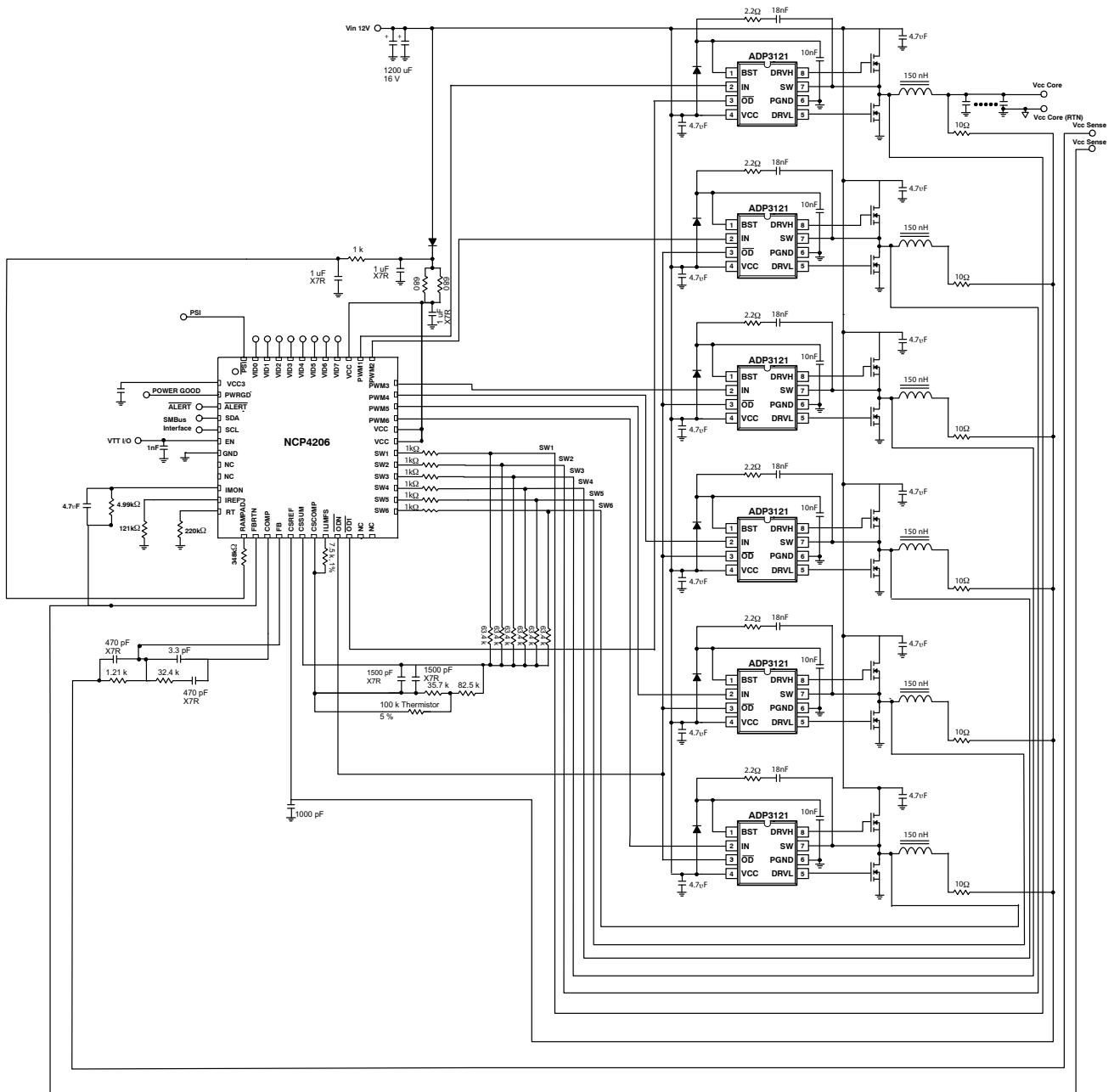


Figure 2. Applications Schematic

NCP4206

Table 1. PIN ASSIGNMENT

| Pin No. | Mnemonic | Description |
|--------------|--------------|--|
| 1 | VCC3 | 3.3 V Power Supply Output. A capacitor from this pin to ground provided decoupling for the internal 3.3 V LDO. |
| 2 | PWRGD | Power-Good Output: Open-drain output that signals when the output voltage is outside of the proper operating range. |
| 3 | ALERT | ALERT Output : Open drain output that asserts low when the VR exceeds a programmable limit. Can be configured for Comparator Mode or Interrupt Mode. |
| 4 | SDA | Digital Input / Output. SMBus serial data bidirectional pin. Requires SMBus pull-up. |
| 5 | SCL | Digital Input. SMBus serial bus clock open drain input. Requires SMBus pull-up. |
| 6 | EN | Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low. |
| 7 | GND | Ground. All internal biasing and the logic output signals of the device are referenced to this ground |
| 8 to 9 | NC | No Connect |
| 10 | IMON | Total Current Output Pin. |
| 11 | IREF | Current Reference Input. An external resistor from this pin to ground sets the reference current for I_{FB} , and I_{LIMFS} . |
| 12 | RT | Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device. |
| 13 | RAMPADJ | PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp. |
| 14 | FBRTN | Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage. |
| 15 | COMP | Error Amplifier Output and Compensation Point. |
| 16 | FB | Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no load offset point. |
| 17 | CSREF | Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power-good and crowbar functions. This pin should be connected to the common point of the output inductors. |
| 18 | CSSUM | Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current. |
| 19 | CSCOMP | Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the gain of the current sense amplifier and the positioning loop response time. |
| 20 | ILIMFS | Current Sense and Limit Scaling Pin. An external resistor from this pin to CSCOMP sets the internal current sensing signal for current-limit and IMON. This value can be over-written using the SMBus interface. |
| 21 | ODN | Output Disable Logic Output for PSI operation. This pin is actively pulled low when PSI is low, otherwise it functions in the same way as OD1. |
| 22 | OD1 | Output Disable Logic Output. This pin is actively pulled low when the EN input is low or when VCC is below its UVLO threshold to signal to the Driver IC that the driver high-side and low-side outputs should go low. |
| 23 to 24 | NC | No Connection |
| 25 to 30 | SW6 to SW1 | Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open. |
| 31 to 32, 39 | VCC | Supply Voltage for the Device. A 340 Ω resistor should be placed between the 12 V system supply and the VCC pin. The internal shunt regulator maintains $V_{CC} = 5$ V. |
| 33 to 38 | PWM6 to PWM1 | Logic-Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3121. Connecting the PWM6, PWM5, PWM4, PWM3 and PWM2 outputs to VCC causes that phase to turn off, allowing the NCP4206 to operate as a 1, 2-, 3-, 4-, 5- or 6, phase controller. |
| 40 to 47 | VID7 to VID0 | Voltage Identification DAC Inputs. These eight pins are pulled down to GND, providing a logic zero if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.375 V to 1.6 V. |
| 48 | PSI | Power State Indicator. Pulling this pin low places the controller in lower power state operation. |

Table 2. ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|-------------|------------------------|------|
| Input Voltage Range (Note 1) | V_{in} | -0.3 to 6 | V |
| FBRTN | V_{FBRTN} | -0.3 to +0.3 V | V |
| PWM2 to PWM6, Rampadj | | -0.3 to $V_{in} + 0.3$ | V |
| SW1 to SW6 | | -5 to +25 V | V |
| SW1 to SW6 (< 200 ns) | | -10 to +25 V | V |
| All other Inputs and Outputs | | -0.3 to $V_{in} + 0.3$ | V |
| Storage Temperature Range | T_{STG} | -65 to 150 | °C |
| Operating Ambient Temperature Range | | 0 to 85 | °C |
| ESD Capability, Human Body Model (Note 2) | ESD_{HBM} | 1.5 | kV |
| ESD Capability, Machine Model (Note 2) | ESD_{MM} | 150 | V |
| Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 3) | T_{SLD} | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)
Latchup Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERM/D

Table 3. THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|-----------------|-------|------|
| Thermal Characteristics, QFN, 7 x 7 mm (Note 4) Thermal Resistance, Junction-to-Air (Note 5) | $R_{\theta JA}$ | 27 | °C/W |

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm² (or 1 in²) of 1 oz copper thickness and FR4 PCB substrate.

ELECTRICAL CHARACTERISTICS

$V_{IN} = (5.0 \text{ V})$ FBRTN – GND, for typical values $T_A = 25^\circ\text{C}$, for min/max values $T_A = 0^\circ\text{C}$ to 85°C ; unless otherwise noted. (Notes 6 and 8)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

REFERENCE CURRENT

| | | | | | | |
|------------------------|----------------------------------|------------|------|-----|------|---------------|
| Reference Bias Voltage | | V_{IREF} | 1.75 | 1.8 | 1.85 | V |
| Reference Bias Current | $R_{IREF} = 121 \text{ k}\Omega$ | I_{IREF} | | 15 | | μA |

ERROR AMPLIFIER

| | | | | | | |
|--------------------------------|--|----------------|-------|-----|-------|---------------|
| Output Voltage Range | | V_{COMP} | 0 | | 4.4 | V |
| Accuracy | Relative to nominal DAC output, referenced to FBRTN (Note 8) In startup | V_{FB} | -9.0 | | +9.0 | mV |
| | | $V_{FB(BOOT)}$ | 1.091 | 1.1 | 1.109 | V |
| Load Line Positioning Accuracy | | | -77 | -80 | -83 | mV |
| Load Line Range | | | -350 | | 0 | mV |
| Load Line Attenuation | | | 0 | | 100 | % |
| Differential Non-linearity | | | -1.0 | | +1.0 | LSB |
| Input Bias Current | $I_{FB} = I_{IREF}$ | I_{FB} | 13.3 | 15 | 18.5 | μA |

6. Refer to Absolute Maximum Ratings and Application Information for Safe Operating Area.
7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25^\circ\text{C}$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. Refer to Application Information Note.
9. Values based on design and/or characterization.

NCP4206

ELECTRICAL CHARACTERISTICS

V_{IN} = (5.0 V) FBRTN – GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted. (Notes 6 and 8)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

ERROR AMPLIFIER

| | | | | | | |
|------------------------|--|----------------------|--|-------------------|-----|------|
| Offset Accuracy | VR Offset Register = 111111, VID = 1.0 V VR Offset Register = 011111, VID = 1.0 V | | | -193.75 193.75 | | mV |
| FBRTN Current | | I _{FBRTN} | | 70 | 200 | μA |
| Output Current | FB forced to V _{OUT} -3% | I _{COMP} | | 500 | | μA |
| Gain Bandwidth Product | COMP = FB | GBW _(ERR) | | 20 | | MHz |
| Slew Rate | COMP = FB | | | 25 | | V/μs |
| BOOT Voltage Hold Time | Internal Timer | t _{BOOT} | | 2.0 | | ms |

VID INPUTS

| | | | | | | |
|---|----------------------------------|--|-----|------|-----|----|
| Input Low Voltage Input High Voltage | VID(X) | V _{IL(VID)} V _{IH(VID)} | 0.8 | | 0.3 | V |
| Input Current | | I _{IN(VID)} | | -5.0 | | μA |
| VID Transition Delay Time | VID code change to FB change | | 400 | | | ns |
| No CPU Detection Turn-Off Delay Time | VID code change to PWM going low | | 5.0 | | | μs |

OSCILLATOR

| | | | | | | |
|-----------------------------|---|----------------------|------|-------------------|-----|-----|
| Frequency Range | | f _{OSC} | 0.25 | | 9.0 | MHz |
| Frequency Variation | T _A = 25°C, R _T = 500 kΩ, 4-phase T _A = 25°C, R _T = 250 kΩ, 4-phase T _A = 25°C, R _T = 121 kΩ, 4-phase | f _{PHASE} | 170 | 195 375 750 | 225 | kHz |
| Output Voltage | R _T = 500 kΩ to GND | V _{RT} | 1.9 | 2.0 | 2.1 | V |
| RAMPADJ Output Voltage | RAMPADJ – FB, V _{FB} = 1.0 V, IRAMPADJ = -150 μA | V _{RAMPADJ} | -50 | | +50 | mV |
| RAMPADJ Input Current Range | | I _{RAMPADJ} | 5.0 | | 125 | μA |

CURRENT SENSE AMPLIFIER

| | | | | | | |
|-----------------------------------|-----------------------------|--------------------------|------|-----|------|------|
| Offset Voltage | CSSUM – CSREF (Note 9) | V _{OS(CSA)} | -1.0 | | +1.0 | mV |
| Input Bias Current, CSREF | CSREF = 1.0 V | I _{BIAS(CSREF)} | -20 | | +20 | μA |
| Input Bias Current, CSSUM | CSREF = 1.0 V | I _{BIAS(CSSUM)} | -10 | | +10 | nA |
| Gain Bandwidth Product | CSSUM = CSCOMP | GBW _(CSA) | | 10 | | MHz |
| Slew Rate | C _{CSCOMP} = 10 pF | | | 10 | | V/μs |
| Input Common-Mode Range | CSSUM and CSREF | | 0 | | 3.0 | V |
| Output Voltage Range | | | 0.05 | | 3.0 | V |
| Output Current | | I _{CSCOMP} | | 500 | | μA |
| Current Limit Latchoff Delay Time | Internal Timer | | | 8.0 | | ms |

PSI

| | | | | | | |
|---|--------------------------|--|-----|------|-----|----|
| Input Low Voltage Input High Voltage | | | 0.8 | | 0.3 | V |
| Input Current | | | | -5.0 | | μA |
| Assertion Timing | F _{sw} = 300kHz | | | 3.3 | | μs |
| De-assertion Timing | F _{sw} = 300kHz | | | 825 | | ns |

6. Refer to Absolute Maximum Ratings and Application Information for Safe Operating Area.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

8. Refer to Application Information Note.

9. Values based on design and/or characterization.

NCP4206

ELECTRICAL CHARACTERISTICS

$V_{IN} = (5.0 \text{ V})$ FBRTN – GND, for typical values $T_A = 25^\circ\text{C}$, for min/max values $T_A = 0^\circ\text{C}$ to 85°C ; unless otherwise noted. (Notes 6 and 8)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

IMON

| | | | | | | |
|----------------|---|--|------|--|------|---------------|
| Clamp Voltage | | | 1.0 | | 1.15 | V |
| Accuracy | $10 \times (\text{CSREF} - \text{CSCOMP}) / R_{ILIM}$ | | -3.0 | | 3.0 | % |
| Output Current | | | | | 800 | μA |
| Offset | | | -3.0 | | 3.0 | mV |

CURRENT LIMIT COMPARATOR

| | | | | | | |
|---------------------------------|--|-----------|--|----|--|---------------|
| I_{LIM} Bias Current | $\text{CSREF} - \text{CSCOMP} / R_{ILIM}$, $\text{CSREF} - \text{CSCOMP} = 150 \text{ mV}$, $R_{ILIMC} = 7.5 \text{ k}\Omega$ | I_{LIM} | | 20 | | μA |
| Current Limit Threshold Current | $4/3 \times I_{REF}$ | I_{CL} | | 20 | | μA |

CURRENT BALANCE AMPLIFIER

| | | | | | | |
|-------------------------------|-----------------------------|--------------------|------|-----|------|------------------|
| Common-Mode Range | | $V_{SW(X)CM}$ | -600 | | +200 | mV |
| Input Resistance | $SW(X) = 0 \text{ V}$ | $R_{SW(X)}$ | 14 | 19 | 25 | $\text{k}\Omega$ |
| Input Current | $SW(X) = 0 \text{ V}$ | $I_{SW(X)}$ | 7.0 | 12 | 20 | μA |
| Input Current Matching | $SW(X) = 0 \text{ V}$ | $\Delta I_{SW(X)}$ | -6.0 | | +6.0 | % |
| Phase Balance Adj. Range Low | Phase Bal Registers = 00000 | | | -25 | | % |
| Phase Balance Adj. Range High | Phase Bal Registers = 11111 | | | +25 | | % |

DELAY TIMER

| | | | | | | |
|------------------|---------------------------|--|--|-----|--|----|
| Internal Timer | Delay Time Register = 011 | | | 2.0 | | ms |
| Timer Range Low | Delay Time Register = 000 | | | 0.5 | | ms |
| Timer Range High | Delay Time Register = 111 | | | 4.0 | | ms |

SOFT-START

| | | | | | | |
|------------------|---------------------------------|--|--|-----|--|------|
| Internal Timer | Soft-Start Slope Register = 010 | | | 0.5 | | V/ms |
| Timer Range Low | Soft-Start Slope Register = 000 | | | 0.1 | | V/ms |
| Timer Range High | Soft-Start Slope Register = 111 | | | 1.5 | | V/ms |

ENABLE INPUT

| | | | | | | |
|---|---------------------------------------|------------------------------|-----|------|-----|---------------|
| Input Low Voltage Input High Voltage | | $V_{IL(EN)}$ $V_{IH(EN)}$ | 0.8 | | 0.3 | V |
| Input Current | | $I_{IN(EN)}$ | | -1.0 | | μA |
| Delay Time | $EN > 0.8 \text{ V}$, Internal Delay | $t_{DELAY(EN)}$ | | 2.0 | | ms |

ODN AND OD1 OUTPUTS

| | | | | | | |
|-----------------------------|------------------------------------|-----------------|-----|-----|-----|------------------|
| Output Low Voltage | $I_{OD(SINK)} = -400 \mu\text{A}$ | $V_{OL(ODN/1)}$ | | 160 | 500 | mV |
| Output High Voltage | $I_{OD(SOURCE)} = 400 \mu\text{A}$ | $V_{OL(ODN/1)}$ | 4.0 | 5.0 | | V |
| ODN / OD1 Pulldown Resistor | | | | 60 | | $\text{k}\Omega$ |

POWER-GOOD COMPARATOR

| | | | | | | |
|------------------------------|---------------------------------------|-----------------|------|------|------|----|
| Undervoltage Threshold | Relative to Nominal DAC Output | $V_{PWRGD(UV)}$ | -600 | -500 | -400 | mV |
| Undervoltage Adj. Range Low | PWRGD_LO Register = 000 | | | -500 | | mV |
| Undervoltage Adj. Range High | PWRGD_LO Register = 111 | | | -150 | | mV |
| Overvoltage Threshold | Relative to DAC Output, PWRGD_Hi = 00 | $V_{PWRGD(OV)}$ | 200 | 300 | 400 | mV |

6. Refer to Absolute Maximum Ratings and Application Information for Safe Operating Area.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25^\circ\text{C}$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

8. Refer to Application Information Note.

9. Values based on design and/or characterization.

NCP4206

ELECTRICAL CHARACTERISTICS

$V_{IN} = (5.0\text{ V})$ FBRTN – GND, for typical values $T_A = 25^\circ\text{C}$, for min/max values $T_A = 0^\circ\text{C}$ to 85°C ; unless otherwise noted. (Notes 6 and 8)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

POWER–GOOD COMPARATOR

| | | | | | | |
|---|---|-----------------|-----|-------------------|-----|---------------------------|
| Overvoltage Adjustment Range Low | PWRGD_Hi Register = 11 | | | 150 | | mV |
| Overvoltage Adjustment Range High | PWRGD_Hi Register = 00 | | | 300 | | mV |
| Output Low Voltage | $I_{PWRGD(SINK)} = -4\text{ mA}$ | $V_{OL(PWRGD)}$ | | 150 | 300 | mV |
| Power–Good Delay Time During Soft–Start VID Code Changing VID Code Static | Internal Timer | | 100 | 2.0 250 200 | | ms μs ns |
| Crowbar Trip Point Overvoltage Adjustment Range Low Overvoltage Adjustment Range High | Relative to DAC Output, PWRGD_Hi = 00 PWRGD_Hi Register = 11 PWRGD_Hi Register = 00 | $V_{CROWBAR}$ | 200 | 300 150 300 | 400 | mV |
| Crowbar Reset Point | Relative to FBRTN | | 250 | 300 | 350 | mV |
| Crowbar Delay Time VID Code Changing VID Code Static | Overvoltage to PWM going low | $t_{CROWBAR}$ | 100 | 250 400 | | μs ns |

PWM OUTPUTS

| | | | | | | |
|---------------------|--|---------------|-----|-----|-----|----|
| Output Low Voltage | $I_{PWM(SINK)} = -400\text{ }\mu\text{A}$ | $V_{OL(PWM)}$ | | 160 | 500 | mV |
| Output High Voltage | $I_{PWM(SOURCE)} = 400\text{ }\mu\text{A}$ | $V_{OH(PWM)}$ | 4.0 | 5.0 | | V |

SMBus INTERFACE

| | | | | | | |
|------------------------------------|--------------------------|-------------------|------|-----|-----|---------------|
| Logic High Input Voltage | | $V_{IH(SDA,SCL)}$ | 2.1 | | | V |
| Logic Low Input Voltage | | $V_{IL(SDA,SCL)}$ | | | 0.8 | V |
| Hysteresis | | | | 500 | | mV |
| SDA Output Low Voltage | $I_{SDA} = -6\text{ mA}$ | V_{OL} | | | 0.4 | V |
| Input Current | | V_{IH}, I_{IL} | -1.0 | | 1.0 | μA |
| Input Capacitance | | $C_{SCL, SDA}$ | | 5.0 | | pF |
| Clock Frequency | | f_{SCL} | | | 400 | kHz |
| SCL Falling Edge to SDA Valid Time | | | | | 1.0 | μs |

ALERT, FAULT OUTPUTS

| | | | | | | |
|-----------------------------|--------------------------|----------|--|--|-----|---------------|
| Output Low Voltage | $I_{OUT} = -6\text{ mA}$ | V_{OL} | | | 0.4 | V |
| Output High Leakage Current | $V_{OH} = 5.0\text{ V}$ | V_{OH} | | | 1.0 | μA |

ANALOG / DIGITAL CONVERTER

| | | | | | | |
|----------------------------------|---------------------------------|--|--|-----------|--|-----|
| Total Unadjusted Error (TUE) | | | | ± 1.0 | | % |
| Differential Non–linearity (DNL) | 8 Bits | | | 1.0 | | LSB |
| Conversion Time | Averaging Enabled (32 averages) | | | 80 | | ms |

SUPPLY

| | | | | | | |
|------------------------|--|------------|------|------|------|----|
| V_{CC} | V_{CC} | | 4.70 | 5.25 | 5.75 | V |
| DC Supply Current | $V_{SYSTEM} = 13.2\text{ V}$, $R_{SHUNT} = 340\text{ }\Omega$ | I_{VCC} | | 21 | 26 | mA |
| UVLO Turn–On Current | | | | 6.5 | 11 | mA |
| UVLO Threshold Voltage | V_{CC} Rising | V_{UVLO} | 9.0 | | | V |
| UVLO Turn–Off Voltage | V_{CC} Falling | | | 4.1 | | V |

6. Refer to Absolute Maximum Ratings and Application Information for Safe Operating Area.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25^\circ\text{C}$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

8. Refer to Application Information Note.

9. Values based on design and/or characterization.

NCP4206

ELECTRICAL CHARACTERISTICS

$V_{IN} = (5.0 \text{ V})$ FBRTN – GND, for typical values $T_A = 25^\circ\text{C}$, for min/max values $T_A = 0^\circ\text{C}$ to 85°C ; unless otherwise noted. (Notes 6 and 8)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---------------------|---|-----------|-----|-----|-----|------|
| SUPPLY | | | | | | |
| VCC3 Output Voltage | $I_{VCC3} = 1 \text{ mA}$ | V_{CC3} | 3.0 | 3.3 | 3.6 | V |
| Supply | $V_{SYSTEM} = 12 \text{ V}$, $R_{SHUNT} = 340 \Omega$ (Note 8) | | | | | |

- Refer to Absolute Maximum Ratings and Application Information for Safe Operating Area.
- Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25^\circ\text{C}$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
- Refer to Application Information Note.
- Values based on design and/or characterization.

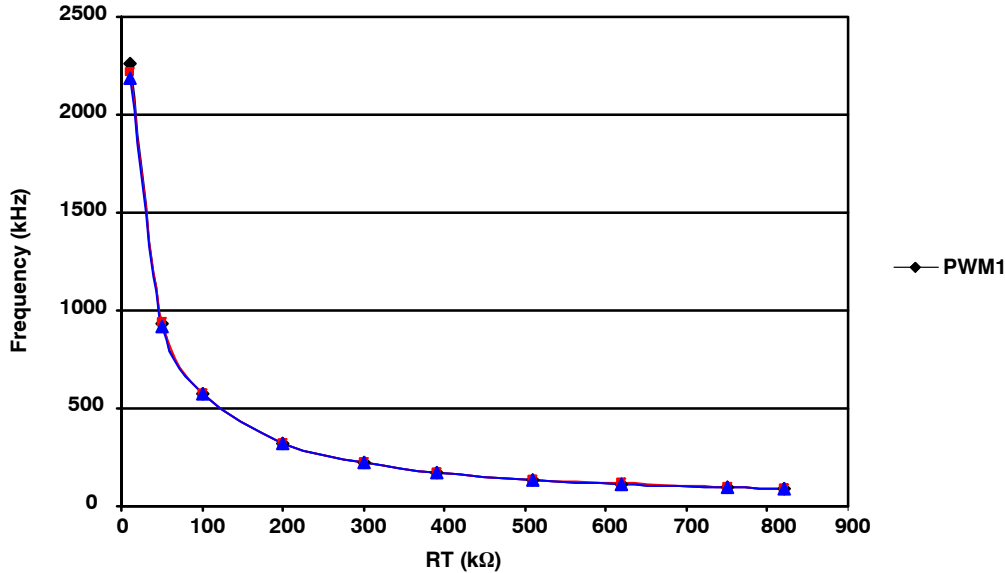


Figure 3. NCP4206 RT vs Frequency

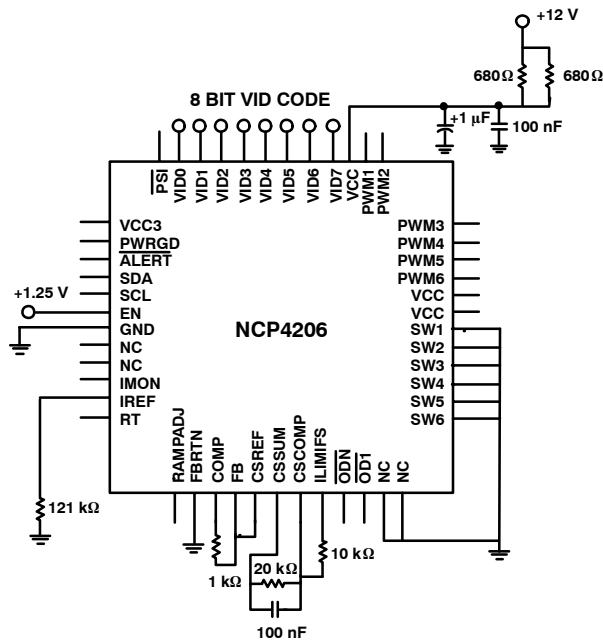


Figure 4. Closed-Loop Output Voltage Accuracy



Once the SS circuit has reached the boot voltage, the boot voltage delay time (TD3) is started. The end of the boot voltage delay time signals the beginning of the second soft start time (TD4). The SS voltage changes from the boot

voltage to the programmed VID DAC voltage (either higher or lower) using 6.25 mV steps.

The soft start slew rate is programmed using Bits <2:0> of the Ton_Rise (0xD5) command code. Table 4 provides the soft start values. Figure 8 shows typical start-up waveforms for the NCP4206.

Table 4. SOFT-START CODES

| Code | Soft-Start (V/msec) |
|------|---------------------|
| 000 | 0.3 |
| 001 | 0.3 |
| 010 | 0.5 = default |
| 011 | 0.7 |
| 100 | 0.9 |
| 101 | 1.1 |
| 110 | 1.3 |
| 111 | 1.5 |

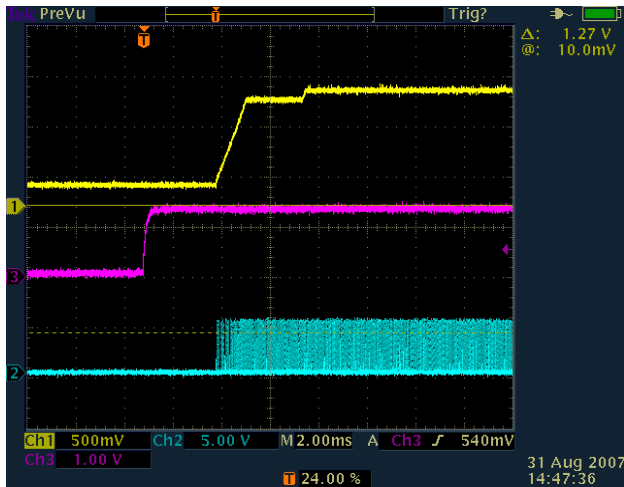


Figure 8. Typical Start-up Waveforms
Channel 1: CSREF
Channel 2: EN
Channel 3: PWM1

Phase Detection

During startup, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the NCP4206 operates as a 6-phase PWM controller.

To operate as a 5-phase controller connect PWM6 to V_{CC} . To operate as a 4-phase controller, connect PWM5 and PWM6 to V_{CC} . To operate as a 3-phase controller, connect PWM4, PWM5 and PWM6 to V_{CC} . To operate as a 2-phase controller connect PWM3, PWM4, PWM5 and PWM6, to V_{CC} . To operate as a 1-phase controller connect PWM2, PWM3, PWM4, PWM5 and PWM6 to V_{CC} .

Prior to soft start, while EN is low, the PWM6, PWM5, PWM4, PWM3 and PWM2 pins sink approximately 100 μ A each. An internal comparator checks each pin's voltage

versus a threshold of 3 V. If the pin is tied to V_{CC} , it is above the threshold. Otherwise, an internal current sink pulls the pin to GND, which is below the threshold. PWM1 is low during the phase detection interval that occurs during the first eight clock cycles of TD2. After this time, if the remaining PWM outputs are not pulled to V_{CC} , the 100 μ A current sink is removed, and they function as normal PWM outputs. If they are pulled to V_{CC} , the 100 μ A current source is removed, and the outputs are put into a high impedance state.

The PWM outputs are logic-level devices intended for driving fast response external gate drivers such as the [ADP3121](#). Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be on at the same time to allow overlapping phases.

Master Clock Frequency

The clock frequency of the NCP4206 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 3. To determine the frequency per phase, the clock is divided by the number of phases in use. If all phases are in use, divide by 6. If 4 phases are in use divide by 4.

Output Voltage Differential Sensing

The NCP4206 combines differential sensing with a high accuracy VID DAC and reference, and a low offset error amplifier. This maintains a worst-case specification of ± 10 mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB pin and FBRTN pin. FB is connected through a resistor, R_B , to the regulation point, usually the remote sense pin of the microprocessor. FBRTN is connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 70 μ A to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

Output Current Sensing

The NCP4206 provides a dedicated current-sense amplifier (CSA) to monitor the total output current for proper voltage positioning versus load current, for the IMON output and for current-limit detection. Sensing the load current at the output gives the total real time current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low-side MOSFET. This amplifier can be configured several ways, depending on the objectives of the system, as follows:

- Output inductor DCR sensing without a thermistor for lowest cost.

- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature.
- Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the average output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors, to the inverting input CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor. This difference signal is used internally to offset the VID DAC for voltage positioning. This different signal can be adjusted between 50% – 150% of the external value using the SMBus Loadline Calibration (0xDE) and Loadline Set (0xDF) commands.

The difference between CSREF and CSCOMP is then used as a differential input for the current-limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors to make it extremely accurate.

The CPU current can also be monitored over the SMBus. The current limit and the loadline can be programmed over SMBus.

Loadline Setting

The Loadline is programmable over the SMBus on the NCP4206. It is programmed using the Loadline Calibration (0xDE) and Loadline Set (0xDF) commands. The Loadline can be adjusted between 0% and 100% of the external R_{CSA} . In this example $R_{CSA} = 1\text{ m}\Omega$. R_O needs to be $0.8\text{ m}\Omega$, therefore programming the Loadline Calibration + Loadline Set register to give a combined percentage of 80% will set the R_O to $0.8\text{ m}\Omega$.

Table 5. LOADLINE COMMANDS

| Code | Loadline (as a percentage of R_{CSA}) |
|--------|--|
| 0 0000 | 0% |
| 0 0001 | 3.226% |
| 1 0000 | 51.6% = default |
| 1 0001 | 53.3% |
| 1 1110 | 96.7% |
| 1 1111 | 100% |

Current Limit Setpoint

The current limit threshold on the NCP4206 is programmed by a resistor between the ILIMFS pin and the CSCOMP pin. The ILIMFS current, I_{ILIMFS} , is compared with an internal current reference of $20\text{ }\mu\text{A}$. If I_{ILIMFS} exceeds $20\text{ }\mu\text{A}$ then the output current has exceeded the limit and the current limit protection is tripped.

$$I_{ILIMFS} = \frac{V_{ILIMFS} - V_{CSCOMP}}{R_{ILIMFS}} \quad (\text{eq. 1})$$

Where $V_{ILIMFS} = V_{CSREF}$

$$I_{ILIMFS} = \frac{V_{CSREF} - V_{CSCOMP}}{R_{ILIMFS}} \quad (\text{eq. 2})$$

$$V_{CSREF} - V_{CSCOMP} = \frac{R_{CS}}{R_{PH}} \times R_L \times I_{LOAD}$$

Where R_L = DCR of the Inductor

Assuming that:

$$\frac{R_{CS}}{R_{PH}} \times R_L = 1\text{ m}\Omega \quad (\text{eq. 3})$$

i.e. the external circuit is set up for a $1\text{ m}\Omega$ Loadline then the R_{ILIMFS} is calculated as follows

$$I_{ILIMFS} = \frac{1\text{ m}\Omega \times I_{LOAD}}{R_{ILIMFS}} \quad (\text{eq. 4})$$

Assuming we want a current limit of 150 A that means that I_{ILIMFS} must equal $20\text{ }\mu\text{A}$ at that load.

$$20\text{ }\mu\text{A} = \frac{1\text{ m}\Omega \times 150\text{ A}}{R_{ILIMFS}} = 7.5\text{ k}\Omega \quad (\text{eq. 5})$$

Solving this equation for R_{LIMITS} we get $7.5\text{ k}\Omega$.

The current limit threshold can be modified from the resistor programmed value by using the SMBus interface using Bits <4:0> of the Current Limit Threshold command (0xE2). The limit is programmable between 50% of the external limit and 146.7% of the external limit. The resolution is 3.3%. Table 6 gives some examples codes:

Table 6. CURRENT LIMIT

| Code | Current Limit (% of External Limit) |
|--------|-------------------------------------|
| 0 0000 | 50% |
| 0 0001 | 53.3% |
| 1 0000 | 100% = default |
| 1 0001 | 103.3% |
| 1 1110 | 143.3% |
| 1 1111 | 146.7% |

Active Impedance Control Mode

For controlling the dynamic output voltage droop as a function of output current, the CSA gain and loadline programming can be scaled to be equal to the droop impedance of the regulator times the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This allows enhanced feed-forward response.

Output Current Monitoring

IMON is an analog output from the NCP4206 representing the total current being delivered to the load. It outputs an accurate current that is directly proportional to the current set by the ILIMFS resistor. The current is then run through a parallel RC connected from the IMON pin to the FBRTN pin to generate an accurately scaled and filtered voltage as per the VR11.1 specification. The size of the resistor is used to set the IMON scaling.

$$I_{\text{IMON}} = 10 \times \frac{R_{\text{CSA}} \times I_{\text{LOAD}}}{R_{\text{ILIMFS}}} \quad (\text{eq. 6})$$

and

$$R_{\text{CSA}} = \frac{\text{DCR}(\text{inductor}) \times \text{RCS}}{R_{\text{PH}}} \quad (\text{eq. 7})$$

If the IMON and the OCP need to be changed based on the TDC of the CPU, then the ILIMFS resistor is the only component that needs to be changed. If the IMON scaling is the only change needed then changing the IMON resistor accomplishes this.

The IMON pin also includes an active clamp to limit the IMON voltage to 1.15 V MAX while maintaining 900 mV MIN full scale accurate reporting.

Current Control Mode and Thermal Balance

The NCP4206 has individual inputs (SW1 to SW6) for each phase that are used for monitoring the current of each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning as described in the Output Current Sensing section.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp.

The balance between the phases can be programmed using the SMBus Phase Bal SW(x) commands (0xE3 to 0xE8). This allows each phase to be adjusted if there is a difference in temperature due to layout and airflow considerations. The phase balance can be adjusted from a default gain of 5 (Bits 4:0 = 10000). The minimum gain programmable is 3.75 (Bits 4:0 = 00000) and the maximum gain is 6.25 (Bits 4:0 = 11111).

Voltage Control Mode

A high gain, high bandwidth, voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed in Table 10. The VID code is set using the VID Input pins or it can be programmed over the SMBus using the VOUT_Command. By default,

the NCP4206 outputs a voltage corresponding to the VID Inputs. To output a voltage following the VOUT_Command the user first needs to program the required VID Code. Then the VID_EN Bits need to be enabled. The following is the sequence

1. Program the required VID Code to the VOUT_Command code (0x21)
2. Set the VID_EN bit (Bit 3) in the VR Config 1A (0xD2) and on the VR Config 1B (0xD3).

This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with Resistor R_B and is used for sensing and controlling the output voltage at this point. A current source (equal to I_{REF}) from the FB pin flowing through R_B is used for setting the no load offset voltage from the VID voltage. The no load voltage is negative with respect to the VID DAC for Intel CPU's. The main loop compensation is incorporated into the feedback network between FB and COMP.

An offset voltage can be added to the control voltage over the serial interface. This is done using Bits <5:0> of the VOUT_CAL (0xDD) Command. The max offset that can be applied is ± 200 mV (even if the sum of the offsets > 200 mV). The LSB size is 6.25 mV. A positive offset is applied when Bit 5 = 0. A negative offset is applied when Bit 5 = 1.

Table 7. OFFSET CODES

| VOUT_CAL CODE | OFFSET VOLTAGE |
|---------------|----------------|
| 0 0001 | +6.25 mV |
| 0 0010 | +12.5 mV |
| 0 0011 | +18.75 mV |

Dynamic VID

The NCP4206 has the ability to dynamically change the VID inputs while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as Dynamic VID (DVID). A DVID can occur under either light or heavy load conditions. The processor signals the controller by changing the VID inputs (or by programming a new VOUT_Command) in a single or multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID bit changes state, the NCP4206 detects the change and ignores the DAC inputs for a minimum of 200 ns. This time prevents a false code due to logic skew while the VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 100 μ s to prevent a false PWRGD or CROWBAR event. Each VID change resets the internal timer.

If a VID off code is detected the NCP4206 will wait for 5 μ sec to ensure that the code is correct before initiating a shutdown of the controller.

The NCP4206 also uses the TON_Transition (0xD6) to limit the DVID slew rates. These can be encountered when the system does a large single VID step for power state changes, thus the DVID slew rate needs to be limited to prevent large inrush currents.

The transition slew rate is programmed using Bits <2:0> of the Ton_Transition (0xD6) command code. Table 8 provides the transition rate values.

Table 8. TRANSITION RATE CODES

| Code | Transition Rate (V/msec) |
|------|--------------------------|
| 000 | 1 |
| 001 | 3 |
| 010 | 5 = default |
| 011 | 7 |
| 100 | 9 |
| 101 | 11 |
| 110 | 13 |
| 111 | 15 |

Enhanced transient Mode

The NCP4206 incorporates enhanced transient response for both load step up and load release. For load step up it senses the output of the error amp to determine if a load step up has occurred and then sequences on the appropriate number of phases to ramp up the output current.

For load release, it also senses the output of the error amp and uses the load release information to trigger the TRDET pin, which is then used to adjust the error amp feedback for optimal positioning. This is especially important during high frequency load steps.

Additional information is used during load transients to ensure proper sequencing and balancing of phases during high frequency load steps as well as minimizing the stress on components such as the input filter and MOSFET's.

Current Reference

The IREF pin is used to set an internal current reference. This reference current sets I_{FB} . A resistor to ground programs the current based on the 1.8 V output.

$$I_{REF} = \frac{1.8 \text{ V}}{R_{IREF}} \quad (\text{eq. 8})$$

Typically, R_{IREF} is set to 121 k Ω to program $I_{REF} = 15 \mu\text{A}$.

Internal Delay Timer

The delay times for the start up timing sequence are set by an internal timer. The default time is 2 msec which can be changed through the SMBus interface. This timer is used for multiple delay timings (TD1, TD3, and TD5) during the start-up sequence. Also, it is used for timing the current limit latch off as explained in the CURRENT LIMIT section. The current limit timer is set to 4 times the delay timer.

The delay timer is programmed using Bits <2:0> of the Ton Delay command (0xD4). The delay can be programmed between 0.5 msec and 4 msec. Table 9 provides the programmable delay values

Table 9. DELAY CODES

| Code | Delay (msec) |
|------|--------------|
| 000 | 0.5 |
| 001 | 1 |
| 010 | 1.5 |
| 011 | 2 = default |
| 100 | 2.5 |
| 101 | 3 |
| 110 | 3.5 |
| 111 | 4 |

Current Limit, Short Circuit and Latch-off Protection

The NCP4206 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMFS pin to CSCOMP, and can be adjusted using the SMBus interface.

The current limit threshold can be modified from the resistor programmed value by using the SMBus interface using Bits <4:0> of the Current Limit Threshold command (0xE2). The limit is programmable between 50% of the external limit and 146.7% of the external limit. The resolution is 3.3%. The current limit threshold can be modified from the resistor programmed value by using the serial interface.

If the limit is reached and TD5 has completed, an internal latch-off delay time will start, and the controller will shut down if the fault is not removed. This delay is four times longer than the delay time during the start-up sequence. The current limit delay time only starts after the TD5 has completed. If there is a current limit during start-up, the NCP4206 will go through TD1 to TD5, and then start the latch-off time. As the controller continues to cycle the phases during the latch-off delay time, if the short is removed before the timer is complete, the controller can return to normal operation.

The latch-off function can be reset by either removing and reapplying the supply voltage to the NCP4206, or by toggling the EN pin low for a short time.

The OCP latch-off function can be disabled by using the SMBus interface. Setting the CLIM_EN bit (bit 1) of the VR Config 1A (0xD2) and VR Config 1B (0xD3) registers to 0 disables the current limit latch off function. The NCP4206 can continue to operate in current limit indefinitely.

During start-up when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit limits controls of the internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low-side MOSFETs through the

current balance circuitry. Typical over-current latch-off waveforms are shown in Figure 9.

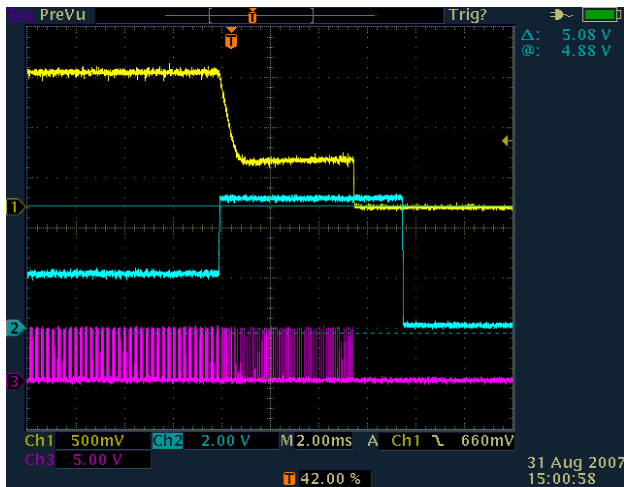


Figure 9. Over Current Latch-off Waveforms
Channel 1: CSREF,
Channel 2: COMP, Channel 3: PWM1

An inherent per phase current limit protects individual phases if one or more phases stops functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

Power Good Monitoring

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified in the specifications above based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if the VID DAC inputs are in no CPU mode, or whenever the EN pin is pulled low. PWRGD is blanked during a DVID event for a period of 100 μ s to prevent false signals during the time the output is changing.

The PWRGD circuitry also incorporates an initial turn-on delay time (TD5). Prior to the SS voltage reaching the programmed VID DAC voltage and the PWRGD masking time finishing, the PWRGD pin is held low. Once the SS circuit reaches the programmed DAC voltage, the internal timer operates.

The value for the PWRGD high limit and low limit can be programmed using the serial interface.

Power State Indicator

The $\overline{\text{PSI}}$ pin is an input used to determine the operating state of the load. If this input is pulled low, the load is in a low power state and the controller asserts the $\overline{\text{ODN}}$ pin low, which can be used to disable phases and maintain better efficiency at lighter loads.

The sequencing into and out of low power operation is maintained to minimize output deviations as well as

providing full power load transients immediately after exiting a low power state.

Output Crowbar

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 300 mV.

The value for the crowbar limit follows the programmable PWRGD high limit.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high-side MOSFET, this action current-limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

Output Enable and UVLO

For the NCP4206 to begin switching, the input supply current to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.8 V threshold. This initiates a system start-up sequence. If either UVLO or EN is less than their respective thresholds, the NCP4206 is disabled. This holds the PWM outputs at ground and forces PWRGD, $\overline{\text{ODN}}$ and $\overline{\text{ODI}}$ signals low.

In the application circuit (see Figure 2), the $\overline{\text{ODI}}$ pin should be connected to the $\overline{\text{OD}}$ inputs of the external drivers for the phases that are always on. The $\overline{\text{ODN}}$ pin should be connected to the $\overline{\text{OD}}$ inputs of the external drivers on the phases that are shut down during low power operation. Grounding the driver $\overline{\text{OD}}$ inputs disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

SMBus Interface

Control of the NCP4206 is carried out using the SMBus Interface. The physical protocol for SMBus closely matches that of I²C. The NCP4206 SMBus address is 0x20 (010 0000), with the R/W bit set to 0. This gives an 8 bit address of 0x40.

Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high might be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

1. When all data bytes have been read or written, stop conditions are established. In write mode, the

master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse; this is known as No Acknowledge. The master takes the data line low during the low period before the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the NCP4206, write operations contain one, two or three bytes, and read operations contain one or two bytes. The command code or register address determines the number of bytes to be read or written. See the register map for more information.

To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed (i.e. command code), and then data can be written to that register or read from it.

The first byte of a read or write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write byte operation is shown in Figure 11. The device address is sent over the bus, and then R/\overline{W} is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

2. The read byte operation is shown in Figure 12.

First the command code needs to be written to the NCP4206 so that the required data is sent back.

This is done by performing a write to the NCP4206 as before, but only the data byte containing the register address is sent, because no data is written to the register. A repeated start is then issued and a read operation is then performed consisting of the serial bus address; R/\overline{W} bit set to 1, followed by the data byte read from the data register.

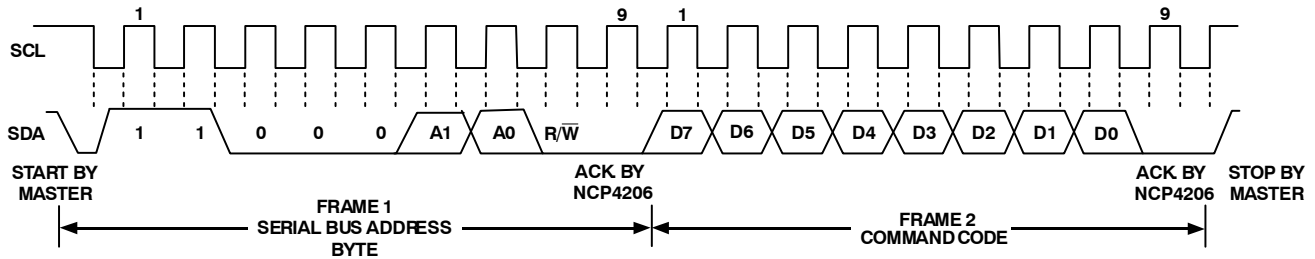


Figure 10. Send Byte

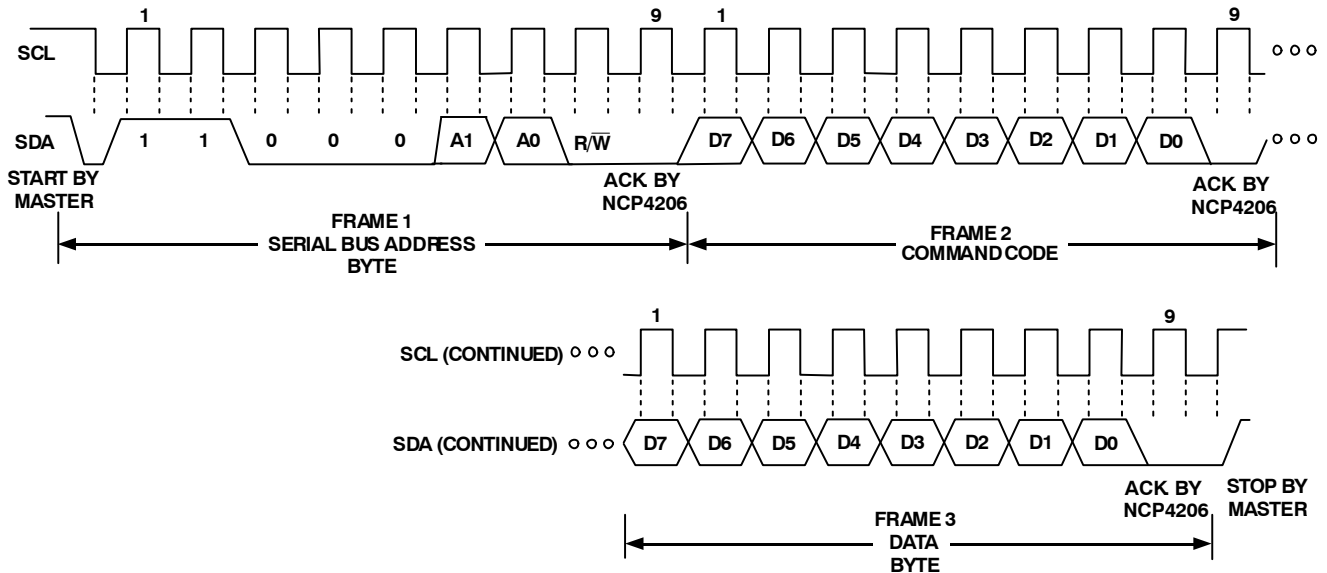


Figure 11. Write Byte

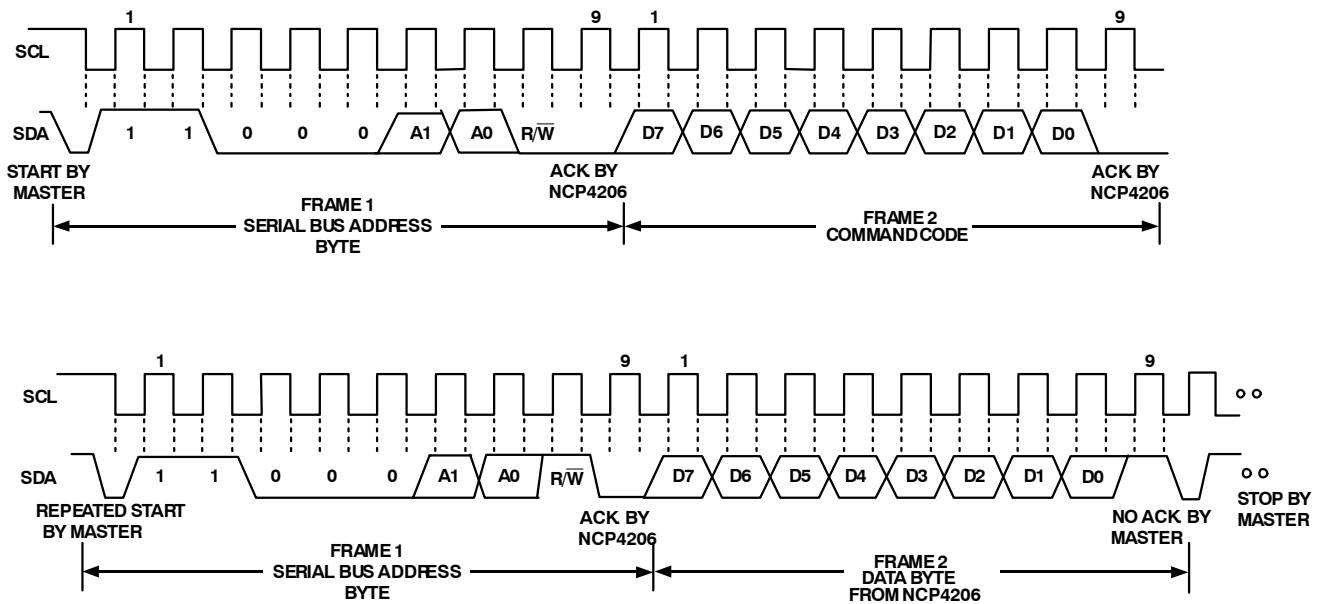


Figure 12. Read Byte

1. It is not possible to read or write a data byte from a data register without first writing to the address pointer register, even if the address pointer register is already at the correct value.
2. In addition to supporting the send byte, the NCP4206 also supports the read byte, write byte, read word and write word protocols. (See *System Management Bus Specifications Rev. 2.0* and the *SMBus Specification Rev 1.1 Part I and Part II* for more information.)

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the NCP4206 are discussed in this section. The following abbreviations are used in the diagrams:

S – START
P – STOP
R – READ
W – WRITE
A – ACKNOWLEDGE
 \bar{A} – NO ACKNOWLEDGE

The NCP4206 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the NCP4206, the send byte protocol is used to clear faults. This operation is shown in Figure 13.

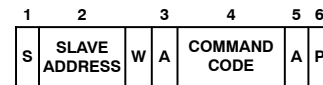


Figure 13. Send Byte Command

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows: The master device asserts a start condition on SDA.

1. The master sends the 7-bit slave address followed by the write bit (low).
2. The addressed slave device asserts ACK on SDA.
3. The master sends a command code.
4. The slave asserts ACK on SDA.
5. The master sends a data byte.
6. The slave asserts ACK on SDA.
7. The master asserts a stop condition on SDA and the transaction ends.

The byte write operation is shown Figure 14.

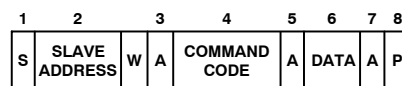


Figure 14. Single Byte Write to a Register

Write Word

In this operation, the master device sends a command byte and two data bytes to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends the first data byte.
7. The slave asserts ACK on SDA.
8. The master sends the second data byte.
9. The slave asserts ACK on SDA.
10. The master asserts a stop condition on SDA and the transaction ends.

The word write operation is shown in Figure 15.

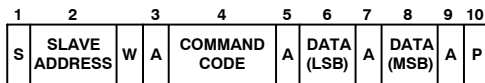


Figure 15. Single Word Write to a Register

Block Write

In this operation, the master device sends a command byte and a byte count followed by the stated number of data bytes to the slave device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code
5. The slave asserts ACK on SDA
6. The master sends the byte count N
7. The slave asserts ACK on SDA
8. The master sends the first data byte
9. The slave asserts ACK on SDA
10. The master sends the second data byte.
11. The slave asserts ACK on SDA
12. The master sends the remainder of the data bytes
13. The slave asserts an ACK on SDA after each data byte.
14. After the last data byte the master asserts a STOP condition on SDA

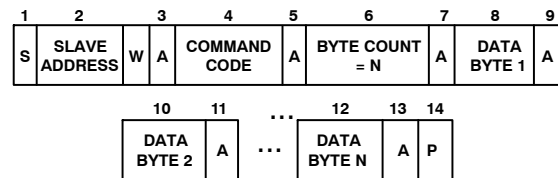


Figure 16. Block Write to a Register

Read Operations

The NCP4206 uses the following SMBus read protocols.

Read Byte

In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a repeated start condition on SDA
7. The master sends the 7 bit slave address followed by the read bit (high)
8. The slave asserts ACK on SDA
9. The slave sends the Data Byte
10. The master asserts NO ACK on SDA.
11. The master asserts a stop condition on SDA and the transaction ends.

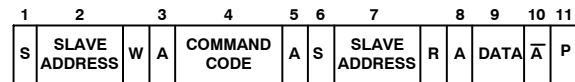


Figure 17. Single Byte Read from a Register

Read Word

In this operation, the master device receives two data bytes from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.

4. The master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA
7. The master sends the 7 bit slave address followed by the read bit (high)
8. The slave asserts ACK on SDA
9. The slave sends the first Data Byte (low Data Byte)
10. The master asserts ACK on SDA.
11. The slave sends the second Data Byte (high Data Byte)
12. The masters asserts a No ACK on SDA
13. The master asserts a stop condition on SDA and the transaction ends.

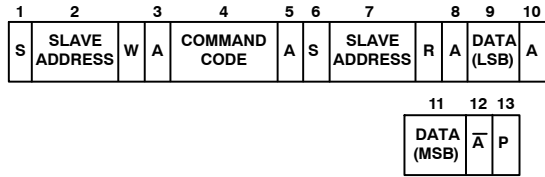


Figure 18. Word Read from a Command Coder

In this operation, the master device sends a command byte, the slave sends a byte count followed by the stated number of data bytes to the master device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a REPEATED START condition on SDA

5. The master sends the 7-bit slave address followed by the read bit (high).
6. The slave asserts ACK on SDA
7. The slave sends the byte count N
8. The master asserts ACK on SDA
9. The slave sends the first data byte
10. The master asserts ACK on SDA
11. The slave sends the remainder of the data bytes, the master asserts an ACK on SDA after each data byte.
12. After the last data byte the master asserts a No ACK on SDA.
13. The master asserts a STOP condition on SDA

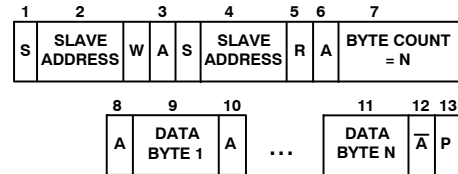


Figure 19. Block Write to a Command Coder

SMBus Timeout

The NCP4206 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the NCP4206 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Configuration Register 1 (0xD1)

Bit 3 SMB_TO_EN = 1; SMBus timeout enabled.

Table 10. VR11 AND VR10.X VID CODES FOR THE NCP4206

| OUTPUT | VR11 DAC CODES | | | | | | | |
|---------|----------------|------|------|------|------|------|------|------|
| | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
| OFF | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| OFF | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1.60000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1.59375 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1.58750 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1.58125 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1.57500 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1.56875 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1.56250 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1.55625 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1.55000 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1.54375 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1.53750 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

NCP4206

Table 10. VR11 AND VR10.X VID CODES FOR THE NCP4206

| OUTPUT | VR11 DAC CODES | | | | | | | |
|---------|----------------|------|------|------|------|------|------|------|
| | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
| 1.53125 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1.52500 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1.51875 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1.51250 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1.50625 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1.50000 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1.49375 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1.48750 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1.48125 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1.47500 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1.46875 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1.46250 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1.45625 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1.45000 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1.44375 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1.43750 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1.43125 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1.42500 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1.41875 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1.41250 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1.40625 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1.40000 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1.39375 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1.38750 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1.38125 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1.37500 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1.36875 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1.36250 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1.35625 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1.35000 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1.34375 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1.33750 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1.33125 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1.32500 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1.31875 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1.31250 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1.30625 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1.30000 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1.29375 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1.28750 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1.28125 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |

NCP4206

Table 10. VR11 AND VR10.X VID CODES FOR THE NCP4206

| OUTPUT | VR11 DAC CODES | | | | | | | |
|---------|----------------|------|------|------|------|------|------|------|
| | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
| 1.27500 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1.26875 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1.26250 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1.25625 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1.25000 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1.24375 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1.23750 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1.23125 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1.22500 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1.21875 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1.21250 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1.20625 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1.20000 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1.19375 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1.18750 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1.18125 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1.17500 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1.16875 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1.16250 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1.15625 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1.15000 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1.14375 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1.13750 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1.13125 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1.12500 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1.11875 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1.11250 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1.10625 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1.10000 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1.09375 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1.08750 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1.08125 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1.07500 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1.06875 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1.06250 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1.05625 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1.05000 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1.04375 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1.03750 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1.03125 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1.02500 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |

NCP4206

Table 10. VR11 AND VR10.X VID CODES FOR THE NCP4206

| OUTPUT | VR11 DAC CODES | | | | | | | |
|---------|----------------|------|------|------|------|------|------|------|
| | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
| 1.01875 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1.01250 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1.00625 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1.00000 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0.99375 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0.98750 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0.98125 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0.97500 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0.96875 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0.96250 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0.95625 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0.95000 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0.94375 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0.93750 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0.93125 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0.92500 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0.91875 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0.91250 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0.90625 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0.90000 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0.89375 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0.88750 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0.88125 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0.87500 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0.86875 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0.86250 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0.85625 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0.85000 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0.84375 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0.83750 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0.83125 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0.82500 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0.81875 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0.81250 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0.80625 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0.80000 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0.79375 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0.78750 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0.78125 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0.77500 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0.76875 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

NCP4206

Table 10. VR11 AND VR10.X VID CODES FOR THE NCP4206

| OUTPUT | VR11 DAC CODES | | | | | | | |
|---------|----------------|------|------|------|------|------|------|------|
| | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
| 0.76250 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0.75625 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0.75000 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0.74375 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0.73750 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0.73125 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0.72500 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0.71875 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0.71250 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0.70625 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0.70000 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0.69375 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0.68750 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0.68125 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0.67500 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0.66875 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0.66250 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0.65625 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0.65000 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0.64375 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0.63750 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0.63125 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0.62500 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0.61875 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0.61250 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0.60625 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0.60000 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0.59375 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0.58750 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0.58125 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0.57500 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0.56875 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0.56250 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0.55625 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0.55000 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0.54375 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0.53750 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0.53125 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0.52500 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0.51875 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0.51250 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

NCP4206

Table 10. VR11 AND VR10.X VID CODES FOR THE NCP4206

| OUTPUT | VR11 DAC CODES | | | | | | | |
|---------|----------------|------|------|------|------|------|------|------|
| | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
| 0.50625 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0.50000 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| OFF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| OFF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 11. SMBus COMMANDS FOR THE NCP4206

| Cmd Code | R/W | Default | Description | # Bytes | Comment | | |
|----------|-----|---------|---------------|---------|---|---|---|
| 0x01 | R/W | 0x80 | Operation | 1 | 00xx xxxx – Immediate Off 01xx xxxx – Soft Off 1000 xxxx – On (slew rate set by soft-start) – Default 1001 01xx – Margin Low (Ignore Fault) 1001 10xx – Margin Low (Act on Fault) 1010 01xx – Margin High (Ignore Fault) 1010 10xx – Margin High (Act on Fault) | | |
| 0x02 | R/W | 0x17 | ON_OFF_Config | 1 | Configures how the controller is turned on and off. | | |
| | | | | | Bit | Default | Comment |
| | | | | | 7:5 | 000 | Reserved for Future Use |
| | | | | | 4 | 1 | This bit is read only. Switching starts when commanded by the Control Pin and the Operation Command, as set in Bits 3:0. |
| | | | | | 3 | 0 | 0: Unit ignores OPERATION commands over the SMBus 1: Unit responds to OPERATION command, powerup may also depend upon Control input, as described in Bit 2 |
| | | | | | 2 | 1 | 0: Unit ignores EN pin 1: Unit responds EN pin, powerup may also depend upon the Operation Register, as described for Bit 3 |
| | | | | | 1 | 1 | Control Pin polarity 0 = Active Low 1 = Active High |
| | | | | | 0 | 1 | This bit is read only. 1: means that when the controller is disabled it will either immediately turn off or soft off (as set in the Operation Command) |
| 0x03 | W | NA | Clear_Faults | 0 | Writing any value to this command code will clear all Status Bits immediately. The SMBus ALERT is deasserted on this command. If the fault is still present the fault bit shall immediately be asserted again. | | |
| 0x10 | R/W | 0x00 | Write Protect | 1 | The Write_Protect command is used to control writing to the SMBus device. There is also a lock bit in the Manufacture Specific Registers that once set will disable writes to all commands until the power to the NCP4206 is cycled. | | |
| | | | | | Data Byte | Comment | |
| | | | | | 1000 0000 | Disables all writes except to the Write_Protect Command | |
| | | | | | 0100 0000 | Disables all writes except to the Write_Protect and Operation Commands | |
| | | | | | 0010 0000 | Disables all writes except to the Write_Protect, Operation, ON_OFF_Config and VOUT_COMMAND Commands | |
| | | | | | 0000 0000 | Enables writes to all commands | |
| | | | | | 0001 0000 | Disables all writes except to WRITE_PROTECT, PAGE and all MFR-SPECIFIC Commands | |

NCP4206

Table 11. SMBus COMMANDS FOR THE NCP4206

| Cmd Code | R/W | Default | Description | # Bytes | Comment | | |
|----------|-----|---------|--------------------|---------|--|-------------------|---|
| 0x19 | R | 0xB0 | Capability | 1 | This command allows the host to get some information on the SMBus device. | | |
| | | | | | Bit | Default | Comment |
| | | | | | 7 | 1 | PEC (Packet Error Checking) is supported |
| | | | | | 6:5 | 01 | Max supported bus speed is 400 kHz |
| | | | | | 4 | 1 | NCP4206 has an SMBus ALERT pin and ARA is supported |
| | | | | | 3:0 | 000 | Reserved for future use |
| 0x20 | R | 0x20 | VOUT_MODE | 1 | The NCP4206 supports VID mode for programming the output voltage. | | |
| 0x21 | R/W | 0x00 | VOUT_COMMAND | 2 | Sets the output voltage using VID. | | |
| 0x25 | R/W | 0x0020 | VOUT_MARGIN_HIGH | 2 | Sets the output voltage when operation command is set to Margin High. Programmed in VID Mode. | | |
| 0x26 | R/W | 0x00B2 | VOUT_MARGIN_LOW | 2 | Sets the output voltage when operation command is set to Margin Low. Programmed in VID Mode. | | |
| 0x38 | R/W | 0x0001 | IOUT_CAL_GAIN | 2 | Sets the ratio of voltage sensed to current output. Scale is Linear and is expressed in $1/\Omega$ | | |
| 0x39 | R/W | 0x0000 | IOUT_CAL_OFFSET | 2 | This offset is used to null out any offsets in the output current sensing circuitry. Units are Amps | | |
| 0x4A | R/W | 0x0064 | IOUT_OC_WARN_LIMIT | 2 | This sets the high current limit. Once this limit is exceeded IOUT_OC_WARN_LIMIT bit is set in the Status_IOUT register and an ALERT is generated. This limit is set in Amps. | | |
| 0x6A | R/W | 0x012C | POUT_OP_WARN LIMIT | 2 | This sets the output power over power warn limit. Once exceeded Bit 0 of the Status_IOUT Command gets set and the ALERT output gets asserted (if not masked) | | |
| 0x78 | R | 0x00 | STATUS BYTE | 1 | Bit | Name | Description |
| | | | | | 7 | BUSY | A fault was declared because the NCP4206 was busy and unable to respond. |
| | | | | | 6 | OFF | This bit is set whenever the NCP4206 is not switching. |
| | | | | | 5 | VOUT_OV | This bit gets set whenever the NCP4206 goes into OVP mode. |
| | | | | | 4 | IOUT_OC | This bit gets set whenever the NCP4206 latches off due to an overcurrent event. |
| | | | | | 3 | VIN_UV | Not supported. |
| | | | | | 2 | TEMP | Not supported. |
| | | | | | 1 | CML | A Communications, memory or logic fault has occurred. |
| | | | | | 0 | None of the Above | A fault has occurred which is not one of the above. |

NCP4206

Table 11. SMBus COMMANDS FOR THE NCP4206

| Cmd Code | R/W | Default | Description | # Bytes | Comment | | | |
|----------|-----|---------|-------------|---------|---------|----------------------------|---|--|
| 0x79 | R | 0x0000 | STATUS WORD | 2 | Byte | Bit | Name | Description |
| | | | | | Low | 7 | Res | Reserved for future use. |
| | | | | | Low | 6 | OFF | This bit is set whenever the NCP4206 is not switching. |
| | | | | | Low | 5 | VOUT_OV | This bit gets set whenever the NCP4206 goes into OVP mode. |
| | | | | | Low | 4 | IOUT_OC | This bit gets set whenever the NCP4206 latches off due to an overcurrent event. |
| | | | | | Low | 3 | Res | Reserved for future use. |
| | | | | | Low | 2 | TEMP | Not supported. |
| | | | | | Low | 1 | CML | A Communications, memory or logic fault has occurred. |
| | | | | | High | 0 | None of the Above | A fault has occurred which is not one of the above. |
| | | | | | High | 7 | VOUT | This bit gets set whenever the measured output voltage goes outside its power good limits or an OVP event has taken place, i.e. any bit in Status VOUT is set. |
| 0x79 | R | 0x0000 | STATUS WORD | 2 | Byte | Bit | Name | Description |
| | | | | | High | 6 | IOUT/P _{OUT} | This bit gets set whenever the measured output current or power exceeds its warning limit or goes into OCP. i.e. any bit in Status I _{OUT} is set. |
| | | | | | High | 5 | INPUT | Not supported. |
| | | | | | High | 4 | MFR | A manufacturer specific warning or fault has occurred. |
| | | | | | High | 3 | POWER _{GOOD} | The Power Good signal is deasserted. Same as PowerGood in General Status. |
| | | | | | High | 2 | Res | Reserved for future use. |
| | | | | | High | 1 | OTHER | A Status bit in Status Other is asserted. |
| | | | | | High | 0 | Res | Reserved for future use. |
| 0x7A | R | 0x00 | STATUS VOUT | 1 | Bit | Name | Description | |
| | | | | | 7 | Res | Not supported. | |
| | | | | | 6 | VOUT_OVER VOLTAGE WARNING | This bit gets set whenever the measured output voltage goes above its powergood limit. | |
| | | | | | 5 | VOUT_UNDER VOLTAGE WARNING | This bit gets set whenever the measured output voltage goes below its powergood limit. | |
| | | | | | 4 | Res | Reserved for future use. | |
| | | | | | 3 | VOUT_MAX Warning | Not supported, Can't program an output greater than MAX VID as there are no bits to program it. | |
| | | | | | 2 | Res | Not supported. | |
| | | | | | 1 | Res | Not supported. | |
| | | | | | 0 | Res | Not supported. | |

NCP4206

Table 11. SMBus COMMANDS FOR THE NCP4206

| Cmd Code | R/W | Default | Description | # Bytes | Comment | | |
|----------|-----|---------|--------------|---------|--|---|--|
| 0x7B | R | 0x00 | STATUS IOUT | 1 | Bit | Name | Description |
| | | | | | 7 | I _{OUT} Overcurrent | This bit gets set if the NCP4206 latches off due to an OCP Event. |
| | | | | | 6 | Res | Reserved for future use. |
| | | | | | 5 | I _{OUT} Overcurrent Warning | This bit gets set if I _{OUT} exceeds its programmed high warning limit. |
| | | | | | 4 | Res | Reserved for future use. |
| | | | | | 3 | Res | Reserved for future use. |
| | | | | | 2 | Res | Reserved for future use. |
| | | | | | 1 | Res | Not supported. |
| | | | | | 0 | P _{OUT} Over Power Warning Fault | This bit gets set if the measured P _{OUT} exceeds the Warn Limit. |
| 0x7E | R | 0x00 | STATUS CML | 1 | Bit | Desc. | Name |
| | | | | | 7 | Supported | Invalid or Unsupported Command Received |
| | | | | | 6 | Supported | Invalid or Unsupported Data Received |
| | | | | | 5 | Supported | PEC Failed |
| | | | | | 4 | Not supported | Memory Fault Detected |
| | | | | | 3 | Not supported | Processor Fault Detected |
| | | | | | 2 | Supported | Reserved |
| | | | | | 1 | Supported | A communication fault other than the ones listed has occurred |
| 0x80 | R | 0x00 | STATUS_ALERT | 1 | Bit | Name | Description |
| | | | | | 7 | Res | Reserved for future use. |
| | | | | | 6 | Res | Reserved for future use. |
| | | | | | 5 | Res | Reserved for future use. |
| | | | | | 4 | Res | Reserved for future use. |
| | | | | | 3 | Res | Reserved for future use. |
| | | | | | 2 | V _{MON} WARN | Gets asserted when V _{MON} exceeds its programmed WARN limits. |
| | | | | | 1 | Res | Reserved for future use. |
| 0x8B | R | 0x00 | READ_VOUT | 2 | 0 | Res | Reserved for future use. |
| | | | | | 1 | Res | Reserved for future use. |
| | | | | | 2 | Res | Reserved for future use. |
| | | | | | 3 | Res | Reserved for future use. |
| | | | | | 4 | Res | Reserved for future use. |
| | | | | | 5 | Res | Reserved for future use. |
| | | | | | 6 | Res | Reserved for future use. |
| | | | | | 7 | Res | Reserved for future use. |
| 0x8B | R | 0x00 | READ_VOUT | 2 | Readback output voltage. Voltage is read back in VID Mode | | |
| 0x8C | R | 0x00 | READ_IOUT | 2 | Readback output current. Current is read back in Linear Mode (Amps). | | |
| 0x96 | R | 0x00 | READ_POUT | 2 | Readback Output Power, read back in Linear Mode in W's. | | |
| 0x99 | R | 0x41 | MFR_ID | 1 | | | |
| 0x9A | R | 0x0208 | MFR_MODEL | 2 | | | |
| 0x9B | R | 0x03 | MFR_REVISION | 1 | | | |

NCP4206

Table 12. MANUFACTURER SPECIFIC COMMAND CODES FOR THE NCP4206

| Cmd Code | R/W | Default | Description | # Bytes | Comment | | |
|----------|-----|---------|-------------|---------|---------|----------------|---|
| 0xDO | R/W | 0x00 | Lock/Reset | 1 | Bit | Name | Description |
| | | | | | 1 | Reset | Resets all registers to their POR Value. Has no effect if Lock bit is set. |
| | | | | | 0 | Lock | Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only and cannot be modified until the NCP4206 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable). |
| 0xD1 | R/W | 0x03 | Mfr Config | 1 | Bit | Name | Description |
| | | | | | 7:6 | PSI | These bits sets the number of phases turned on during PSI. 00 = CL set for 1 Phase (default) 01 = CL set for 2 Phases 10 = CL set for 3 Phases 11 = CL set for 1 Phase |
| | | | | | 5 | Res | Reserved for future use. |
| | | | | | 4 | ALERT Mode | 1 = Comparator Mode. 0 = ALERT Mode. |
| | | | | | 3 | SMB_TO_EN | SMBus Timeout Enable. When the SMB_TO_EN bit is set to 1, the SMBus Timeout feature is enabled. In this state if, at any point during an SMBus transaction involving the NCP4206, activity ceases for more than 35 ms, the NCP4206 assumes the bus is locked and releases the bus. This allows the NCP4206 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable.) |
| | | | | | 2 | Res | Reserved for future use. |
| | | | | | 1 | ALERT_EN | Enable the ALERT pin. |
| | | | | | 0 | ENABLE_MONITOR | When the ENABLE_MONITOR bit is set to 1, the NCP4206 starts conversions with the ADC and monitors the voltages and temperatures. |

Table 12. MANUFACTURER SPECIFIC COMMAND CODES FOR THE NCP4206

| Cmd Code | R/W | Default | Description | # Bytes | Comment | | |
|----------|-----|---------|--------------------------|---------|--|-------------------|--|
| 0xD2 | R/W | 0x72 | VR Config. 1A | 1 | Bit | Name | Description |
| | | | | | 6:4 | Phase Enable Bits | 000 = Phase 1 001 = Phase 2 010 = Phase 3 011 = Phase 4 100 = Phase 5 101 = Phase 6 |
| | | | | | 3 | VID_EN | When the VID_EN bit is set to 1, the VID code in the VOUT_COMMAND register sets the output voltage. When VID_EN is set to 0, the output voltage follows the VID input pins. |
| | | | | | 2 | LOOP_EN | When the LOOP_EN bit is set to 1 in both registers, the control loop test function is enabled. This allows measurement of the control loop AC gain and phase response with appropriate instrumentation. The control loop signal insertion pin is I _{MON} . The control loop output pin is COMP. |
| | | | | | 1 | CLIM_EN | When CLIM_EN is set to 1, the current limit time out latchoff functions normally. When this bit is set to 0 in both registers, the current limit latchoff is disabled. In this state, the part can be in current limit indefinitely. |
| | | | | | 0 | Res | Reserved for future use. |
| 0xD3 | R/W | 0x72 | VR Config. 1B | 1 | This register is for security reasons. It has the same format as register 0xD2. Bits need to be set in both registers for the function to take effect. | | |
| 0xD4 | R/W | 0x03 | Ton Delay | 1 | | | |
| 0xD5 | R/W | 0x02 | Ton Rise | 1 | | | |
| 0xD6 | R/W | 0x01 | Ton Transition | 1 | | | |
| 0xD7 | R | 0x00 | V _{MON} Voltage | 2 | This is a 16 bit value that reports back the voltage measured between FB and FBRTN | | |
| 0xD8 | R | 0x00 | EN/VTT Voltage | 2 | This is a 16 bit value that reports back the voltage on the VTT Pin. | | |
| 0xDD | R/W | 0x00 | VOUT_CAL | 1 | Offset Command Code for V _{OUT} , max ±200 mV | | |
| 0xDE | R/W | 0x10 | Loadline Calibration | 1 | <p>This value sets the internal loadline attenuation DAC calibration value. The maximum loadline is controlled externally by setting the gain of the current sense amplifier as explained in the applications section. This maximum loadline can then be adjusted from 100% to 0% in 30 steps. Each LSB represents a 3.226% change in the load line.</p> <p>00000 = No Load Line 10000 = 51.6% of external load line 11111 = 100% of external Loadline</p> | | |
| 0xDF | R/W | 0x00 | Loadline Set | 1 | <p>This value sets the internal loadline attenuation DAC value. The maximum loadline is controlled externally by setting the gain of the current sense amplifier as explained in the applications section. This maximum loadline can then be adjusted from 100% to 0% in 30 steps. Each LSB represents a 3.226% change in the load line.</p> <p>00000 = No Load Line 10000 = 51.6% of external load line 11111 = 100% of external load Line</p> | | |
| 0xE0 | R/W | 0x00 | PWRGD Hi Threshold | 1 | <p>This value sets the PWRGD Hi Threshold and the CROWBAR Threshold:</p> <p>Code = 00, PWRGD HI = 300 mV (default) Code = 01, PWRGD HI = 250 mV Code = 10, PWRGD HI = 200 mV Code = 11, PWRGD HI = 150 mV</p> | | |

NCP4206

Table 12. MANUFACTURER SPECIFIC COMMAND CODES FOR THE NCP4206

| Cmd Code | R/W | Default | Description | # Bytes | Comment |
|----------|-----|---------|-------------------------|---------|---|
| 0xE1 | R/W | 0x00 | PWRGD Lo Threshold | 1 | This value sets the PWRGD Lo Threshold: Code = 000, PWRGD Lo = -500 mV (default) Code = 001, PWRGD Lo = -450 mV Code = 010, PWRGD Lo = -400 mV Code = 011, PWRGD Lo = -350 mV Code = 100, PWRGD Lo = -300 mV Code = 101, PWRGD Lo = -250 mV Code = 110, PWRGD Lo = -200 mV Code = 111, PWRGD Lo = -150 mV |
| 0xE2 | R/W | 0x10 | Current Limit Threshold | 1 | This value sets the internal current limit adjustment value. The default current limit is programmed using a resistor to ground on the LIMIT pin. The value of this register adjusts this value by a percentage between 50% and 146.7%. Each LSB represents a 3.33% change in the current limit threshold. 11111 = 146.7% of external current limit 10000 = 100% of external current limit (default) 00000 = 50% of external current limit |
| 0xE3 | R/W | 0x10 | Phase Bal SW1 | 1 | These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by $\pm 25\%$ from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25 |
| 0xE4 | R/W | 0x10 | Phase Bal SW2 | 1 | These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by $\pm 25\%$ from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25 |
| 0xE5 | R/W | 0x10 | Phase Bal SW3 | 1 | These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by $\pm 25\%$ from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25 |
| 0xE6 | R/W | 0x10 | Phase Bal SW4 | 1 | These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by $\pm 25\%$ from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25 |
| 0xE7 | R/W | 0x10 | Phase Bal SW5 | 1 | These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by $\pm 25\%$ from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25 |
| 0xE8 | R/W | 0x10 | Phase Bal SW6 | 1 | These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by $\pm 25\%$ from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25 |

NCP4206

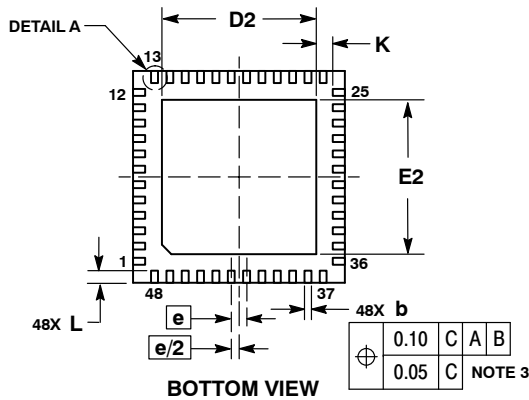
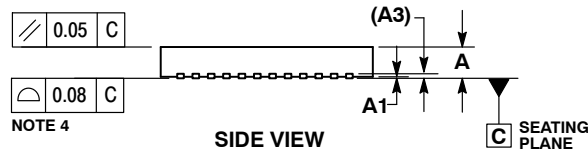
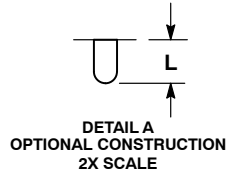
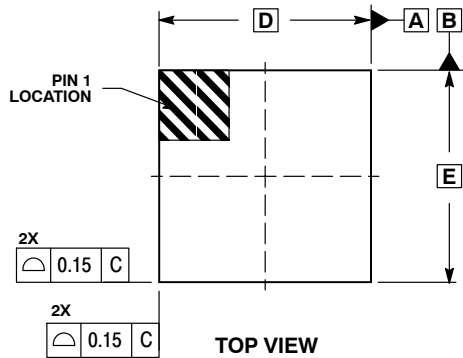
Table 12. MANUFACTURER SPECIFIC COMMAND CODES FOR THE NCP4206

| Cmd Code | R/W | Default | Description | # Bytes | Comment | | |
|----------|-----|---------|-----------------------------|---------|-----------------------------|-----------------------------|---|
| 0xF1 | R | 0x00 | ICPU MSB | 1 | | | |
| 0xF6 | R/W | 0x0002 | V _{MON} Warn Limit | 2 | V _{MON} Warn Limit | | |
| 0xF9 | R/W | 0x00 | Mask ALERT | 1 | Bit | Name | Description |
| | | | | | 7 | Mask V _{OUT} | Masks any ALERT caused by bits in Status V _{OUT} Register. |
| | | | | | 6 | Mask I _{OUT} | Masks any ALERT caused by bits in Status I _{OUT} Register. |
| | | | | | 5 | Res | Reserved |
| | | | | | 4 | Mask Temperature | Not Supported |
| | | | | | 3 | Mask CML | Masks any ALERT caused by bits in Status CML Register. |
| | | | | | 2 | V _{MON} | Masks any ALERT caused by V _{MON} exceeding its high or low limit. |
| | | | | | 1 | Res | Reserved |
| | | | | | 0 | Mask P _{OUT} | Masks any ALERT caused by P _{OUT} exceeding its programmed limit. |
| 0xFA | R/W | 0x00 | Mask FAULT | 1 | Bit | Name | Description |
| | | | | | 7 | Mask V _{OUT} FAULT | Masks any ALERT caused by OVP. |
| | | | | | 6 | Mask I _{OUT} FAULT | Masks any ALERT caused by OCP. |
| 0xFB | R | 0x10 | General Status | 1 | Bit | Name | Description |
| | | | | | 6 | ALERT | |
| | | | | | 5 | POWER GOOD | Replaced by Bit 3 of the Status Word Command |
| | | | | | 4 | RDY | |
| 0xFC | R | 0x00 | Phase Status | 1 | Bit | Name | Description |
| | | | | | 7 | Reserved | |
| | | | | | 6 | Reserved | |
| | | | | | 5 | Phase 6 | This bit is set to 1 when Phase 6 is enabled. |
| | | | | | 4 | Phase 5 | This bit is set to 1 when Phase 5 is enabled. |
| | | | | | 3 | Phase 4 | This bit is set to 1 when Phase 4 is enabled. |
| | | | | | 2 | Phase 3 | This bit is set to 1 when Phase 3 is enabled. |
| | | | | | 1 | Phase 2 | This bit is set to 1 when Phase 2 is enabled. |
| | | | | | 0 | Phase 1 | This bit is set to 1 when Phase 1 is enabled |

NCP4206

PACKAGE DIMENSIONS

QFN48 7x7, 0.5P
CASE 485AJ
ISSUE O

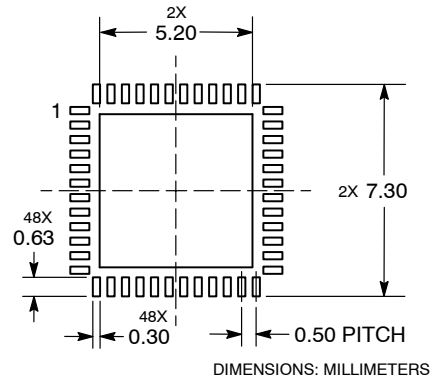


NOTES:


1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MIN | MAX |
|-----|------|------|
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.20 | 0.30 |
| D | 7.00 | BSC |
| D2 | 5.00 | 5.20 |
| E | 7.00 | BSC |
| E2 | 5.00 | 5.20 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[onsemi:](#)

[NCP4206MNR2G](#)