AR0220

1/1.8-Inch CMOS Digital Image Sensor

ON Semiconductor®

www.onsemi.com

General Description

ON Semiconductor AR0220AT is a 1/1.8−inch CMOS digital image sensor with a 1828 H x 948 V active−pixel array. This advanced automotive sensor captures images in either linear, or high dynamic range, with rolling−shutter readout. AR0220AT is optimized for both low light and challenging high dynamic range scene performance, with a 4.2 μm BSI pixel and on−sensor 120 dB HDR capture capability. The sensor includes flexible functions such as in−pixel binning, windowing, and both video and single frame modes. The sophisticated sensor fault detection features and embedded data on AR0220AT are designed to enable camera ASIL B compliance. The device is programmable through a simple two−wire serial interface, and supports MIPI output interface.

Table 1. KEY PARAMETERS

Parameter		Typical Value
Optical format		1/1.8 inch (8.93 mm)
Active pixels		1820 x 940 = 1.7M
Pixel size		4.2 μm
Color filter array		RGB Bayer, RCCC, RCCB
Shutter type		Electronic rolling shutter
Input clock range		6 − 50 MHz
Output clock maximum		85.5 MHz
Output	Serial	MIPI CSI−2 12−, 14−, 16−, or 20−bit
Frame rate	Full resolution	60 fps at 3−exposure HDR 36 fps at 4−exposure HDR
Responsivity*	RCCC (Clear)	135 ke−/lux*sec
	RGB (Green)	60.5 ke−/lux*sec
	RCCB (Clear)	135 ke−/lux*sec
SNR_{MAX}		44.7 dB
Maximum dynamic range		> 120 dB
Supply voltage	I/O	1.8 or 2.8 V
	Digital	1.2 V
	Analog	2.8 V
	MIPI	1.2 V
Power consumption (typical)		424 mW (Full resolution 60 fps MIPI 4 lane output 3−exp HDR mode) 269 mW (Full resolution 60 fps MIPI 4 lane output Linear mode)
Operating temperature		−40°C to +105°C (ambient) −40°C to +125°C (junction)
Package options		12 x 9 mm iBGA

*D65, 670 nm IRCF

Features

- High Performance 4.2 μm Automotive Grade Backside Illuminated (BSI) Pixel with DR−Pix™ Technology
- Advanced On−Sensor HDR Reconstruct with Flexible Exposure Ratio Control
- Full Resolution Video Capture at 60fps in 3−exposure HDR and 36fps in 4−exposure HDR
- Fast Single Exposure Video Capture at 100fps in 10−bit and 85fps in 12−bit output
- Line interleaved T1/T2/T3/T4 output
- Sensor Fault Detection for ASIL−B Compliance Support
- 2x2 In−pixel Binning Mode and Color Binning Mode
- Data Interfaces: 4−lane MIPI CSI−2
- Selectable Automatic or User Controlled Black Level Control
- Frame to Frame Switching Among up to 4 Contexts to Enable Multi−function Systems
- Spread−spectrum Input Clock Support
- Multi−Camera Synchronization Support
- Multiple CFA Options including RGB, and RCCC, RCCB
- These are Pb−Free Devices

Applications

- 1.7 MP, High Performance ADAS (Automotive Driver Assistant System)
- Automotive Rear View or Backup
- Automotive Surround View
- Electronic Mirror Replacement
- ADAS + Viewing Fusion
- High Dynamic Range Imaging

ORDERING INFORMATION

Part number	Description	Orderable Product Attribute Description	Package
AR0220AT3R00XUEA0−DPBR	RCCC, 0°CRA, iBGA	Dry Pack with Protective Film, Double Side BBAR Glass	iBGA87 (Pb−free)
AR0220AT3R00XUEA0−DRBR	RCCC, 0°CRA, iBGA	Dry Pack without Protective Film, Double Side BBAR Glass	
AR0220AT3R00XUD20	RCCC, 0°CRA	Recon/Die	
AR0220AT3R00XUEAH3−GEVB	RCCC, 0°CRA	Demo3 Headboard	
MARS1−AR0220AT3R−GEVB	RCCC, 0°CRA	MARS Sensor Board	
AR0220AT3C00XUEA0−DPBR	RGB, 0°CRA, iBGA	Dry Pack with Protective Film, Double Side BBAR Glass	
AR0220AT3C00XUEA0−DRBR	RGB, 0°CRA, iBGA	Dry Pack without Protective Film, Double Side BBAR Glass	
AR0220AT3C00XUD20	RGB, 0°CRA	Recon/Die	
AR0220AT3C00XUEAH3−GEVB	RGB, 0°CRA	Demo3 Headboard	
MARS1−AR0220AT3−GEVB	RGB, 0°CRA	MARS Sensor Board	
AR0220AT3B00XUEA0−DRBR	RCCB, 0°CRA, iBGA	Dry Pack without Protective Film, Double Side BBAR Glass	
AR0220AT3B00XUEA0−DPBR	RCCB, 0°CRA, iBGA	Dry Pack with Protective Film, Double Side BBAR Glass	
AR0220AT3B00XUD20	RCCB, 0°CRA	Recon/Die	
AR0220AT3B00XUEAH3−GEVB	RCCB, 0°CRA	Demo3 Headboard	

NOTE: Contact the ON Semiconductor sales or marketing representative to discuss your specific requirements.

General Description

The ON Semiconductor AR0220AT can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1820 x 940 resolution image at 60 frames per second (fps). In linear mode, it outputs 12−bit raw data, using serial MIPI output ports. In high dynamic range mode, it outputs 12−bit, 14−bit or 16−bit compressed or 20−bit linearized data using the MIPI port. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME_VALID, LINE_VALID and pixel clock can be programmed to output by GPIO pins in serial mode.

The AR0220AT includes additional features to allow application−specific tuning: windowing and offset, auto black level correction, and on−board temperature sensor. Optional register information and histogram statistic information can be embedded in first and last two lines of the image frame.

The sensor is designed to operate in a wide temperature range (−40°C to +125°C junction).

Functional Overview

The AR0220AT is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 50 MHz. The maximum output pixel rate is 85.5 Mp/s. Figure 1 shows a block diagram of the sensor.

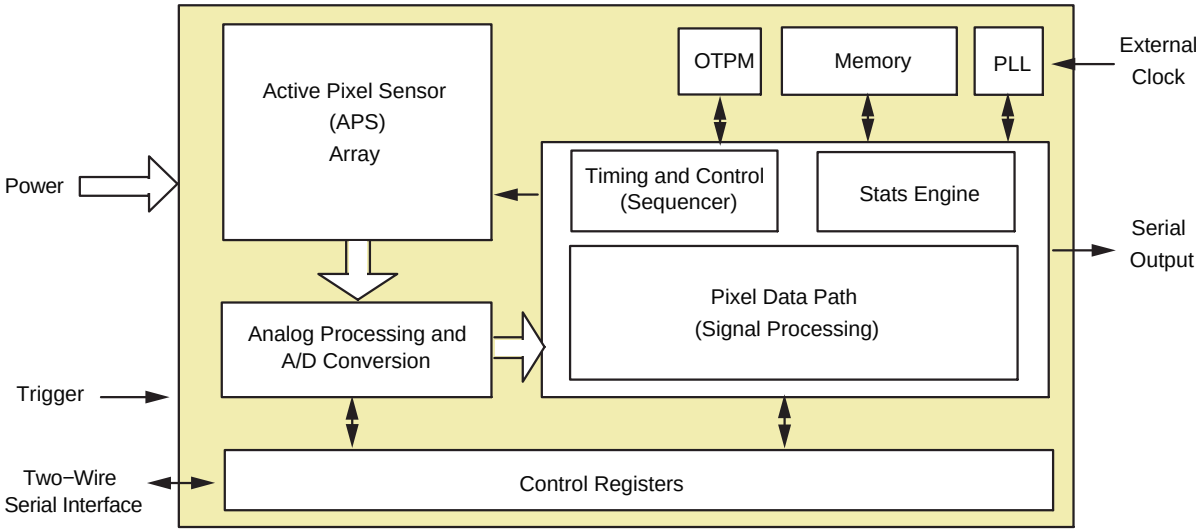


Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.7 Mp BSI Active−Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog−to−digital converter (ADC). The output from the ADC is a 12−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined onchip to produce a single image at 20−bit per pixel value. A compressing mode is further offered to allow this 20−bit pixel value to be transmitted to the host system as a 12− or 14− or 16−bit value with close to zero loss in image quality. The pixel data are output at a rate of up to 85.5 Mp/s.

Features Overview

The AR0220AT has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the AR0220AT Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

- Operating Modes
  The AR0220AT works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two−wire serial interface for both modes.
- Window Control
  Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital

binning and skipping modes are supported, as are vertical and horizontal mirror operations.

- Context Switching
  Context switching may be used to rapidly switch between two sets of register values. Refer to the AR0220AT Developer Guide for a complete set of context switchable registers.
- Gain
  The AR0220AT can be configured for analog gain of up to 4x, and digital gain of up to 8x.
- MIPI
  The AR0220 image sensor supports 4−line MIPI CSI−2 D−PHY
- PLL
  An on chip PLL provides reference clock flexibility and supports spread spectrum sources for improved EMI performance.
- Reset
  The AR0220AT may be reset by a register write, or by a dedicated input pin.
- Output Enable
  The AR0220AT output pins may be tri−stated using dedicated register bits.
- Temperature Sensor
- Black Level Correction
- Row Noise Correction
- Digital Correlated Double Sampling (CDS)
- Test Patterns
  Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to gray, and a walking 1s test pattern.

PIXEL DATA FORMAT

Pixel Array Structure

The AR0220AT pixel array is configured as 1828 columns by 948 rows (see Figure 2). The dark pixels are optically black and are used internally to monitor black level. There are 1828 columns by 948 rows of optically active pixels. While the sensor's format is 1820 x 940, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for RCCC, RCCB or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out. The optical center of the readable active pixels can be found between X_ADDR 913 and 914, and between Y_ADDR 473 and 474.

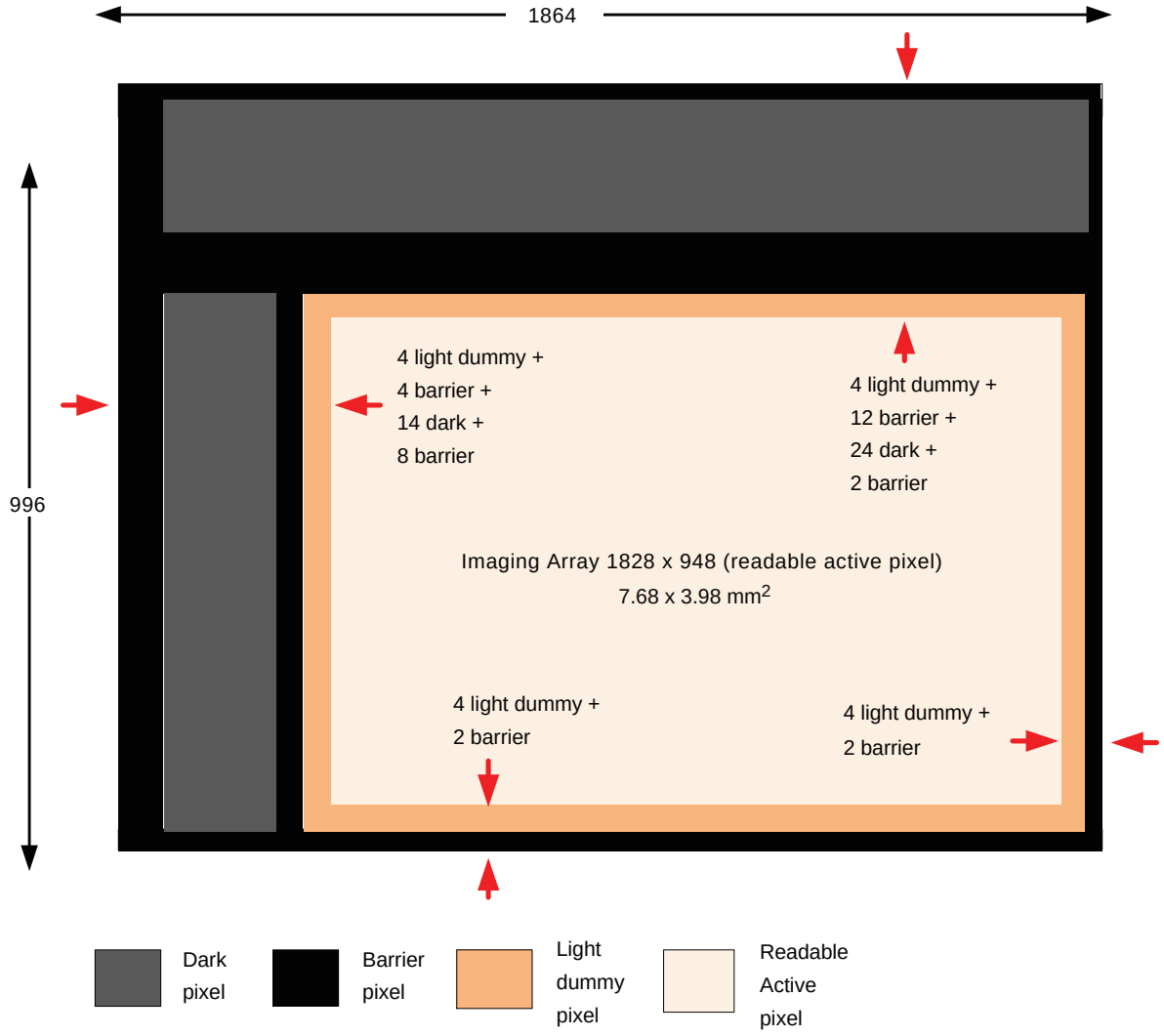


Figure 2. Pixel Array Description

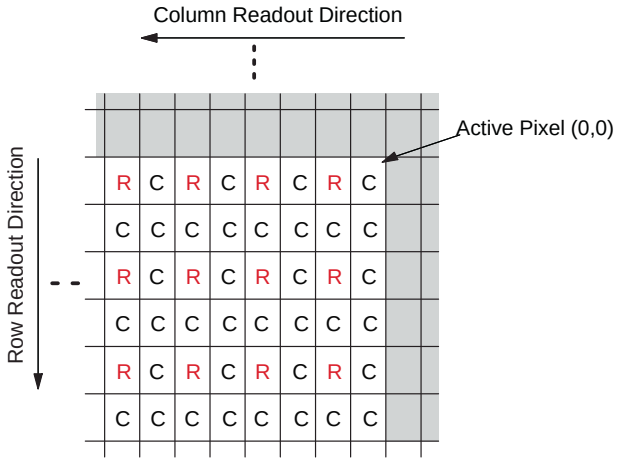


Figure 3. Pixel Color Pattern Detail (Top Right Corner) RCCC

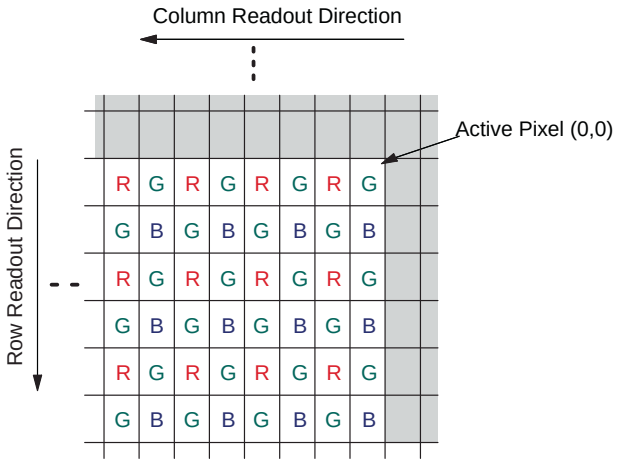


Figure 4. Pixel Color Pattern Detail (Top Right Corner) Bayer

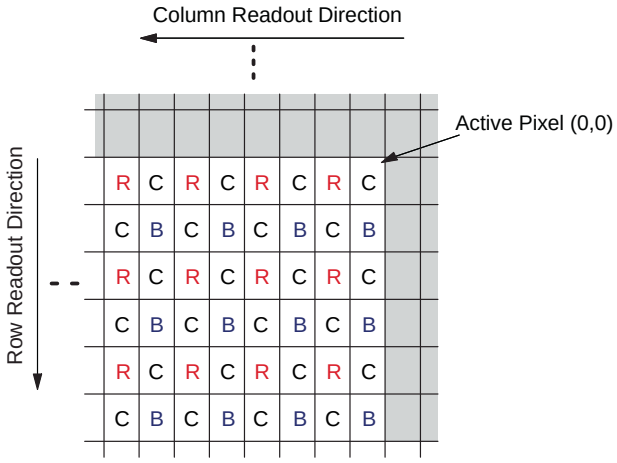


Figure 5. Pixel Color Pattern Detail (Top Right Corner) RCCB

BSI Dark Polymer and Metal Light Shield Borders

The BSI metal light shield layer is placed so that dark reference pixels (on the left and top sides) are covered by metal as required to ensure full light blockage. The readable active pixels is indicated in Figure 6 and Figure 7 by the white rectangle. Because there are no pixels on the right and bottom edges that must be covered by metal, the right and bottom edges of the BSI light shield are pulled back to help minimize RCFA effects. The curved green line in the figures represents the border of the metal light shield.

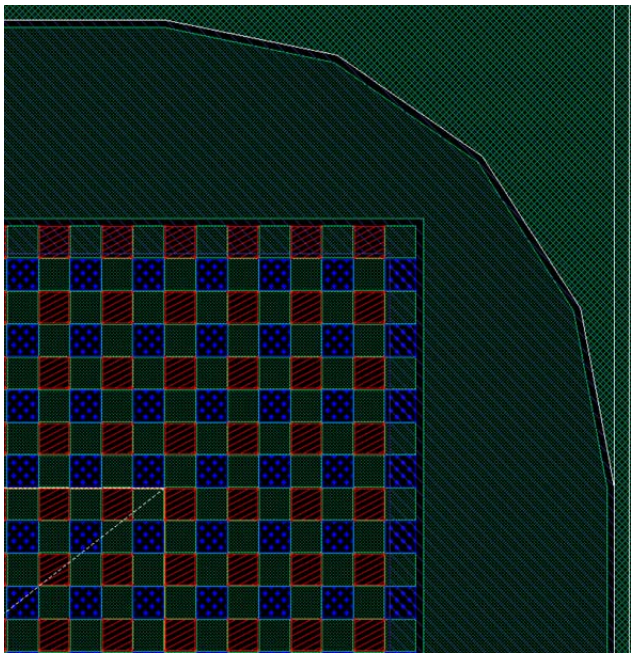


Figure 6. Upper Right Corner Detail of BSI Light Blocking

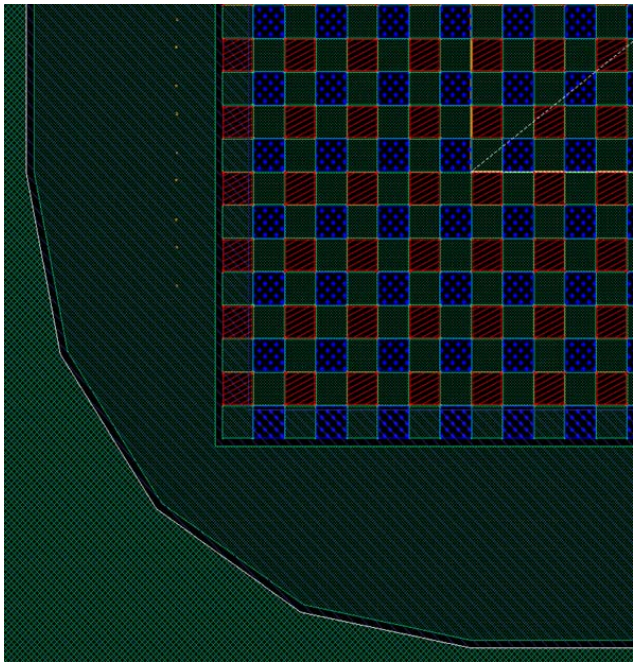


Figure 7. Lower Left Corner Detail of BSI Light Blocking

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 3). This reflects the actual layout of the array on the die.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 8. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 8.

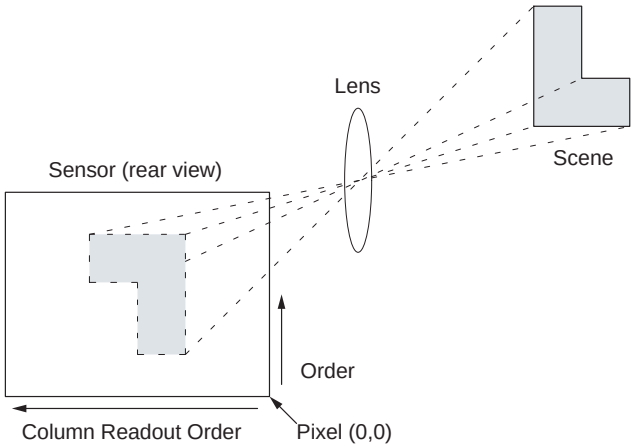


Figure 8. Imaging a Scene

CONFIGURATION AND PINOUT

The figures and tables below show a typical configuration for the AR0220 image sensor and show the package pinout.

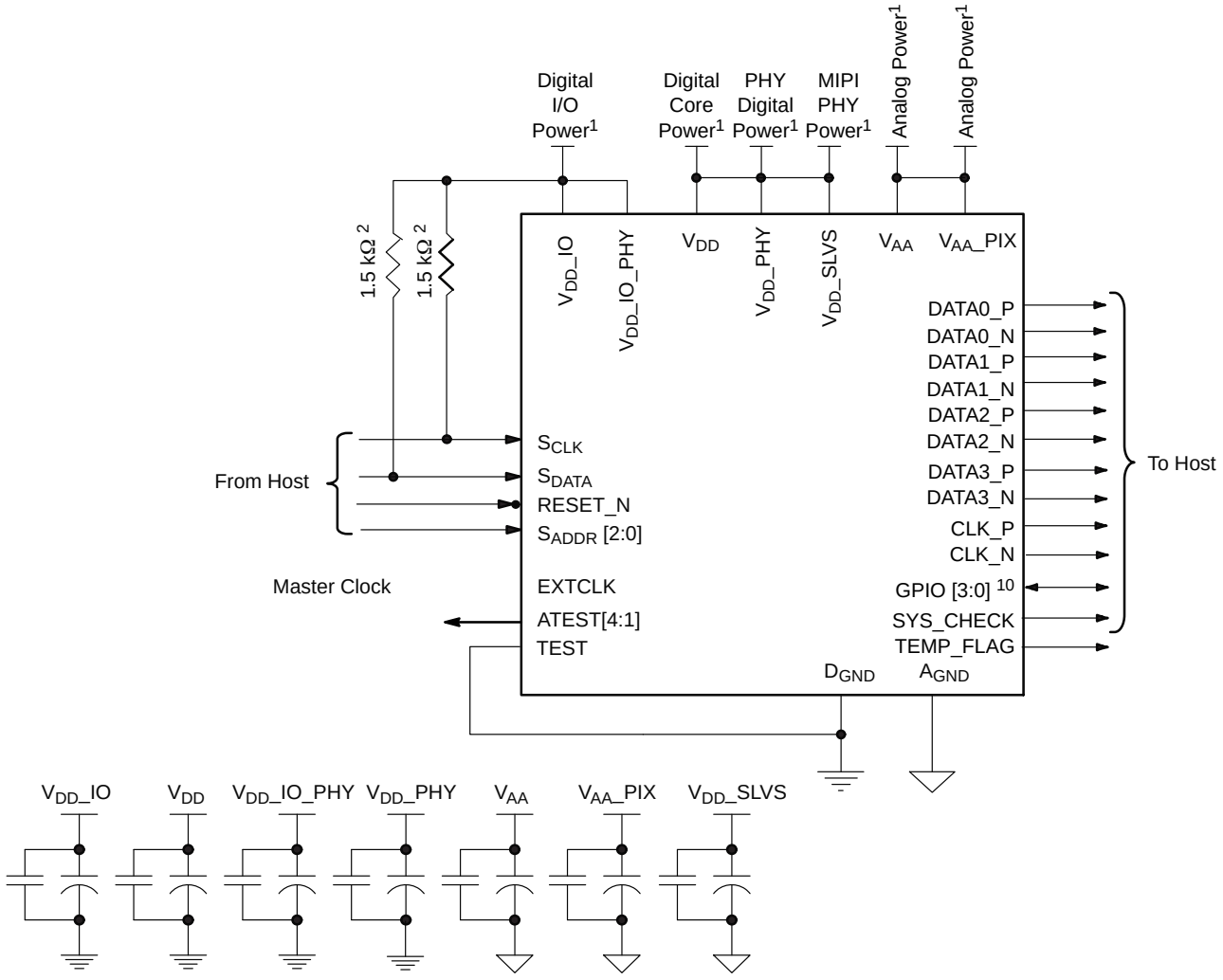


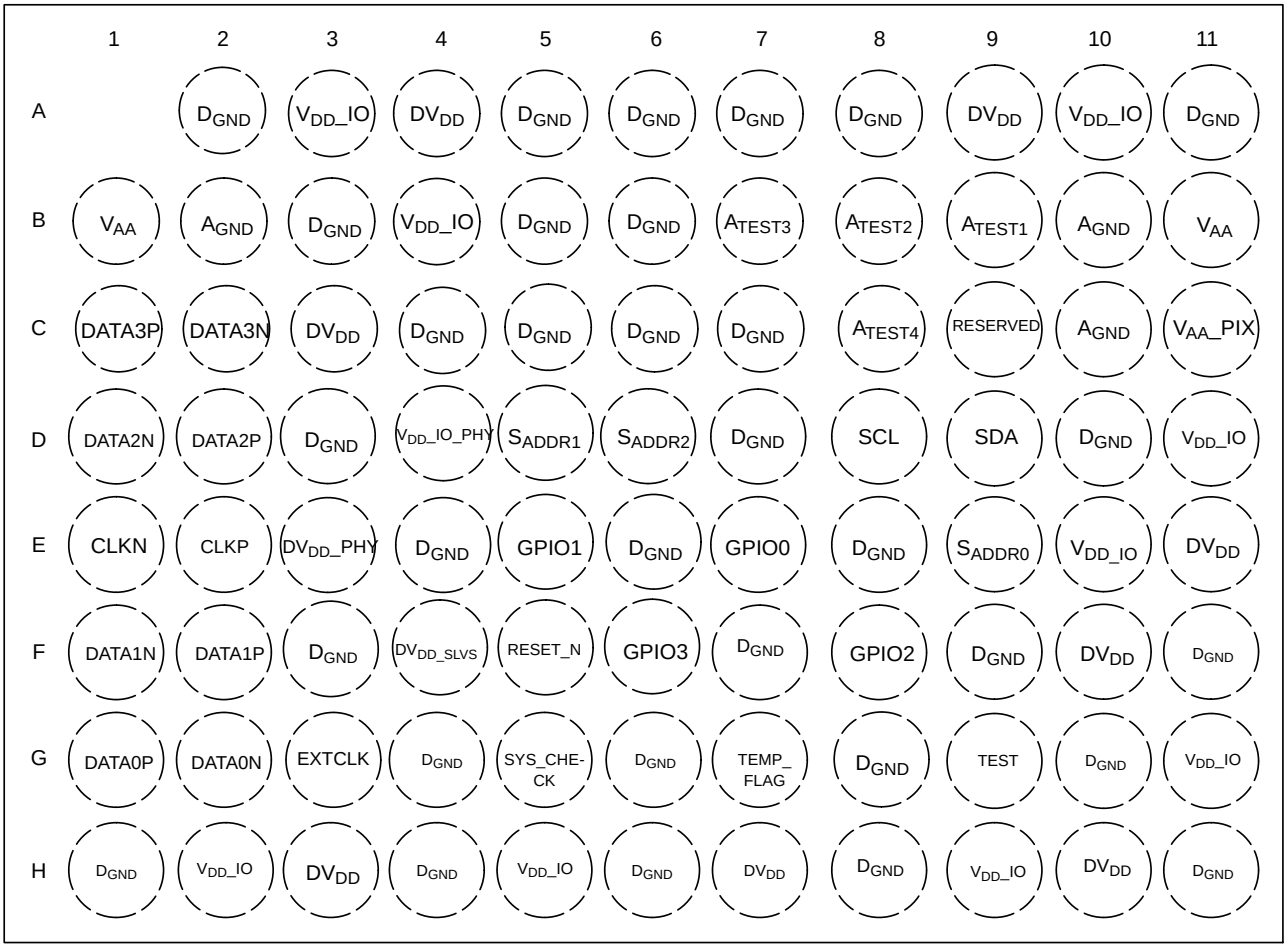
Figure 9. Typical Configuration, Four−Lane MIPI

Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. Different ATEST pins should not be tied together and should be left floating. It is recommended to have the ATEST pins brought out on the PCB and be placed as close as possible to the sensor for debug purpose
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0220 demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage current.
7. DVDD and DVDD_PHY are tied together on the chip.
8. VAA and VAA_PIX are independent on chip but should be tied together externally.
9. Most voltage combinations of VDDIO/VDDIO_PHY are allowed, except VDD_IO=1V8, VDD_IO_PHY=2V8.
10. With default GPIO configuration setting, GPIO[2:0] can be left unconnected if not used. It is recommended to tie GPIO3 to DGND if not used.

Table 2. PIN DESCRIPTIONS, 12 x 9 mm, 87−BALL iBGA

Name	iBGA Pin	Type	Description
CLKN	E1	Output	MIPI serial clock differential N
CLKP	E2	Output	MIPI serial clock differential P
DATA0N	G2	Output	MIPI serial data, lane 0, differential N
DATA0P	G1	Output	MIPI serial data, lane 0, differential P
DATA1N	F1	Output	MIPI serial data, lane 1, differential N
DATA1P	F2	Output	MIPI serial data, lane 1, differential P
DATA2N	D1	Output	MIPI serial data, lane 2, differential N
DATA2P	D2	Output	MIPI serial data, lane 2, differential P
DATA3N	C2	Output	MIPI serial data, lane 3, differential N
DATA3P	C1	Output	MIPI serial data, lane 3, differential P
TEMP_FLAG	G7	Output	Temperature monitoring flag
SYS_CHECK	G5	Output	Combined OR of all error flags
EXTCLK	G3	Input	External Input clock
RESET_N	F5	Input	Asynchronous reset (active LOW) All settings are restored to factory default
TEST	G9	Input	Manufacturing test enable pin (Tied to GND for normal operation)
SCL	D8	Input	Two−Wire Serial clock input
SDA	D9	I/O	Two−Wire Serial data I/O
SADDR0	E9	Input	Two−Wire Serial address select (LSB)
SADDR1	D5	Input	Two−Wire Serial address select
SADDR2	D6	Input	Two−Wire Serial address select (MSB)
GPIO0	E7	I/O	General Purpose I/O
GPIO1	E5	I/O	General Purpose I/O
GPIO2	F8	I/O	General Purpose I/O
GPIO3	F6	I/O	General Purpose I/O
VAA	B1, B11	Power	Analog power, 2.8 V nominal.
VAA_PIX	C11	Power	Analog pixel array power. 2.8 V nominal.
VDD_IO	A3, A10, B4, D11, E10, G11, H2, H5, H9	Power	Digital I/O power. 1.8 V or 2.8 V nominal.
DVDD	A4, A9, C3, E11, F10, H3, H7, H10	Power	Core digital power. 1.2 V nominal.
VDD_IO_PHY	D4	Power	Power to serial PHYS. Use 1.8V Use 1.8V or 2.8V nominal for MIPI.
DVDD_PHY	E3	Power	Primary PHY I/O power in MIPI mode. 1.2 V nominal.
DVDD_SLVS	F4	Power	Reference voltage for serial interface. Tie to VDD when MIPI is being used.
AGND	B2, B10, C10	Power	Analog ground
DGND	A2, A5, A6, A7, A8, A11, B3, B5, B6, C4, C5, C6, C7, D3, D7, D10, E4, E6, E8, F3, F7, F9, F11, G4, G6, G8, G10, H1, H4, H6, H8, H11	Power	Digital ground
ATEST1	B9		Analog manufacturing test access. Must be left floating for normal operation.
ATEST2	B8		Analog manufacturing test access. Must be left floating for normal operation.
ATEST3	B7		Analog manufacturing test access. Must be left floating for normal operation.
ATEST4	C8		Analog manufacturing test access. Must be left floating for normal operation.
RESERVED	C9		No connection. Must be left floating for normal operation



Top View
(Ball Down)

Figure 10. 12 x 9 mm 87−Ball iBGA Package

TWO−WIRE SERIAL REGISTER INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the AR0220AT. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two−wire serial interface specification allow the slave device to drive SCLK LOW; the AR0220AT uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements:

11. A (repeated) start condition
12. A slave address/data direction byte
13. An (a no) acknowledge bit
14. A message byte
15. A stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH−to−LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The default slave addresses used by the AR0220AT are 0x20(write address) and 0x21 (read address) in accordance with the specification. An additional 7 alternate slave address can be selected by enabling and asserting the SADDR [2:0] inputs.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which the WRITE should take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8−bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The slave’s internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from Random Location

This sequence (Figure 11) starts with a dummy WRITE to the 16−bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8−bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. Figure 11 shows how the internal register address maintained by the AR0220AT is loaded and incremented as the sequence proceeds.

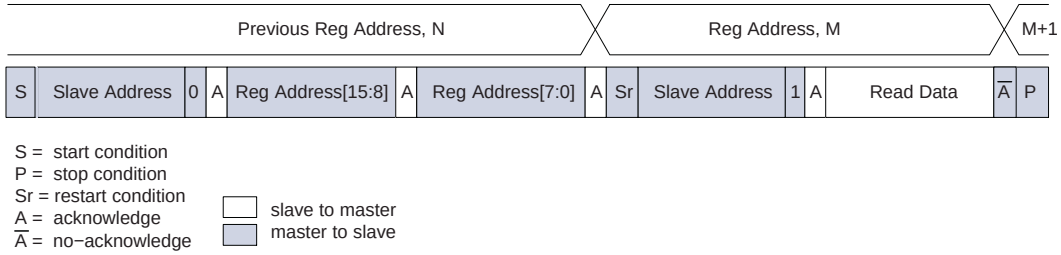


Figure 11. Single READ from Random Location

Single READ from Current Location

This sequence (Figure 12) performs a read using the current value of the AR0220AT internal register address. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

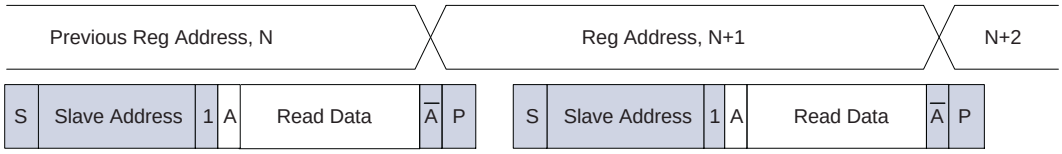


Figure 12. Single READ from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 13) starts in the same way as the single READ from random location (Figure 11). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

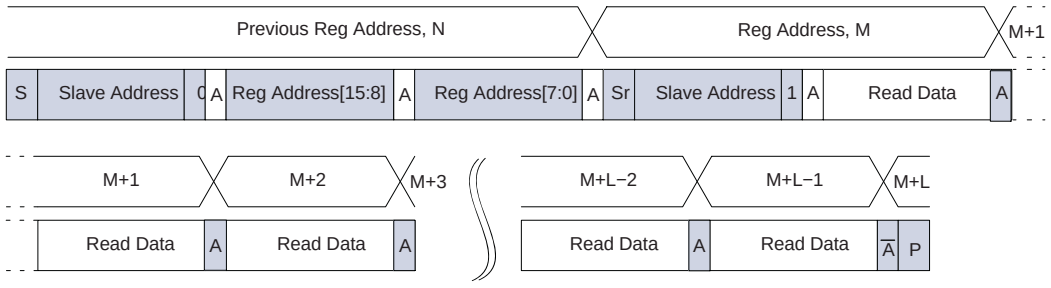


Figure 13. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 14) starts in the same way as the single READ from current location (Figure 12). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

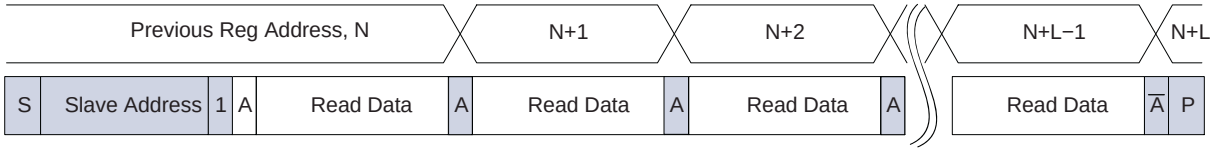


Figure 14. Sequential READ, Start from Current Location

Single WRITE to Random Location

This sequence (Figure 15) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

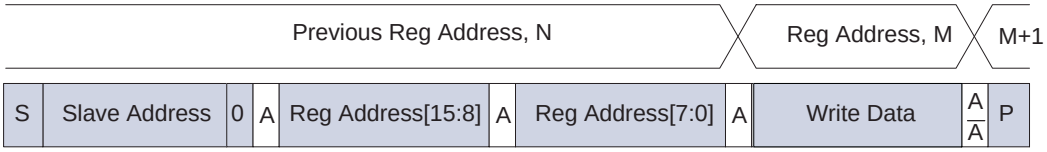


Figure 15. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 16) starts in the same way as the single WRITE to random location (Figure 15). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

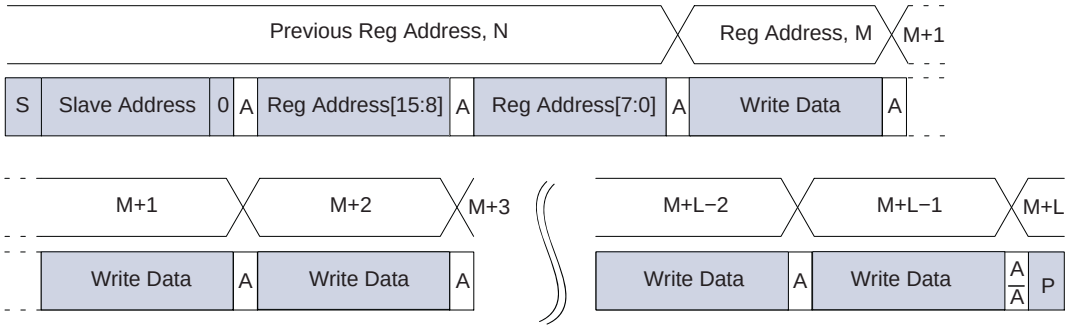
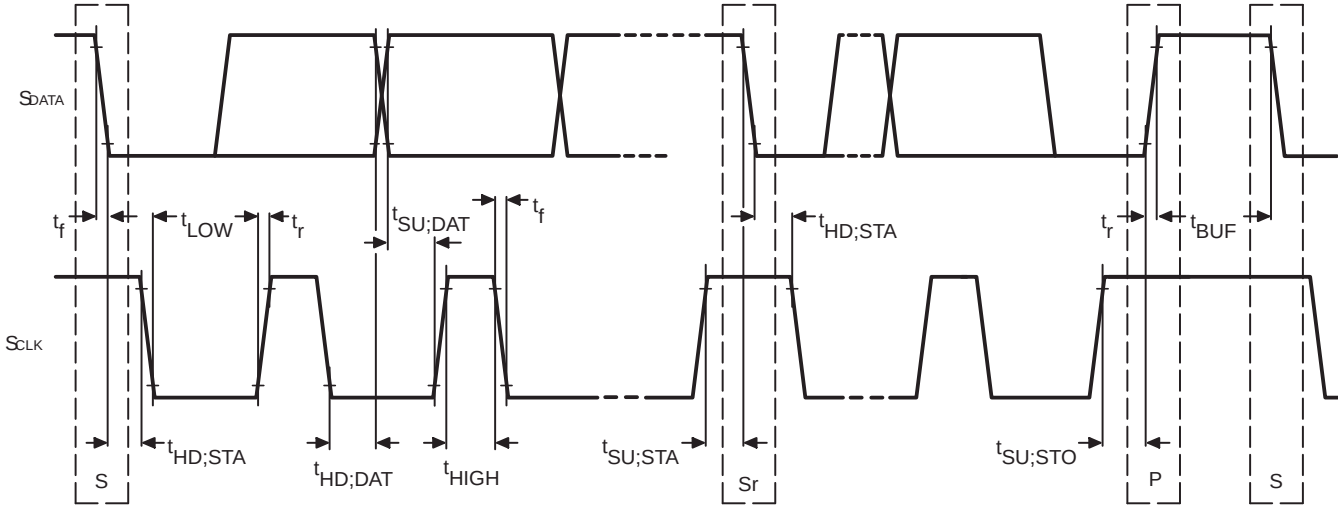


Figure 16. Sequential WRITE, Start at Random Location

ELECTRICAL SPECIFICATIONS

Two−Wire Serial Register Interface

The electrical characteristics of the two−wire serial register interface (SCLK, SDATA) are shown in Figure 17 and Table 3.



Note: Read sequence: For an 8−bit READ, read waveforms start after WRITE command and register address are issued.

Figure 17. Two−Wire Serial Bus Timing Parameters

Table 3. TWO−WIRE SERIAL BUS CHARACTERISTICS

f_{EXTCLK} = 27 MHz; V_{DD} = V_{DD}_PHY = V_{DD}_SLVS = 1.2 V; V_{DD}_IO = V_{DD}_IO_PHY = V_{AA} = V_{AA}_PIX = 2.8 V; T_A = 25°C

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
M_S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	0	1000	KHz
S_{CLK} High		8*EXTCLK + S_{CLK} rise time		8*EXTCLK + EXTCLK rise time				µs
S_{CLK} Low		6*EXTCLK + S_{CLK} rise time		6*EXTCLK + S_{CLK} rise time				µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4	−	0.6	−	0.26	−	µs
LOW period of the M_S_{CLK} clock	t_{LOW}	4.7	−	1.2	−	0.5	−	µs
HIGH period of the M_S_{CLK} clock	t_{HIGH}	4	−	0.6	−	0.26	−	µs
Set−up time for a repeated START condition	$t_{SU;STA}$	4.7	−	0.6	−	0.26	−	µs
Data hold time	$t_{HD;DAT}$	2	3.453	0	0.93	0	−	µs
Data set−up time	$t_{SU;DAT}$	250	−	100	−	50	−	ns
Rise time of both M_S_{DATA} and M_S_{CLK} time (10−90%)	t_r	−	1000	20 + 0.1 Cb (Note 4)	300	20 + 0.1 Cb (Note 4)	120	ns
Fall time of both M_S_{DATA} and M_S_{CLK} time (10−90%)	t_f	−	300	20 + 0.1 Cb (Note 4)	300	20 + 0.1 Cb (Note 4)	120	ns
Set−up time for STOP condition	$t_{SU;STO}$	4	−	0.6	−	0.26	−	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	−	1.3	−	0.5	−	µs
Capacitive load for each bus line	Cb	−	400	−	400	−	500	pF
Serial interface input pin capacitance	C_{IN_SI}	−	3.3	−	3.3	−	3.3	pF
M_S_{DATA} max load capacitance	C_{LOAD_SD}	−	30	−	30	−	30	pF
M_S_{DATA} pull−up resistor	R_{SD}	1.5	4.7	1.5	4.7	1.5	4.7	kΩ

1. This table is based on I^2C standard (v2.1 January 2000). Philips Semiconductor.
2. Two−wire control is I^2C compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD} levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of S_{CLK}. The two−wire standard specifies a minimum rise and fall time for Fast−Mode and Fast−Mode Plus modes of operation. This specification is not a timing requirement that is enforced on ON Semiconductor sensor's as a receiver, because our receivers are designed to work in mixed systems with std−mode where no such minimum rise and fall times are required/specified. However, it's the host's responsibility when using fast edge rates, especially when two−wire slew−rate driver control isn't available, to manage the generated EMI, and the potential voltage undershoot on the sensor receiver circuitry, to avoid activating sensor ESD diodes and current−clamping circuits. This is typically not an issue in most applications, but should be checked if below minimum fall times and rise times are required.
5. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
6. A Fast−mode I^2C−bus device can be used in a Standard−mode I^2C−bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard−mode I^2C−bus specification) before the S_{CLK} line is released.
7. Cb = total capacitance of one bus line in pF8.

Table 4. I/O TIMING CHARACTERISTICS (2.8 V V_{DD}_IO) (Note 1)

Symol	Definition	Condition	VDD_IO = 2.8 V [1]			Units
			Min	Typ	Max	
f_{EXTCLK}1	Input clock frequency	PLL Enabled	6	−	50	MHz
t_{EXTCLK}1	Input clock period	PLL Enabled	20	−	166	ns
t_R	Input clock rise time		−	3	−	ns
t_F	Input clock fall time		−	3	−	ns
t_{JITTER}	Input clock jitter		−	−	100	ps

1. Minimum and maximum values are taken at 105°C, 2.5 V, and −40°C, 3.1 V. All values are taken at the 50% transition point. The loading used is 20 pF.

Table 5. I/O TIMING CHARACTERISTICS (1.8 V V_{DD}_IO) (Note 1)

Symol	Definition	Condition	VDD_IO = 1.8 V [1]			Units
			Min	Typ	Max	
f_{EXTCLK}1	Input clock frequency	PLL Enabled	6	−	50	MHz
t_{EXTCLK}1	Input clock period	PLL Enabled	20	−	166	ns
t_R	Input clock rise time		−	3	−	ns
t_F	Input clock fall time		−	3	−	ns
t_{JITTER}	Input clock jitter		−	−	100	ps

1. Minimum and maximum values are taken at 105°C, 1.7 V, and −40°C, 1.95 V. All values are taken at the 50% transition point. The loading used is 20 pF.

The DC electrical characteristics are shown in the tables below.

Table 6. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Units
DV_{DD}	Core digital voltage		1.14	1.2	1.26	V
V_{DD}_IO	I/O digital voltage		1.7 / 2.6	1.8 / 2.8	1.9 / 3.0	V
V_{AA}	Analog voltage		2.6	2.8	3.0	V
V_{AA}_PIX	Pixel supply voltage		2.6	2.8	3.0	V
DV_{DD}_PHY	PHY digital voltage		1.14	1.2	1.26	V
V_{DD}_IO_PHY	Serial PHY supply voltage		1.7 / 2.6	1.8 / 2.8	1.9 / 3.0	V
DV_{DD}_SLVS	MIPI supply voltage		1.14	1.2	1.26	V
V_{IH}	Input HIGH voltage		V_{DD}_IO * 0.7	−	−	V
V_{IL}	Input LOW voltage		−	−	V_{DD}_IO * 0.3	V
I_{IN}	Input leakage current	No pull−up resistor; V_{IN} = V_{DD}_IO or D_{GND}	−	−	20	μA
V_{OH}	Output HIGH voltage		V_{DD}_IO − 0.6	−	−	V
V_{OL}	Output LOW voltage		−	−	0.4	V
I_{OH}	Output HIGH current	At specified V_{OH}	10	−	30	mA
I_{OL}	Output LOW current	At specified V_{OL}	10	−	30	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 7. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Minimum	Maximum	Units
V_{SUPPLY_2V8}	Power supply voltage 2V8	−0.3	3.6	V
V_{SUPPLY_1V8}	Power supply voltage 1V8	−0.3	2.7	V
V_{SUPPLY_1V2}	Power supply voltage 1V2	−0.3	1.6	V
I_{SUPPLY_2V8}	Power supply current 2V8	−	167	mA
I_{SUPPLY_1V8}	Power supply current 1V8	−	167	mA
I_{SUPPLY_1V2}	Power supply current 1V2	−	374	mA
I_{GND}	Total ground current	−	540	mA
V_{IN}	DC input voltage	−0.3	V_{DD}_IO + 0.3	V
V_{OUT}	DC output voltage	−0.3	V_{DD}_IO + 0.3	V
T_{STG} (Note 1)	Storage temperature	−40	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. To keep dark current and shot noise artifacts from impacting image quality, keep operating temperature at a minimum.

Table 8. OPERATING CURRENTS IN 4−LANE MIPI OUTPUT AND LINEAR MODE

Definition	Condition	Symbol	Min	Typ	Max	Units
Digital operating current	Streaming, 1820 x 940, 60 fps	I_{DD}	−	100	165	mA
I/O digital operating current	Streaming, 1820 x 940, 60 fps	I_{DD}_IO	−	0.4	4	mA
Analog operating current	Streaming, 1820 x 940, 60 fps	I_{AA}	−	38	55	mA
Pixel supply current	Streaming, 1820 x 940, 60 fps	I_{AA}_PIX	−	5	10	mA
PHY supply current	Streaming, 1820 x 940, 60 fps	I_{DD}_PHY	−	13	20	mA
IO_PHY supply current	Streaming, 1820 x 940, 60 fps	I_{DD}_IO_PHY	−	0.1	4	mA
SLVS supply current	Streaming, 1820 x 940, 60 fps	I_{DD}_SLVS	−	9	14	mA

1. Operating currents are measured at the following conditions:
   V_{AA} = V_{AA}_PIX = V_{DD}_IO = V_{DD}_IO_PHY = 2.8 V
   V_{DD} = V_{DD}_PHY = V_{DD}_SVLS = 1.2 V
   PLL Enabled and PIXCLK = 84 MHz
   T_A = 55°C
   C_{LOAD} = 20 pF
   Measured in dark

Table 9. OPERATING CURRENT IN 4−LANE MIPI OUTPUT AND 3−EXPOSURE HDR MODE

Definition	Condition	Symbol	Min	Typ	Max	Units
Digital operating current	Streaming, 1820 x 940, 60 fps	I_{DD}	−	150	220	mA
I/O digital operating current	Streaming, 1820 x 940, 60 fps	I_{DD}_IO	−	0.4	4	mA
Analog operating current	Streaming, 1820 x 940, 60 fps	I_{AA}	−	65	85	mA
Pixel supply current	Streaming, 1820 x 940, 60 fps	I_{AA}_PIX	−	12	20	mA
PHY supply current	Streaming, 1820 x 940, 60 fps	I_{DD}_PHY	−	13	20	mA
IO_PHY supply current	Streaming, 1820 x 940, 60 fps	I_{DD}_IO_PHY	−	0.1	4	mA
SLVS supply current	Streaming, 1820 x 940, 60 fps	I_{DD}_SLVS	−	9	14	mA

1. Operating currents are measured at the following conditions:
   V_{AA} = V_{AA}_PIX = V_{DD}_IO = V_{DD}_IO_PHY = 2.8 V
   V_{DD} = V_{DD}_PHY = V_{DD}_SVLS = 1.2 V
   PLL Enabled and PIXCLK = 84 MHz
   T_A = 55°C
   C_{LOAD} = 20 pF
   Measured in dark

Table 10. OPERATING CURRENT IN 4−LANE MIPI OUTPUT AND 4−EXPOSURE HDR MODE

Definition	Condition	Symbol	Min	Typ	Max	Units
Digital operating current	Streaming, 1820 x 940, 36fps	IDD	−	145	215	mA
I/O digital operating current	Streaming, 1820 x 940, 36fps	IDD_IO	−	0.1	4	mA
Analog operating current	Streaming, 1820 x 940, 36fps	IAA	−	65	85	mA
Pixel supply current	Streaming, 1820 x 940, 36fps	IAA_PIX	−	12	20	mA
PHY supply current	Streaming, 1820 x 940, 36fps	IDD_PHY	−	8	15	mA
IO_PHY supply current	Streaming, 1820 x 940, 36fps	IDD_IO_PHY	−	0.1	4	mA
SLVS supply current	Streaming, 1820 x 940, 36fps	IDD_SLVS	−	6	10	mA

1. Operating currents are measured at the following conditions:
   V_{AA} = V_{AA}_PIX = V_{DD}_IO = V_{DD}_IO_PHY = 2.8 V
   V_{DD} = V_{DD}_PHY = V_{DD}_SVLS = 1.2 V
   PLL Enabled and PIXCLK = 84 MHz
   T_A = 55°C
   C_{LOAD} = 20 pF
   Measured in dark

Table 11. OPERATING CURRENT IN 4−LANE MIPI OUTPUT AND FAST 1−EXPOSURE MODE

Definition	Condition	Symbol	Min	Typ	Max	Units
Digital operating current	Streaming, 1820 x 940, 100fps	IDD	−	120	180	mA
I/O digital operating current	Streaming, 1820 x 940, 100fps	IDD_IO	−	0.4	4	mA
Analog operating current	Streaming, 1820 x 940, 100fps	IAA	−	45	60	mA
Pixel supply current	Streaming, 1820 x 940, 100fps	IAA_PIX	−	7	12	mA
PHY supply current	Streaming, 1820 x 940, 100fps	IDD_PHY	−	13	20	mA
IO_PHY supply current	Streaming, 1820 x 940, 100fps	IDD_IO_PHY	−	0.1	4	mA
SLVS supply current	Streaming, 1820 x 940, 100fps	IDD_SLVS	−	10	15	mA

1. Operating currents are measured at the following conditions:
   V_{AA} = V_{AA}_PIX = V_{DD}_IO = V_{DD}_IO_PHY = 2.8 V
   V_{DD} = V_{DD}_PHY = V_{DD}_SVLS = 1.2 V
   PLL Enabled and PIXCLK = 84 MHz
   T_A = 55°C
   C_{LOAD} = 20 pF
   Measured in dark
   Sensor output at 10bit

Table 12. STANDBY CURRENT CONSUMPTION

Definition	Condition	Symbol	Min	Typ	Max	Units
Hard standby (clock off)	Analog, 2.8 V		−	50	200	μA
	Digital, 1.2 V		−	15	100	mA
Hard standby (clock on)	Analog, 2.8 V		−	50	200	μA
	Digital, 1.2 V		−	15	100	mA
Soft standby (clock off)	Analog, 2.8 V		−	50	200	μA
	Digital, 1.2 V		−	15	100	mA
Soft standby (clock on)	Analog, 2.8 V		−	800	2000	μA
	Digital, 1.2 V		−	20	100	mA

1. Analog − V_{AA} + V_{AA}_PIX + V_{DD}_IO + V_{DD}_IO_PHY
   Digital − V_{DD} + V_{DD}_PHY + V_{DD}_SVLS

MIPI Electrical Specifications

The ON Semiconductor AR0220AT sensor supports four lanes of MIPI data.

Compliant to MIPI standards:

- MIPI Alliance Standard for CSI−2 version 1.0
- MIPI Alliance Standard for D−PHY version 1.1

Power Up/Down Timing

Power Up

For controlled power up, RESET_N pin must be asserted (low) before supplies. Wait a minimum of 75 μsec after all supplies are valid and before RESET_N is deasserted (high). the part will begin boot−up on EXTCLK. A minimum of 360000 EXTCLK cycles must be provided before the first I2C command can be sent in order to a low the AR0220 to finish its initialization.

Vddio and Vaa power supplies need to come up simultaneously or follow specific sequence shown in Figure 18 if delayed from each other during power up. DVDD can be any order relative to the other supplies.

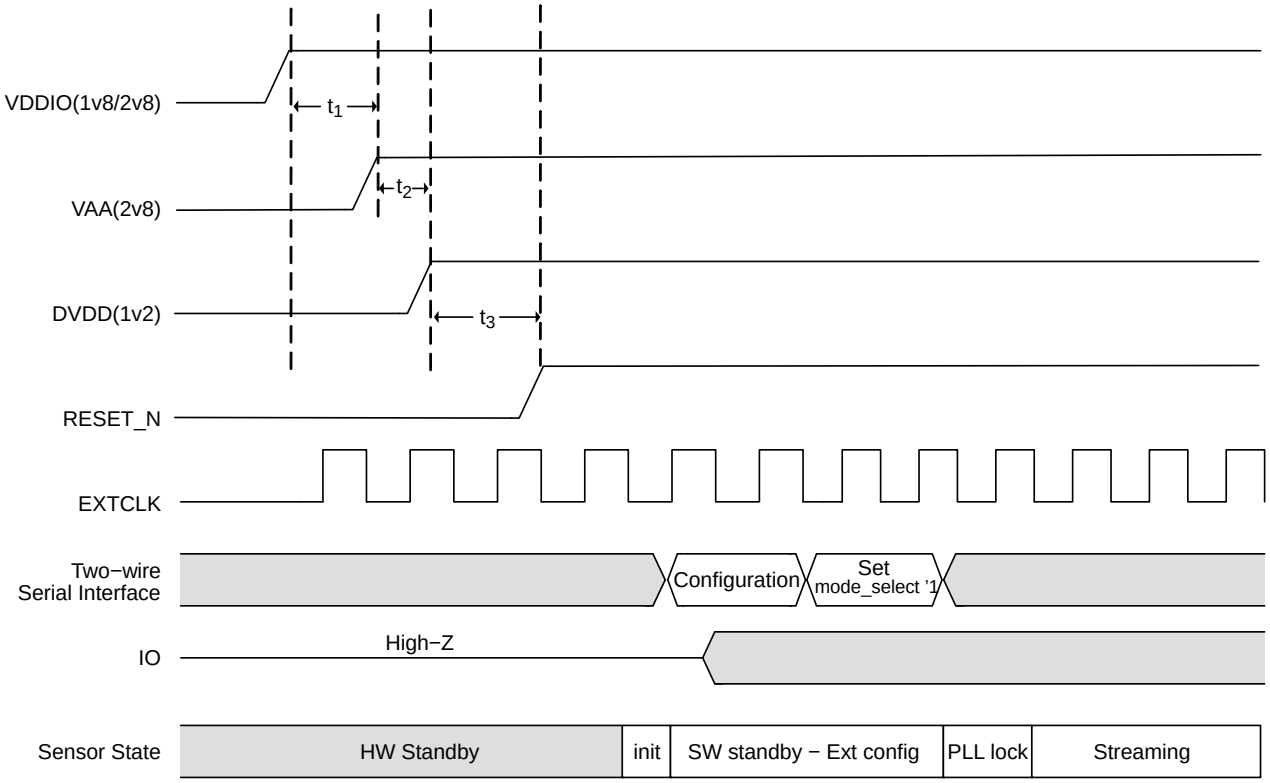


Figure 18. Initial Power Up Sequence

Table 13. POWER UP SEQUENCE

Definition	Symbol	Min	Typ	Max	Units
VDDIO rising to VAA rising	T1	0	10	−	ms
VAA rising to DVDD rising	T2	−	10	−	ms
DVDD rising to RESET_N deasserted(high)	T3	0.075	10	−	ms
Minimum number of EXTCLK cycles prior to the first Two−wire serial interface transaction (Note 2)		360000			cycles
PLL lock time		1.0			ms
External power slew rate	slew rate	−	30	50	mV/μs

2. Start up CRC check time included.

Power Down

For controlled power down, streaming must be first disabled. The RESET_N pin must be asserted (low) before any external supplies are removed. Then the supplies are allowed to be removed simultaneously or follow specific sequence shown in Figure 19 if delayed from each other during power down.

Typical Power Down Sequence:

1. De−assert Streaming: Set software standby mode (mode_select = 0) register.
2. Wait till the end of the current frame (or end−of−line if so configured).
3. Configure I/O for “hold” if desired. “Hold” state requires maintaining VDD_IO; however.
4. Set RESET_N = 0. (Hard Standby, low−leakage state)
5. Follow Power down sequence to remove supplies. For “hold” I/O state, do not power off VDD_IO supply.

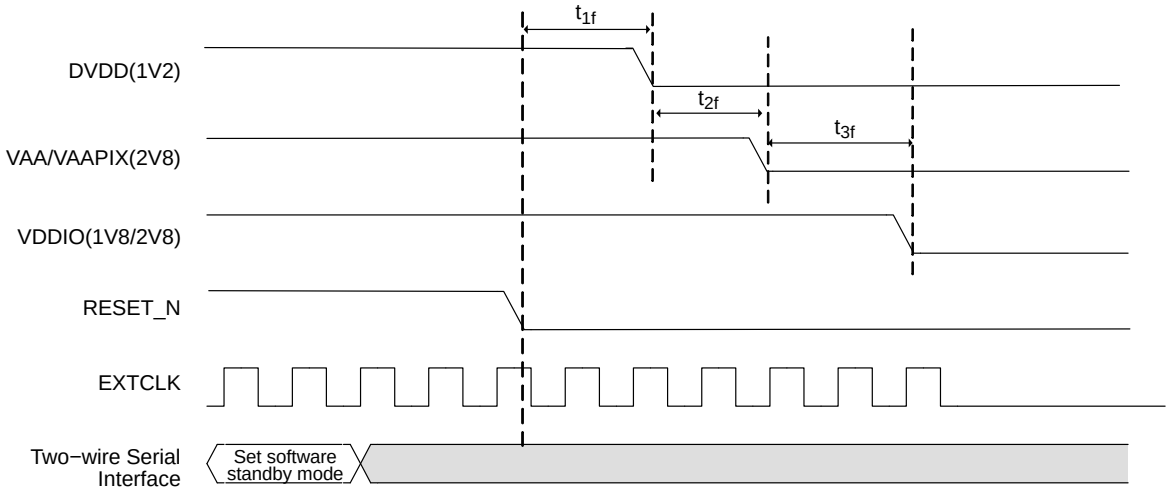


Figure 19. Power Down Sequence

Table 14. POWER DOWN SEQUENCE

Definition	Symbol	Min	Typ	Max	Units
RESET_N falling to any DVDD removal	T1f	0	−	−	ms
DVDD removal to VAA/VAAPIX removal	T2f	0	−	−	ms
VAA/VAAPIX removal to VDDIO removal	T3f	0	−	−	ms

SPECTRAL CHARACTERISTICS

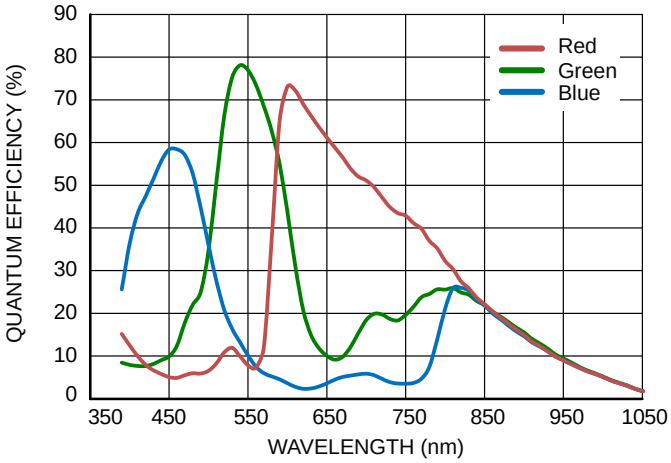


Figure 20. Quantum Efficiency − Color Sensor

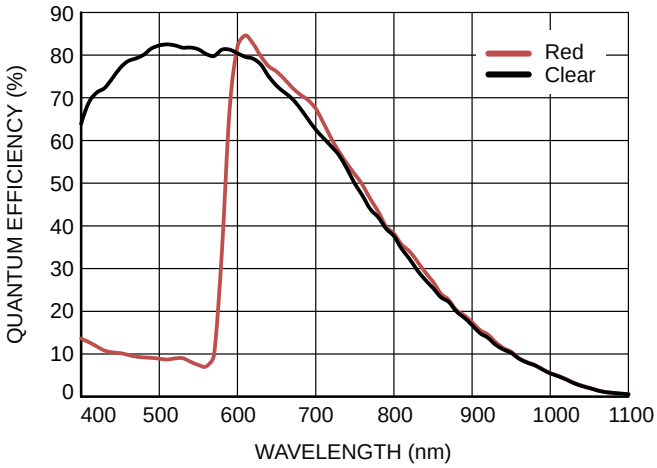


Figure 21. Quantum Efficiency − RCCC Sensor

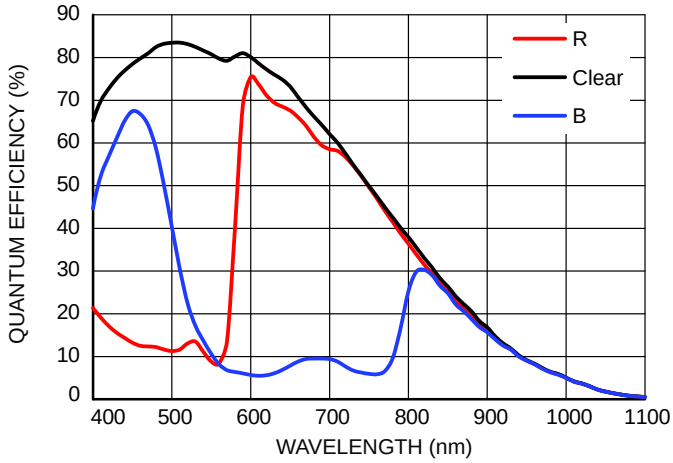
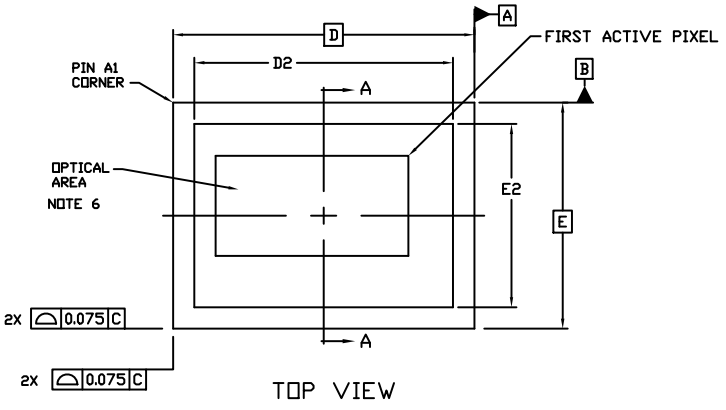
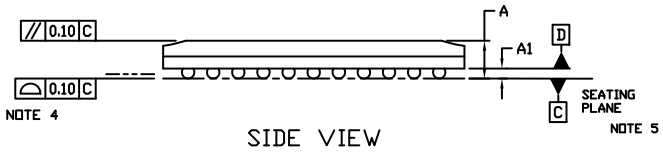


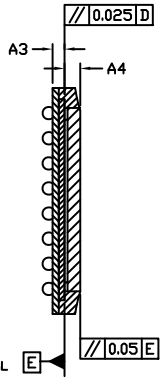
Figure 22. Quantum Efficiency − RCCB

PACKAGE DIMENSIONS

IBGA87 12x9
CASE 503BF
ISSUE A



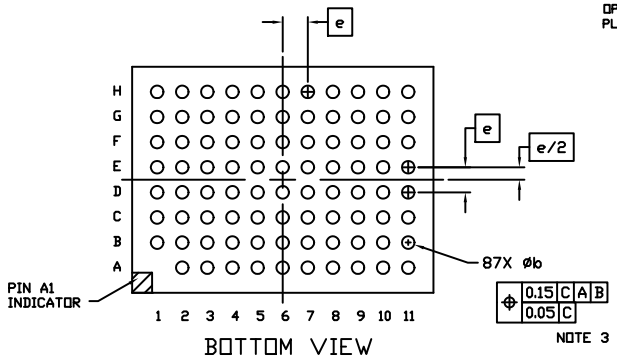


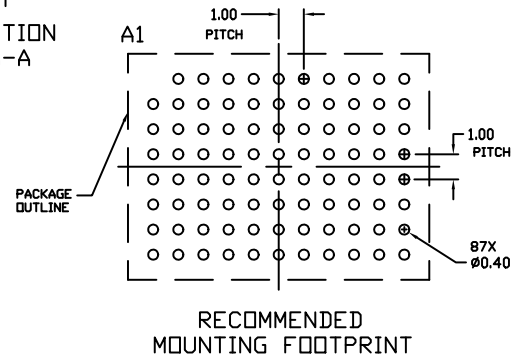


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. MAXIMUM ROTATION OF OPTICAL AREA RELATIVE D AND E WILL BE 1°. OPTICAL AREA IS DEFINED BY THE ACTIVE PIXEL ARRAY. REFER TO THE DEVICE DATA SHEET FOR TOTAL ARRAY AND FIRST ACTIVE PIXEL DEFINITIONS.
7. PARALLELISM APPLIES ONLY TO THE OPTICAL AREA.
8. OPTICAL CENTER OFFSET WITH RESPECT TO THE PACKAGE CENTER IS x=-462.70 MICRONS, Y=389.80 MICRONS ±75 MICRONS.

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	1.65
A1	0.35	0.45
A3	0.425	0.525
A4	0.575	0.675
b	0.45	0.55
D	12.00 BSC	
D2	10.20	10.40
E	9.00 BSC	
E2	7.20	7.40
e	1.00 BSC	





9. ENCAPSULANT: EPOXY
10. SUBSTRATE MATERIAL: EPOXY LAMINANTE 0.25 THICKNESS
11. LID MATERIAL: BOROSILICATE GLASS 0.500mm THICKNESS
12. SOLDER BALL MATERIAL: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu) SOLDER BALL PAD: ø0.4 SMD

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

onsemi:

AR0220AT3C00XUEAH3-GEVB AR0220AT3R00XUEAH3-GEVB