



September 2012



# FAN6862W

## Highly Integrated Green-Mode PWM Controller

### Features

- Low Standby Power: Under 0.1 W
- Low Startup Current: 8  $\mu$ A
- Low Operating Current in Green Mode: 600  $\mu$ A
- Peak-Current Mode Operation with Cycle-by-Cycle Current Limiting
- PWM Frequency Continuously Decreasing with Burst Mode at Light Loads
- $V_{DD}$  Over-Voltage Protection (OVP)
- Constant Output Power Limit (Full AC Input Range)
- Internal Latch Circuit (FAN6862WL) for OVP, OTP
- Fixed PWM Frequency (65 KHz) with Frequency Hopping
- Feedback Open-Loop Protection: 60 ms Delay
- GATE Output Maximum Voltage Clamp: 13.5V
- Soft-Start Time: 5 ms
- Soft Driving for EMI Improvement
- Full Range Frequency Hopping
- Internal OTP Sensor with Hysteresis
- Gate Driving Capability: 400 mA

### Applications

General-purpose switched-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS
- SMPS with Surge-Current Output, such as for Printers, Scanners, Motor Drivers

### Description

A highly integrated PWM controller, FAN6862W provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary Green Mode provides off-time modulation to continuously decrease the switching frequency under light-load conditions. Under zero-load conditions, the power supply enters Burst Mode, which completely shuts off PWM output. Output restarts just before the supply voltage drops below the UVLO lower limit. Green Mode enables power supplies to meet international power conservation requirements.

The FAN6862W is designed for SMPS and integrates a frequency-hopping function that helps to reduce EMI emission of a power supply with minimum line filters. To compensate the power limit variation over universal input range, a bias current limit ( $V_{LIMIT}$ ) adaptively keeps the power limit substantially constant. The gate output is clamped at 13.5 V to protect the external MOSFET from over-voltage damage.

Other protection functions include  $V_{DD}$  Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP). For OTP, an external NTC thermistor can be applied to sense the ambient temperature. When  $V_{DD}$  OVP or OTP is activated, an internal latch circuit latches off the controller. Protection types are shown in Table 1.

Table 1. Protection Type

Part Number	OVP	OLP	OTP / OTP2
FAN6862W	Latch	A/R	Latch
FAN6862WL	Latch	Latch	Latch
FAN6862WR	A/R	A/R	A/R

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6862WTY	-40 to +105°C	6-Lead, SOT23, JEDEC MO-178 Variation AB, 1.6 mm Wide	Tape & Reel
FAN6862WLT			
FAN6862WRT			

## Typical Application

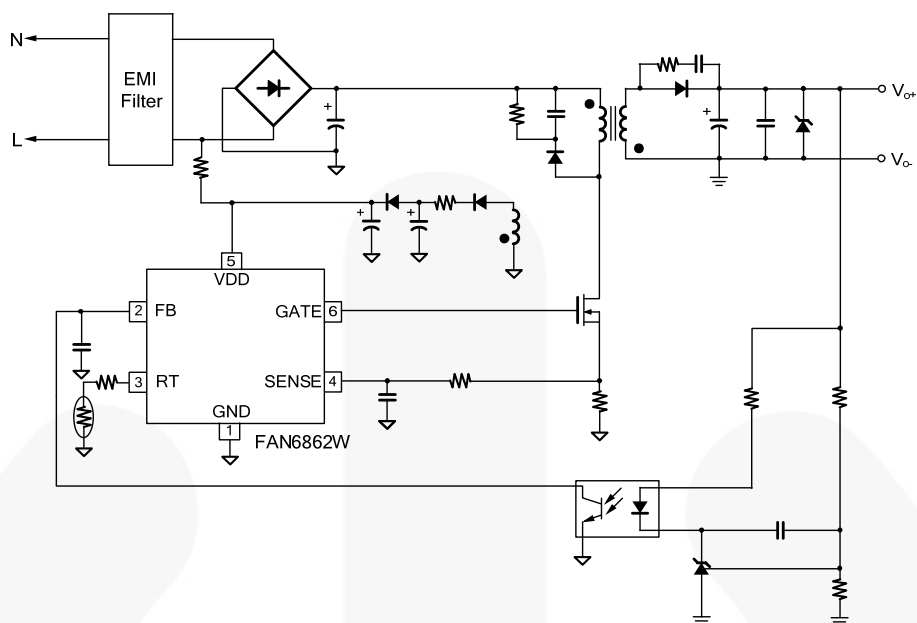


Figure 1. Typical Application

## Block Diagram

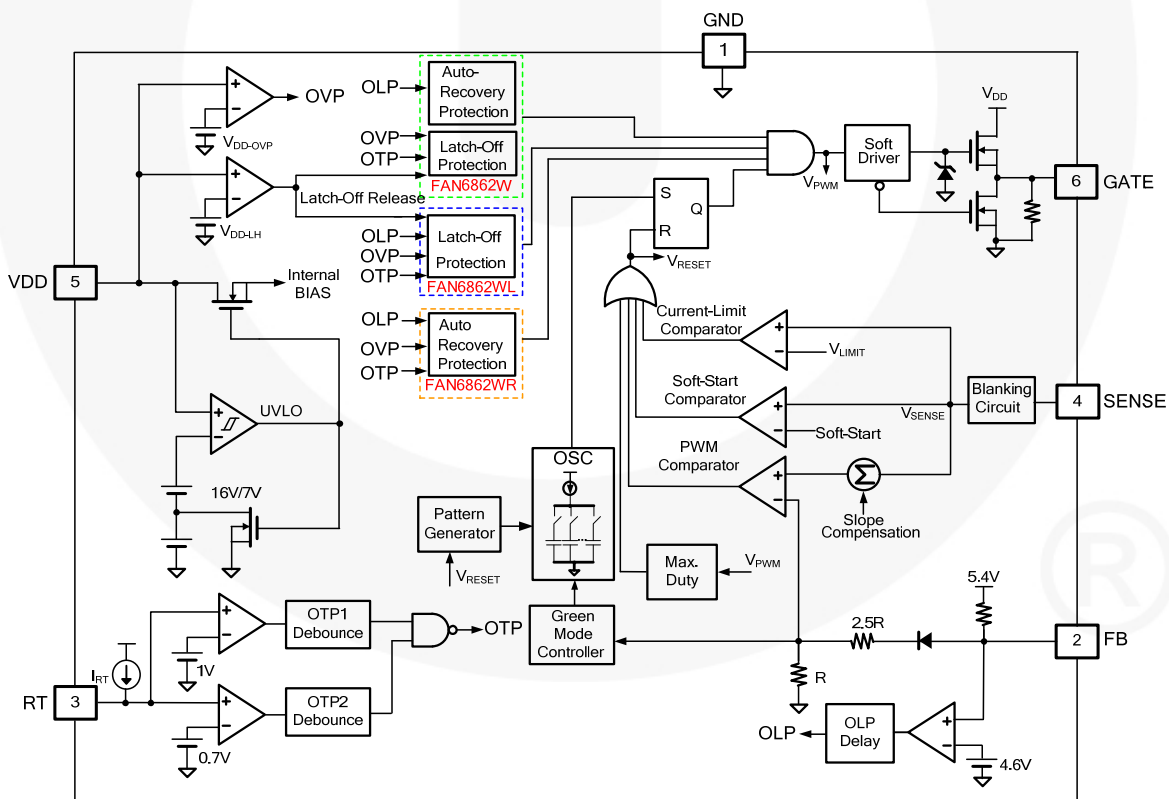


Figure 2. Block Diagram

## Marking Information

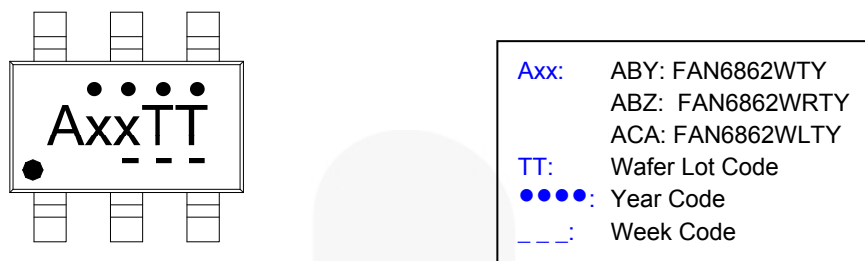


Figure 3. Top Mark

## Pin Configuration

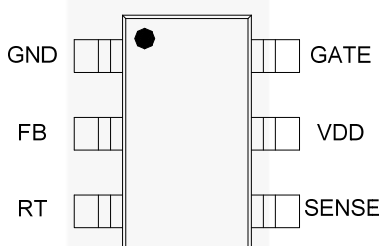


Figure 4. Pin Configuration

## Pin Definitions

Pin #	Name	Function	Description
1	GND	Ground	Ground
2	FB	Feedback	The FB pin provides the output voltage regulation signal. It provides feedback to the internal PWM comparator, so the PWM comparator can control the duty cycle. This pin also provides over-current protection. If $V_{FB}$ is higher than the trigger level and persists at that level, the controller stops and restarts.
3	RT	Temperature Detection	An external NTC thermistor is connected from this pin to the GND pin. The impedance of the NTC decreases at high temperatures. If the voltage of the RT pin drops below the threshold, PWM output is disabled.
4	SENSE	Current Sense	This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled and this activates over-current protection. This pin also provides current amplitude information for Current Mode control.
5	VDD	Power Supply	Power supply
6	GATE	Driver Output	The totem-pole output driver for driving the power MOSFET

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter	Min.	Max.	Unit
$V_{DD}$	Supply Voltage		30	V
$V_L$	Input Voltage to FB, SENSE, and RT Pins	-0.3	7.0	V
$\Theta_{JA}$	Thermal Resistance (Junction-to-Ambient)		244	°C/W
$T_J$	Operating Junction Temperature	-40	+125	°C
$T_{STG}$	Storage Temperature Range	-55	+150	°C
$T_L$	Lead Temperature, Wave Soldering, 10 Seconds		+260	°C
ESD	Human Body Model, JESD22-A114		5.5	kV
	Charge Device Model, JESD22-C101		2.0	

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$T_A$	Operating Ambient Temperature	-40	+105	°C

## Electrical Characteristics

$V_{DD} = 15\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

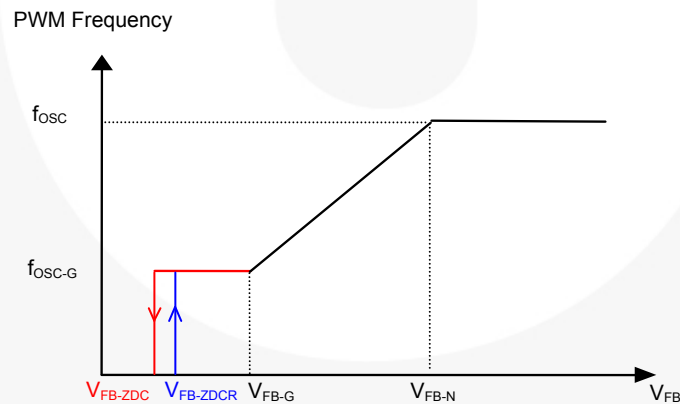
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>V<sub>DD</sub> Section</b>						
$V_{DD-OP}$	Continuously Operating Voltage				20	V
$V_{DD-ON}$	Turn-On Threshold Voltage		15	16	17	V
$V_{DD-OFF}$	Turn-Off Voltage		6.5	7.0	7.5	V
$V_{DD-LH}$	Threshold Voltage for Latch-Off Release	FAN6862W, FAN6862WL Only		4		V
$I_{DD-ST}$	Startup Current	$V_{DD-ON} - 0.16\text{ V}$		8	15	$\mu\text{A}$
$I_{DD-OP1}$	Operating Supply Current in PWM Operation	$V_{DD} = 20\text{ V}$ , $V_{FB} = 3\text{ V}$ Gate Open			2	mA
$I_{DD-OP2}$	Operating Supply Current when $V_{FB} < V_{FB-ZDC}$	$V_{DD} = 15\text{ V}$ , $V_{FB} < V_{FB-ZDC}$		600		$\mu\text{A}$
$V_{DD-OVP}$	$V_{DD}$ Over-Voltage Protection	FAN6862WL-Latch, FAN6862WR-Auto Restart	21.0	22.2	23.5	V
$t_{D-VDDOVP}$	$V_{DD}$ OVP Debounce Time			50		$\mu\text{s}$
$I_{DD-LH}$	Latch-Off Holding Current	$V_{DD} = 5\text{ V}$ ; FAN6862W, FAN6862WL Only		70	80	$\mu\text{A}$
<b>Feedback Input Section</b>						
$A_V$	Input-Voltage to Current-Sense Attenuation		1/4.0	1/3.5	1/3.0	V/V
$Z_{FB}$	Input Impedance			17		k $\Omega$
$V_{FB-OPEN}$	FB Pin Open Voltage		5.2	5.4	5.6	V
$V_{FB-OLP}$	Threshold Voltage for Open-Loop Protection		4.3	4.6	4.9	V
$t_{D-OLP}$	Open-Loop Protection Delay	$V_{FB} > V_{FB-OLP}$ , $t_{ON} > 2.5\text{ }\mu\text{s}$ , $T_A = -40\text{ to }+105^\circ\text{C}$	54	60	66	ms
$t_{D-SCP}$	Secondary Short-Circuit Protection Delay	$FB > V_{FB-OLP}$ , $t_{ON} < 2.5\text{ }\mu\text{s}$ , $T_A = -40\text{ to }+105^\circ\text{C}$	6	7	8	ms
$t_{ON-SCP}$	Short-Circuit Protection On-Time Detection	$V_{FB} > V_{FB-OLP}$ , $T_A = -40\text{ to }+105^\circ\text{C}$		2.5		$\mu\text{s}$
<b>Current Sense Section</b>						
$t_{PD}$	Delay to Output			100	250	ns
$t_{LEB}$	Leading-Edge Blanking Time		200	250		ns
$V_{LIMIT-H}$	High Threshold Voltage for Current Limit	Duty > 55%	0.57	0.60	0.63	V
$V_{LIMIT-L}$	Low Threshold Voltage for Current Limit	Duty = 0%	0.36	0.39	0.42	V
$t_{SOFT-START}$	Period During Startup Time	Startup Time	4.75	5.00	10.00	ms

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**Electrical Characteristics** (Continued) $V_{DD} = 15\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Oscillator Section</b>						
$f_{OSC}$	Normal PWM Frequency	Center Frequency	$V_{FB} > V_{FB-N}$	60	65	68
		Hopping Range	$V_{FB} \geq V_{FB-N}$		$\pm 4.0$	kHz
			$V_{FB} = V_{FB-G}^{(1)}$		$\pm 2.9$	
$t_{hop-1}$	Hopping Period 1 <sup>(1)</sup>	$V_{FB} \geq V_{FB-N}$		4.4		ms
$t_{hop-3}$	Hopping Period 3 <sup>(1)</sup>	$V_{FB} = V_{FB-G}$		11.5		ms
$f_{OSC-G}$	Green Mode Minimum Frequency		18	22	26	kHz
$V_{FB-N}$	FB Threshold Voltage for Frequency Reduction		2.35	2.50	2.65	V
$V_{FB-G}$	FB Voltage at $f_{OSC-G}$		2.05	2.20	2.30	V
$V_{FB-ZDC}$	FB Threshold Voltage for Zero-Duty			1.6		V
$V_{FB-ZDCR} - V_{FB-ZDC}$	ZDC Hysteresis			0.15		V
$f_{DV}$	Frequency Variation vs. $V_{DD}$ Deviation	$V_{DD} = 7.5\text{ V to }21\text{ V}$		0.5	2.0	%
$f_{DT}$	Frequency Variation vs. Temperature Deviation <sup>(1)</sup>	$T_A = -40\text{ to }+105^\circ\text{C}$			2	%

Continued on following page...

**Figure 5. PWM Frequency**

**Electrical Characteristics** (Continued) $V_{DD} = 15\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>PWM Output Section</b>						
$DCY_{MAX}$	Maximum Duty Cycle		60	70	75	%
$V_{OL}$	Output Voltage LOW	$V_{DD} = 15\text{ V}$ , $I_O = 50\text{ mA}$			1.5	V
$V_{OH}$	Output Voltage HIGH	$V_{DD} = 8\text{ V}$ , $I_O = 50\text{ mA}$	6			V
$t_R$	Rising Time (with Soft Driving)	$GATE = 1\text{ nF}$		150		ns
$t_F$	Falling Time	$GATE = 1\text{ nF}$		35		ns
$V_{CLAMP}$	Gate Output Clamping Voltage	$V_{DD} = 20\text{ V}$	12.0	13.5	15.0	V
$I_{O-SOURCE}$	Gate Source Driving Capability <sup>(1)</sup>	$V_{DD} = 15\text{ V}$		400		mA
$I_{O-SINK}$	Gate Sink Driving Capability <sup>(1)</sup>	$V_{DD} = 15\text{ V}$		400		mA
<b>Over-Temperature Protection (OTP) Section</b>						
$R_{RT}$	Maximum External Resistance of RT Pin to Trigger Protection		9	10	11	k $\Omega$
$V_{OTP}$	Threshold Voltage for Over-Temperature Protection	FAN6862W, FAN6862WL-Latch, FAN6862WR-Auto Restart, at $25^\circ\text{C}$	0.94	1.00	1.06	V
$I_{RT}$	Output Current of RT Pin		92	100	108	$\mu\text{A}$
$t_{DOTP}$	Over-Temperature Debounce Time	$V_{FB} = V_{FB-N}$	14	17	19	ms
$V_{OTP2}$	Second Threshold Voltage for Over-Temperature Protection	FAN6862W, FAN6862WL-Latch, FAN6862WR-Auto Restart, at $25^\circ\text{C}$	0.65	0.70	0.75	V
$t_{DOTP2}$	Second Over-Temperature Debounce Time		80	135	200	$\mu\text{s}$
$T_{OTP}$	Protection Junction Temperature <sup>(1,2)</sup>			+135		$^\circ\text{C}$
$T_{Restart}$	Restart Junction Temperature <sup>(1,3)</sup>			$T_{OTP} - 25$		$^\circ\text{C}$

**Notes:**

1. Guarantee by design.
2. When activated, the output is disabled and the latch is turned off.
3. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

## Typical Performance Characteristics

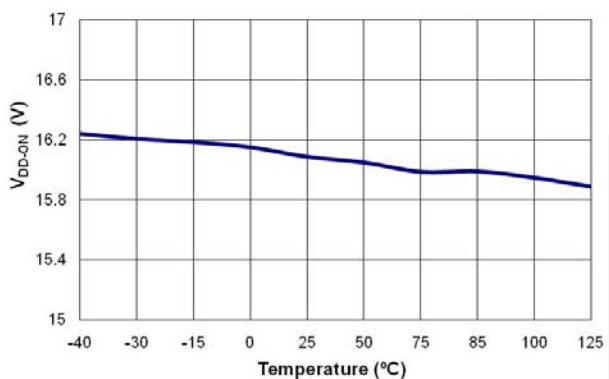


Figure 6. Turn-On Threshold Voltage ( $V_{DD-ON}$ ) vs. Temperature

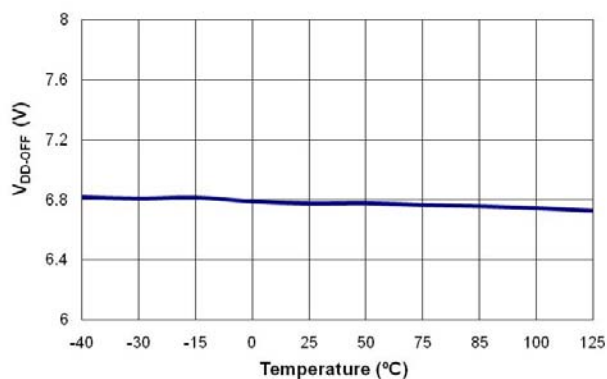


Figure 7. Turn-Off Threshold Voltage ( $V_{DD-OFF}$ ) vs. Temperature

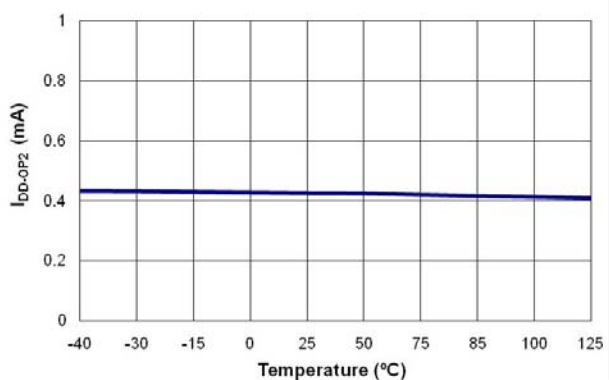


Figure 8. Operating Current ( $I_{DD-OP2}$ ) vs. Temperature

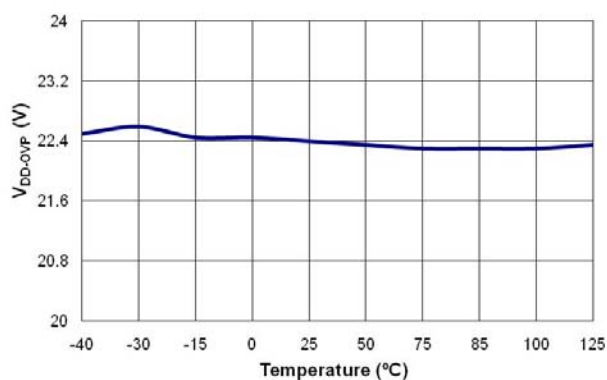


Figure 9.  $V_{DD}$  Over-Voltage Protection ( $V_{DD-OVP}$ ) vs. Temperature

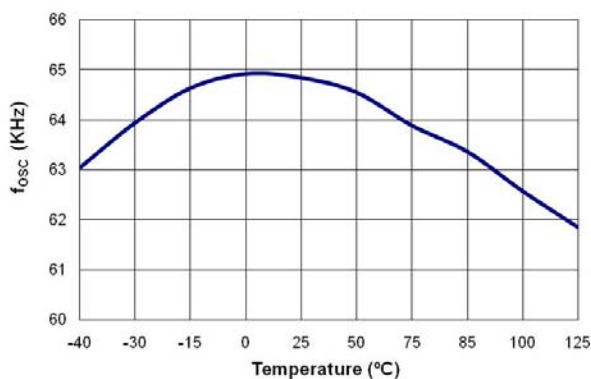


Figure 10. Center Frequency ( $f_{OSC}$ ) vs. Temperature

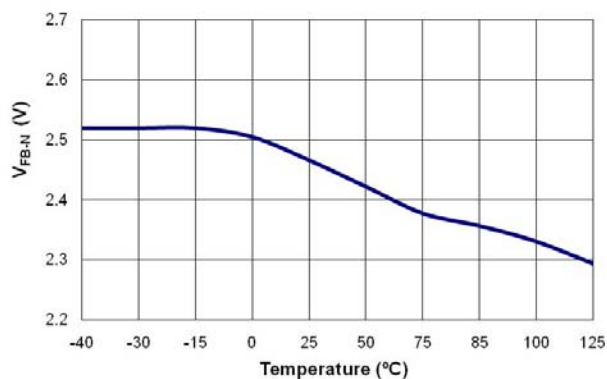
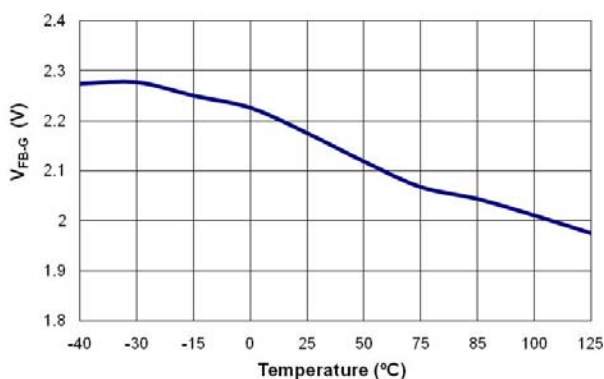
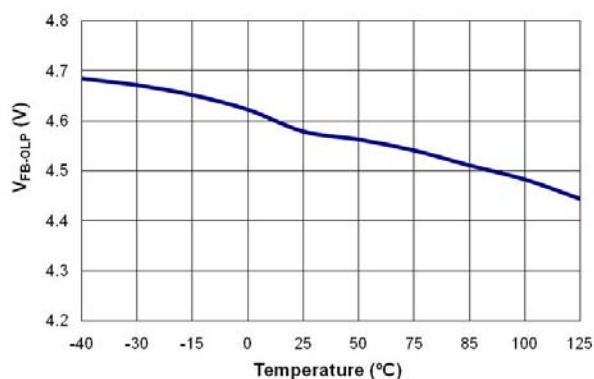
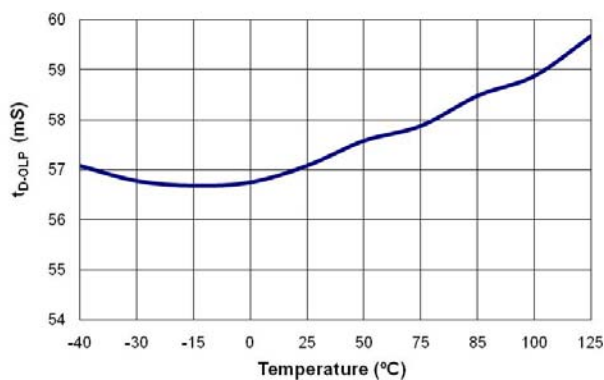
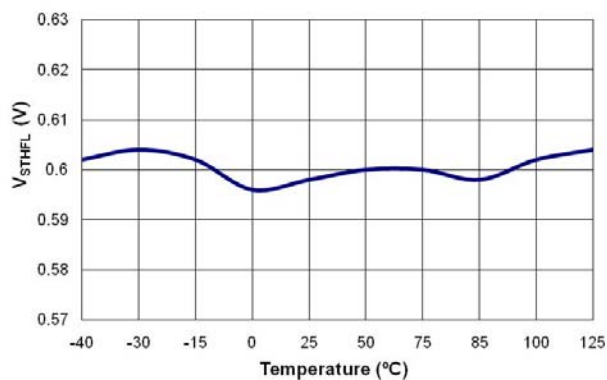
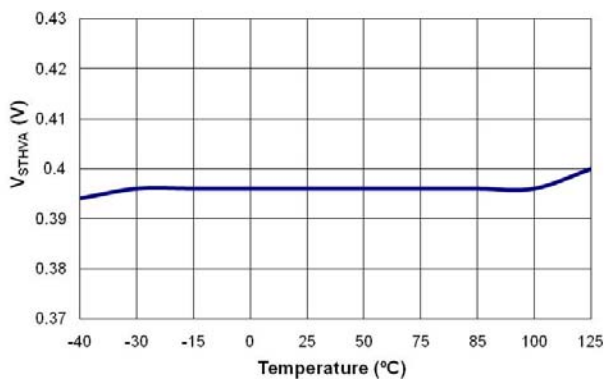
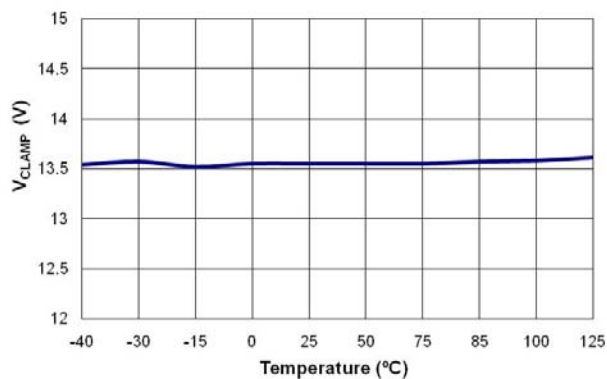


Figure 11. FB Threshold Voltage for Frequency Reduction ( $V_{FB-N}$ ) vs. Temperature



## Typical Performance Characteristics (Continued)

Figure 12. FB Voltage at  $f_{OSC-G}$  ( $V_{FB-G}$ ) vs. TemperatureFigure 13. Threshold Voltage for Open-Loop Protection ( $V_{FB-OLP}$ ) vs. TemperatureFigure 14. Open-Loop Protection Delay ( $t_{D-OLP}$ ) vs. TemperatureFigure 15. Flat Threshold Voltage for Current Limit ( $V_{LIMIT-H}$ ) vs. TemperatureFigure 16. Valley Threshold Voltage for Current Limit ( $V_{LIMIT-L}$ ) vs. TemperatureFigure 17. GATE Output Clamping Voltage ( $V_{CLAMP}$ ) vs. Temperature

## Typical Performance Characteristics (Continued)

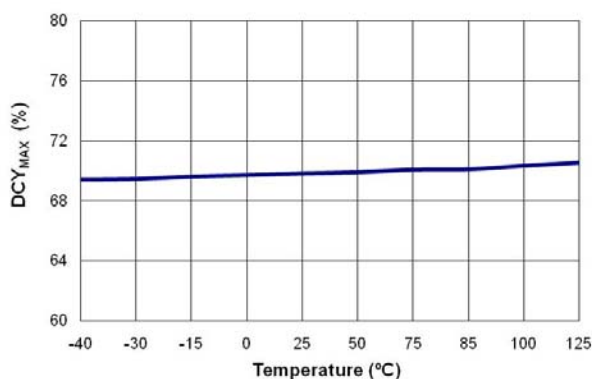


Figure 18. Maximum Duty Cycle (DCY<sub>MAX</sub>) vs. Temperature

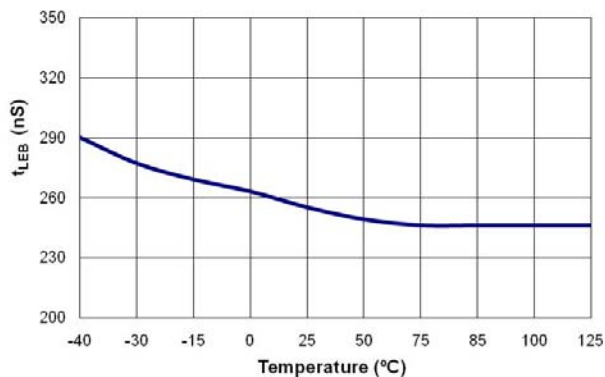


Figure 19. Leading-Edge Blanking Time (t<sub>LEB</sub>) vs. Temperature

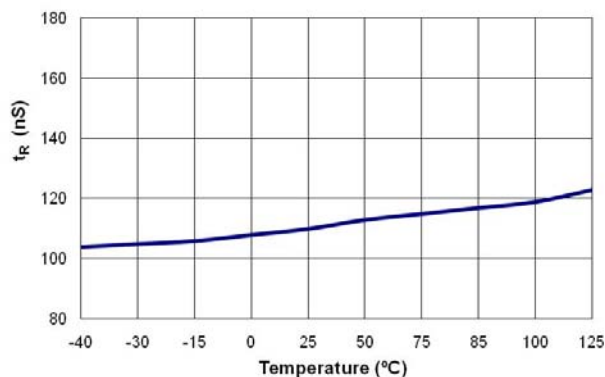


Figure 20. Rising Time (t<sub>R</sub>) vs. Temperature

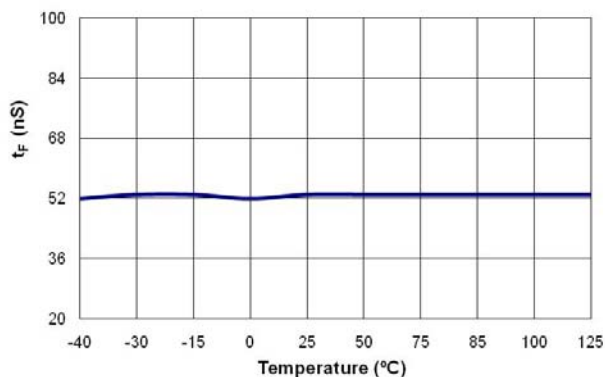


Figure 21. Falling Time (t<sub>F</sub>) vs. Temperature

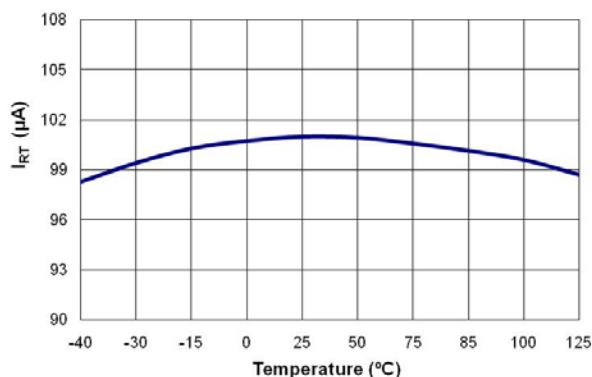


Figure 22. Output Current of RT Pin (I<sub>RT</sub>) vs. Temperature

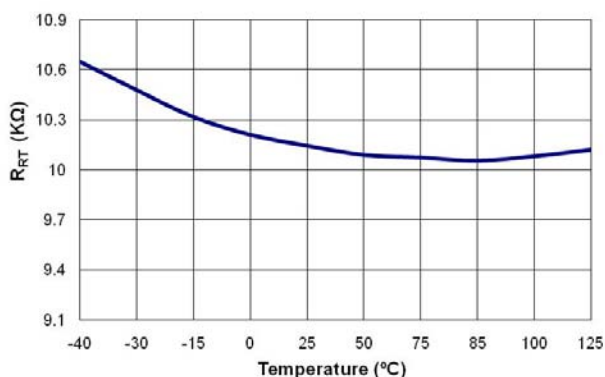


Figure 23. Maximum External Resistance of RT Pin to Trigger Protection (R<sub>RT</sub>) vs. Temperature

## Operation Description

### Startup Operation

Figure 24 shows a typical startup circuit and transformer auxiliary winding for a typical application. Before switching operation begins, FAN6862W consumes only startup current (typically 8  $\mu$ A) and the current supplied through the startup resistor charges the  $V_{DD}$  capacitor ( $C_{DD}$ ). When  $V_{DD}$  reaches turn-on voltage of 16 V ( $V_{DD-ON}$ ), switching begins and the current consumed increases to 2 mA. Power is then supplied from the transformer auxiliary winding. The large hysteresis of  $V_{DD}$  (7 V) provides more holdup time, which allows using a small capacitor for  $V_{DD}$ . The startup resistor is typically connected to AC line for a fast reset of latch protection.

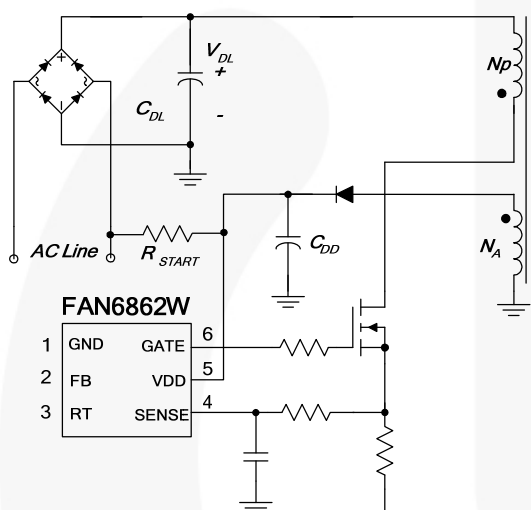


Figure 24. Startup Circuit

### Green-Mode Operation

The FAN6862W uses feedback voltage ( $V_{FB}$ ) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 25, such that the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 65 kHz. Once  $V_{FB}$  decreases below  $V_{FB-N}$  (2.5 V), the PWM frequency starts to linearly decrease from 65 kHz to 22.5 kHz to reduce the switching losses. As  $V_{FB}$  decreases below  $V_{FB-G}$  (2.2 V), the switching frequency is fixed at 22.5 kHz and FAN6862W enters “deep” Green Mode, where the operating current decreases to 600  $\mu$ A (maximum), further reducing the standby power consumption. As  $V_{FB}$  decreases below  $V_{FB-ZDC}$  (1.6V), FAN6862W enters Burst-Mode operation. When  $V_{FB}$  drops below  $V_{FB-ZDC}$ , switching stops and the output voltage starts to drop, which causes the feedback voltage to rise. Once  $V_{FB}$  rises above  $V_{FB-ZDC}$ , switching resumes. Burst Mode alternately enables and disables switching, thereby reducing switching loss in Standby Mode, as shown in Figure 26.

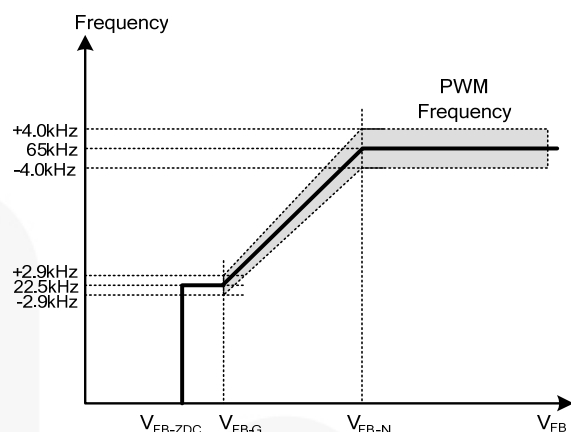


Figure 25. PWM Frequency

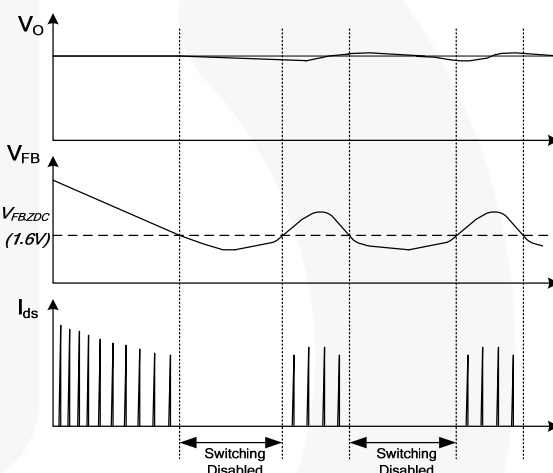


Figure 26. Burst-Mode Operation

### Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. An internal frequency-hopping circuit changes the switching frequency between 61.0 kHz and 69.0 kHz with a period of 4.4 ms, as shown in Figure 27. This covers the whole frequency range and shrinks the period with operation frequency proportionally.

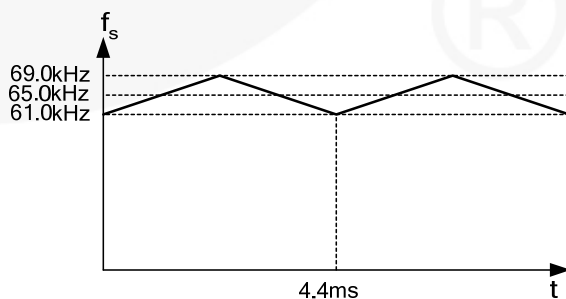


Figure 27. Frequency Hopping

## Protections

Self-protective functions include  $V_{DD}$  Over-Voltage Protection (OVP), Open-Loop / Overload Protection (OLP), Over-Current Protection (OCP), Short-Circuit Protection (SCP) and Over-Temperature Protection (OTP). OLP, OCP and SCP are Auto-Restart Mode protections; OVP and OTP are Latch-Mode protections.

### Auto-Restart Mode Protection

Once a fault condition is detected, switching is terminated and the MOSFET remains off. This causes  $V_{DD}$  to fall because no more power is delivered from auxiliary winding. When  $V_{DD}$  falls to  $V_{DD-OFF}$  (7 V), the protection is reset and the operating current reduces to startup current, which causes  $V_{DD}$  to rise. FAN6862W resumes normal operation when  $V_{DD}$  reaches  $V_{DD-ON}$  (16 V). In this manner, the auto-restart can alternately enable and disable the switching of the MOSFET until the fault condition is eliminated (see Figure 28).

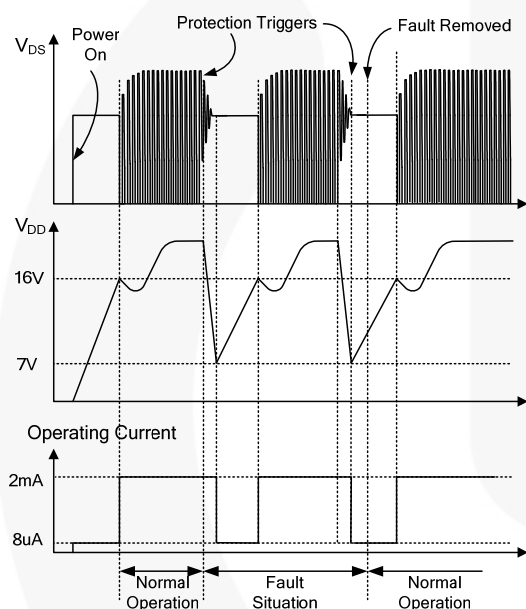


Figure 28. Auto Restart Operation

### Latch-Mode Protection

Once this protection is triggered, switching is terminated and the MOSFET remains off. The latch is reset only when  $V_{DD}$  is discharged below 4 V by unplugging the AC power line.

### Over-Current Protection (OCP)

FAN6862W over-current protection is a pulse-by-pulse bias current limit threshold ( $V_{LIMIT}$ ) that turns off the MOSFET once the sensing voltage of MOSFET drain current reaches the threshold. The  $V_{LIMIT}$  compensates the power-limit variation over the universal input range and adaptively keeps the power limit constant.

### Open-Loop / Overload Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator (KA431 shown in Figure 29) is broken, no current flows through the photo-coupler transistor, which pulls up the feedback voltage to 5.4 V.

When feedback voltage is above 4.6 V for longer than 60 ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value for longer than 60 ms due to the overload condition.

If the secondary output-short situation occurs when the feedback voltage is above 4.6 V, protection time is 7 ms for shorter debounce time.

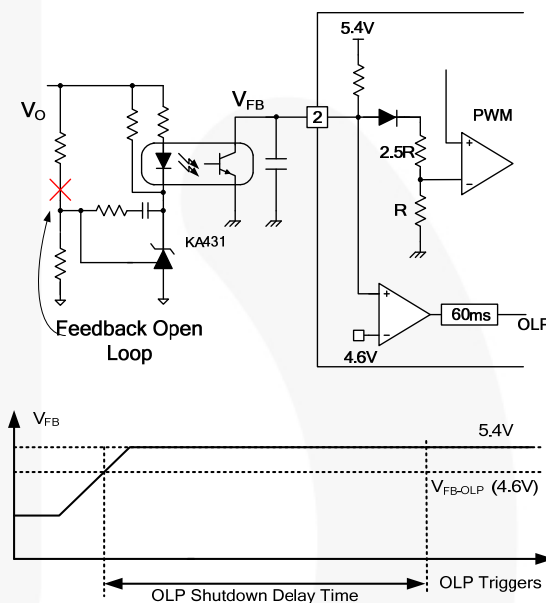


Figure 29. OLP Operation

### $V_{DD}$ Over-Voltage Protection (OVP)

$V_{DD}$  over-voltage protection prevents IC damage caused by over voltage on the  $V_{DD}$  pin. The OVP is triggered when  $V_{DD}$  reaches 22.2 V. A debounce time (typically 50  $\mu$ s) prevents false triggering by switching noise.

### Over-Temperature Protection (OTP)

The OTP circuit is composed of current source and voltage comparators. Typically, an NTC thermistor is connected between the RT and GND pins. If the voltage of this pin drops below a threshold of 1.0 V, PWM output is disabled after  $t_{DOTP}$  debounce time. If this pin voltage drops below 0.7 V, it triggers the latch-off protection immediately after  $t_{DOTP2}$  debounce time.

## Typical Application Circuit (Netbook Adapter by Flyback)

Application	Fairchild Devices	Input Voltage Range	Output
Netbook Adapter	FAN6862W	90~265 V <sub>AC</sub>	19 V / 2.1A (40 W)

### Features

- High efficiency (>85.3% at full-load condition) meeting EPS regulation with enough margin
- Low standby (pin<0.1 W at no-load condition)
- Soft-start time: 5 ms

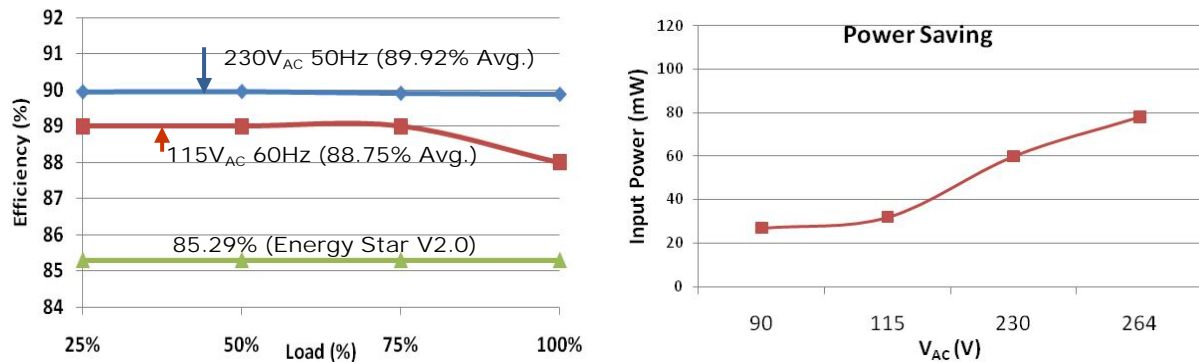


Figure 30. Measured Efficiency and Power Saving

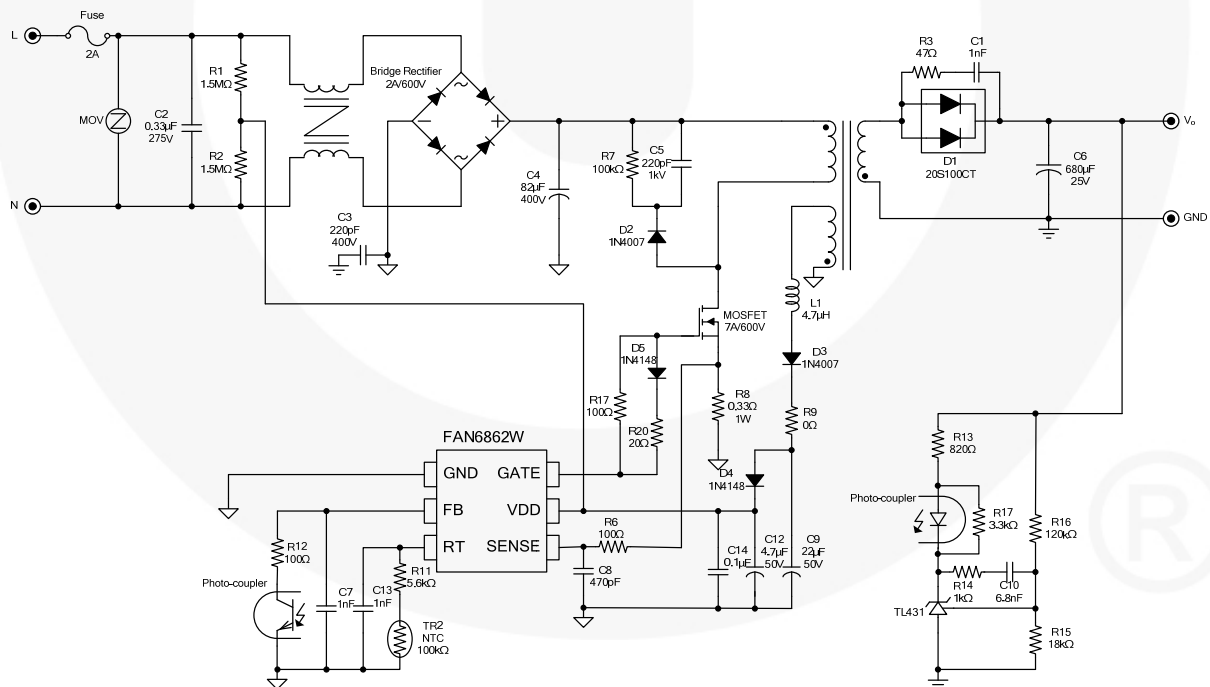


Figure 31. Schematic of Typical Application Circuit

## Transformer Specification

- Core: RM 8
- Bobbin: RM 8

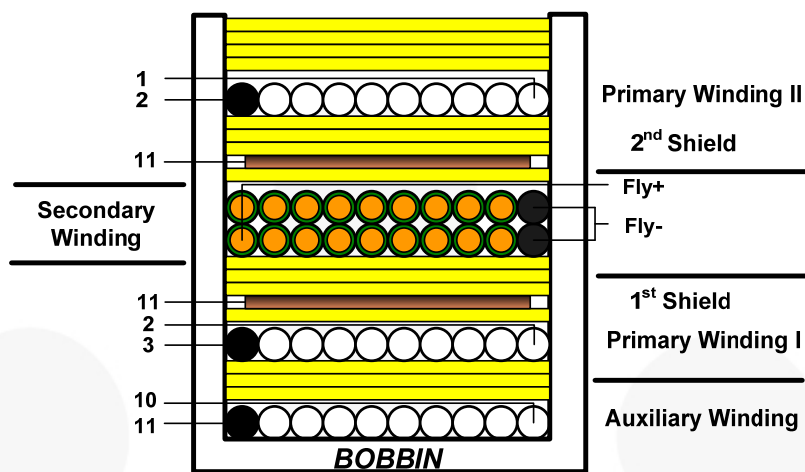
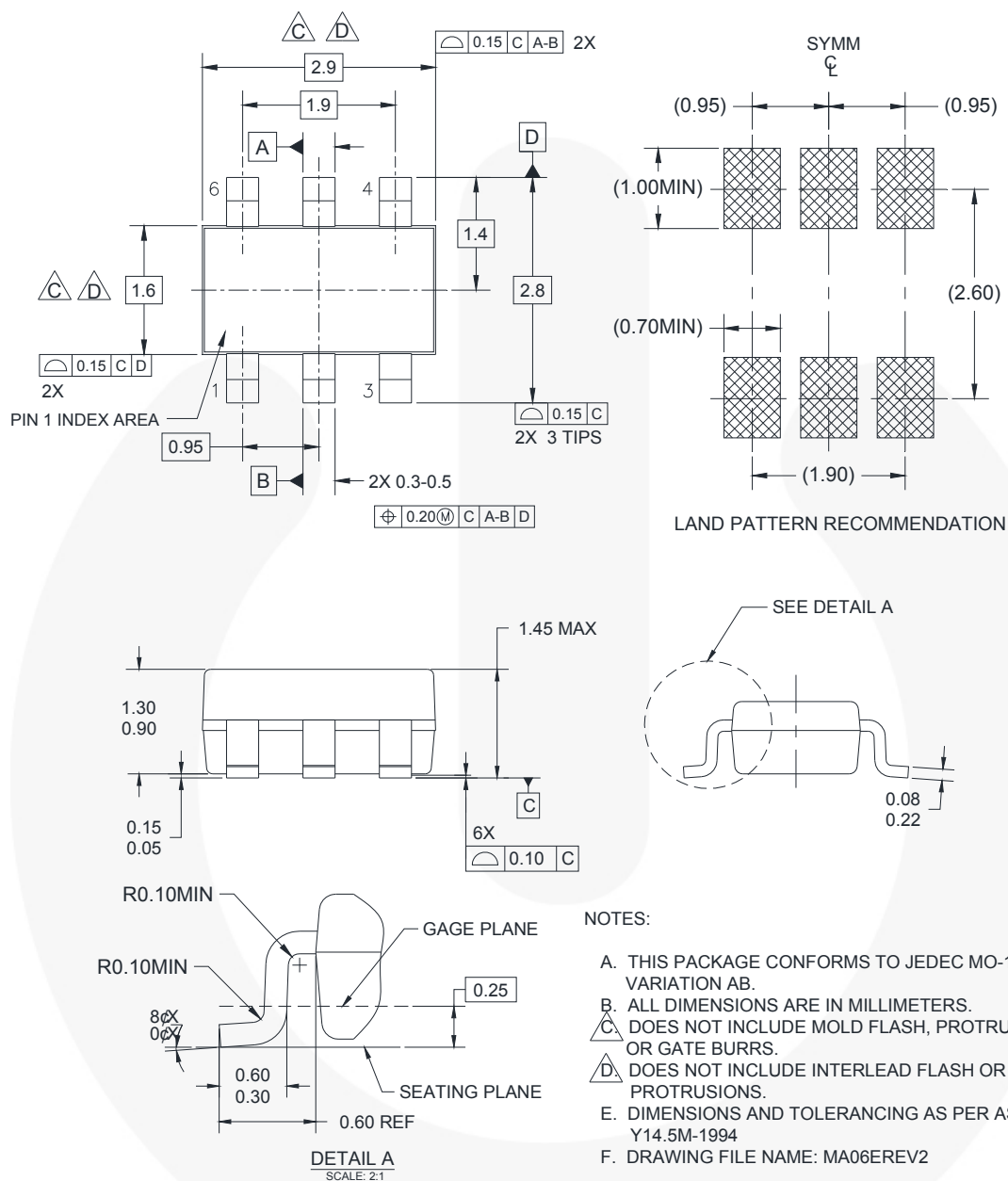


Figure 32. Transformer

NO	Terminal		Wire	Ts	Insulation
	S	F			Ts
N1	11	10	0.25 • 1	9	3
N2	3	2	0.25 • 1	33	1
	11		COPPER SHIELD	1.2	3
N3	Fly-	Fly+	0.5 • 2	12	1
	11		COPPER SHIELD	1.2	3
N4	2	1	0.25 • 1	33	4
			CORE ROUNDING TAPE		3

	Pin	Specification	Remark
Primary-Side Inductance	3—1	920 $\mu$ H $\pm$ 5%	100 kHz, 1 V
Primary-Side Effective Leakage	3—1	15 $\mu$ H Maximum	Short One of the Secondary Windings

## Physical Dimensions



**Figure 33. 6-Lead, SOT23, JEDEC MO-178 Variation AB, 1.6 mm Wide**

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


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FACT®	mWSaver™	SuperSOT™-8	VCM™
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